AT40K05AL, AT40K10AL AT40K20AL, AT40K40AL

5K – 50K Gates Coprocessor FPGA with FreeRAM™

SUMMARY DATASHEET

Features

- Ultra High Performance
    - System Speeds to 100MHz
    - Array Multipliers > 50MHz
    - 10ns Flexible SRAM
    - Internal Tri-state Capability in Each Cell
- FreeRAM™
    - Flexible, Single/Dual Port, Synchronous/Asynchronous 10ns SRAM
    - 2,048 – 18,432 bits of Distributed SRAM Independent of Logic Cells
- 128 – 384 PCI Compliant I/Os
    - Programmable Output Drive
    - Fast, Flexible Array Access Facilitates Pin Locking
    - Pin-compatible with XC4000 and XC5200 FPGAs
- Eight Global Clocks
    - Fast, Low Skew Clock Distribution
    - Programmable Rising/Falling Edge Transitions
    - Distributed Clock Shutdown Capability for Low Power Management
    - Global Reset/Asynchronous Reset Options
    - Four Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
    - Unlimited Re-programmability via Serial or Parallel Modes
    - Enables Adaptive Designs
    - Enables Fast Vector Multiplier Updates
- Pin-compatible Package Options
    - Low-profile, Plastic Quad Flat Packs (LQFP and PQFP)
- User-friendly Design Tools
    - Supoorted by industry standard EDA tools such as Precision Synthesis, Leonardo Spectrum, Synplify, and Others
    - Timing Driven Placement and Routing
    - Automatic/Interactive Multi-chip Partitioning
    - Fast, Efficient Synthesis
    - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic, and RAM Functions
- Supply Voltage 3.3V
- 5V I/O Tolerant

Table 1.   AT40KAL Family[1]

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K – 10K	10K – 20K	20K – 30K	40K – 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496[1]	954[1]	1,520[1]	3,048[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1.   Packages with FCK will have eight less registers.

1.   Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual-port/single-port SRAM, eight global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 114 to 161 in industry standard packages ranging from 144-pin LQFP to 208-pin PQFP, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. The Atmel design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar, and Viewlogic.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution, and other multimedia applications.

1.1   Fast, Flexible, and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, and dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

1.2   Fast, Efficient Array, and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

1.3   Cache Logic Design

The AT40KAL, AT6000, and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

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1.4 Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach, and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. The Atmel PC- based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density, and design flexibility in an FPGA. The cells in the Atmel array are small, efficient, and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

2. Revision History

Doc. Rev.	Date	Comments
G	09/2013	Update Features section, document template, and Atmel logos. Remove 84 PLCC, 100 TQFP, 240 PQFP package options.
F	07/2006	Add Green (Pb/Halide-free/RoHS Compliant) 144-lead LQFP.

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