ATF280F

Rad-Hard Reprogrammable FPGA

DATASHEET

Features

- SRAM-based FPGA designed for Space use
  - 280K equivalent ASIC gates
  - 14,400 cells (two 3-input LUT or one 4-input LUT, one DFF)
  - Unlimited reprogrammability
  - SEE-hardened (Configuration RAM, FreeRAM™, DFF, JTAG, I/O buffers)
  - Rad Hard by Design - No need for mitigation techniques during design
- FreeRAM™
  - 115,200 bits of distributed RAM
  - Organized in 32x4 blocks of RAM
  - Independent of Logic Cells
  - Single/Dual port capability
- Global reset option
- 8 global clocks and 4 fast clocks
- 8 LVDS transceivers and 8 LVDS receivers
- Cold-sparing and PCI-compliant I/Os
- Flexible configuration modes
  - Master/Slave capability
  - Serial/Parallel capability
  - Check of the data during FPGA configuration
- Self Integrity Check (SIC) of the configuration during FPGA operation
- Performance
  - 50MHz system performance
  - 10ns 32X4 FreeRAM™ access time
- Operating range
  - Voltages
    - 1.65V to 1.95V (Core)
    - 3V to 3.6V (Clustered I/Os)
  - Temperature
    - - 55°C to +125°C
- Radiation performance
  - Total dose tested up to 300 krads (Si)
  - No single event latch-up below a LET of 95 MeV/mg/cm2
- ESD better than 2000V for I/O and better than 1000V for LVDS
- Quality grades
  - QML-Q or V
  - ESCC
- Ceramic packages

- 256-pin CQFP (148 I/Os, 8 LVDS Tx and 8 LVDS Rx)
- 352-pin CQFP (249 I/Os, 8 LVDS Tx and 8 LVDS Rx)
- 472-pin CCGA (308 I/Os, 8 LVDS Tx and 8 LVDS Rx)

- Weight: 14.9g (CCGA Package)
- Design Kit including
  - Evaluation board
  - Software design tools
  - ISP probe

Description

The ATF280F is a radiation-hardened reprogrammable FPGA, especially designed for space applications. For low-power consumption applications, the ATF280F is a new device offering many advantages.

The ATF280F supports an innovative built-in SEU protection, which eliminates the need for Triple-Module-Redundancy (TMR). Its re-programmability makes multiple design iterations possible.

The Development Kit enables you to evaluate the ATF280F quickly and economically, running simple demonstrations as well as your complete applications. Throughout your development, from concept to final integration, Atmel provides the tools and support to help you successfully integrate your application into the ATF280F.

The ATF280F is available in CCGA/CLGA 472 packages and features up to 308 standard I/Os and 16 LVDS I/Os for the user application. The CQFP256 and CQFP352 packages are also available for applications requiring fewer I/O's.

Table 1. ATF280F Summary

Function	ATF280F
Available ASIC Gates (50% typ. routable)	280K
Rows x Columns	120x120
Core Cells	14 400
RAM Bits	115 200
I/O max	308

Figure 2. ATF280F Overview

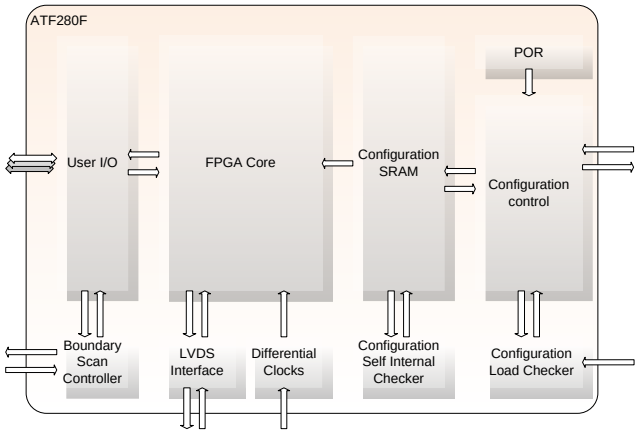


Table of Contents

1. Glossary

FPGA	Field Programmable Gate Array
POR	Power On Reset
SRAM	Static Random Access Memory
SEU	Single Event Unit
CSIC	Configuration Self Internal Checker

2. Pin Description

The ATF280F is a built over a standard Atmel AT40K FPGAs architecture in which most of the pins support multiplexed functions. The various functions families available for the ATF280F FPGA are presented here after:

- [GPIO] : General Purpose Input/Output functions,
- [CFG] : Configuration management functions,
- [CLOCK] : Clock management functions,
- [LVDS] : LVDS I/O functions,
- [JTAG] : JTAG functions,
- [PWR] : Power Supply functions.

In the following section, a complete description of the functions available for each pin is given. The family to which each function belongs to is precised.

2.1 General Purpose IOs

IOx - General Purpose IO

[GPIO] The general purpose IOs are used to communicate with the peripherals interconnected together with the FPGA. The general purpose IOs are highly configurable. A versatile direction management is proposed, allowing configuration of the IO in any of the following directions: input, output or bidirectional. It is also possible to configure Schmitt trigger on inputs, PCI compatibility for output, pull-up/down for input/output…The general purpose IOs provides also the possibility to configure the output buffer current drive.

2.2 Configuration Interface

RESETN - FPGA Reset

[CFG] RESETN is the manual reset of the FPGA. This function reset the configuration download logic. RESETN is internally pulled up to VCC and is active at a low level. Each time RESETN is activated, the FPGA enters Manual Reset lifephase.

M0, M1, M2 – Configuration Mode

[CFG] The configuration mode pins are used to define the configuration settings of the FPGA. ATF280F samples the configuration mode pins each time a configuration clear cycle is ended.

Caution: The mode pins should not be changed during power-on-reset or manual reset.

IO303_INIT – Multiplexed General Purpose IO / Configuration Error Indicator

[CFG] INIT is globally used as an error indicator regarding configuration logic. INIT can also be used to hold the configuration download start in master mode 0 while tied to a low level prior to CCLK emission. INIT is a bidirectional open drain I/O pulled up to VCC with an internal resistor.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

CON – Configuration Status Indicator

[CFG] CON is the FPGA configuration start and status pin. It is a bidirectional open drain I/O pulled up to VCC with an internal resistor.

CCLK – Configuration Clock

[CFG] CCLK function provides the clock signal used by the configuration logic. Depending on the mode used for configuration download procedure, CCLK function is configured as input or output. For slave mode, the CCLK is configured as an input whereas for master mode, it is configured as an output. When configured in input mode, CCLK is pulled up to VCC with an internal resistor.

IO713_D0 – Multiplexed General Purpose IO / Configuration Data

[CFG] D0 is used to transfer configuration data from or to the FPGA configuration SRAM. D0 is used for serial mode configuration and can be used together with D1 to D15 for parallel mode configuration.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IOx_Dy – Multiplexed General Purpose IO / Configuration Data

[CFG] D1:D15 are the upper bits of the 8/16-bit parallel data bus used to download configuration data to the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO259_LDC – Multiplexed General Purpose IO / Configuration Status Indicator

[CFG] LDC indicates that the configuration download is on-going. LDC is an output and is polarized to a low logic level during the configuration.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO265_HDC - Multiplexed General Purpose IO / Configuration Status Indicator

[CFG] HDC indicates that the configuration download is on-going. HDC is an output and is polarized to a high logic level during the configuration.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO547_CS0 - Multiplexed General Purpose IO / Serial Configuration Chip Select

[CFG] CS0 is an active low chip select used during configuration. It is only available configuration download slave serial mode 1.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO743_A2_CS1 - Multiplexed General Purpose IO / Parallel Configuration Chip Select / Configuration Address

[CFG] CS1 is an active low chip select used during configuration. It is only available configuration download slave parallel mode 2.

[CFG] A0:A19 are used to control external addressing of the memories during downloads.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO720_GCK6_CSOUT - Multiplexed General Purpose IO / Clock / Configuration Select Output

[CFG] CSOUT is the configuration pin used to enable the downstream device in an FPGA cascade chain.

[CLOCK] GCK6 function is used to provide clock signals over the entire surface of the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IOx_Az - Multiplexed General Purpose IO / Configuration Address

[CFG] A0:A23 are used to control external addressing of the memories during downloads.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IOx_GCKy_Az - Multiplexed General Purpose IO / Clock / Configuration Address

[CFG] A0:A23 are used to control external addressing of the memories during downloads.

[CLOCK] GCK function is used to provide clock signals over the entire surface of the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO655_CHECKN - Multiplexed General Purpose IO / Configuration Check

[CFG] CHECKN pin is used to enable the CHECK function when combined with a configuration download start.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO225_OTSN - Multiplexed General Purpose IO / Tri-State Command

[CFG] OTSN pin is used to tri-state all the FPGA pins configured as user I/Os.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

2.3 LVDS Interface

ILVDSx / ILVDSNx - LVDS Receiver Differential Pair (Input)

[LVDS] ILDVSx/ILVDSNx receiver is a pair of differential signals that comply with the LVDS standard.

OLVDSx / OLVDSNx - LVDS Driver Differential Pair (Output)

[LVDS] OLDVSx/OLVDSNx transmitter is a pair of differential signals that comply with the LVDS standard.

VREF - LVDS reference voltage

[LVDS] VREF is the reference voltage for LVDS transmission operations. Each LVDS cluster has dedicated VREF source. It shall be accurately power supplied to 1.25V to comply with the LVDS standard.

2.4 Clocks Interface

IOx_FCKy - Multiplexed General Purpose IO / Fast Clock

[CLOCK] FCK function is used to provide high frequency clock to part of the design.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IOx_GCKy - Multiplexed General Purpose IO / Clock

[CLOCK] GCK function is used to provide clock signals over the entire surface of the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IOx_GCKy_Az - Multiplexed General Purpose IO / Clock / Configuration Address

[CFG] A0:A23 are used to control external addressing of the memories during downloads.

[CLOCK] GCK function is used to provide clock signals over the entire surface of the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

IO720_GCK6_CSOUT - Multiplexed General Purpose IO / Clock / Configuration Select Output

[CFG] CSOUT is the configuration pin used to enable the downstream device in an FPGA cascade chain.

[CLOCK] GCK6 function is used to provide clock signals over the entire surface of the FPGA.

[GPIO] General Purpose IO functionalities apply to this signal when used in IO mode.

2.5 JTAG

TRST - Test Reset (pull-down input)

[JTAG] This asynchronous active low input resets the TAP when asserted.

This signal is meant for board testing purpose and shall be driven low in the final application.

TCK - Test Clock (pull-up input with Schmitt trigger)

[JTAG] This input is used to clock state information and test data into and out of the device during operation of the TAP.

TMS - Test Mode select (pull-up input)

[JTAG] This synchronous input is used to control the state of the TAP controller in the device.

TDI - Test data input (pull-up input)

[JTAG] This input is used to serially shift test data and test instructions into the device during TAP operation.

TDO - Test data output (tri-statable output)

[JTAG] This input is used to serially shift test data and test instructions out of the device during TAP operation.

Caution: Refer to Erratum 2: TRST JTAG pin.

2.6 Power Supply

VDD - Core Power Supply

[PWR] VDD is the power supply input for the ATF280F core.

VCC - I/O Power Supply

[PWR] VCC is the power supply input for the programmable I/Os. Each I/O cluster has dedicated VCCy sources where ‘y’ is the cluster number (1 < y < 8).

VCCB - LVDS I/O Power Supply

[PWR] VCCB is the power supply input for the LVDS I/Os. Each pair of LVDS channels has a dedicated VCCB sources.

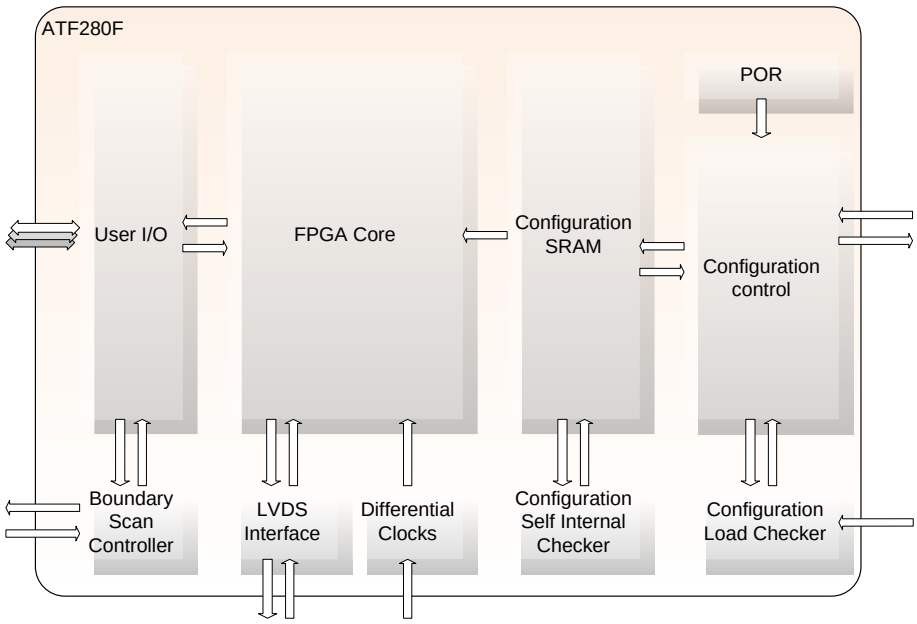
VSS - Ground

3. Architecture

The ATF280F architecture is developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

Here is an overview of the internal architecture of the ATF280F:

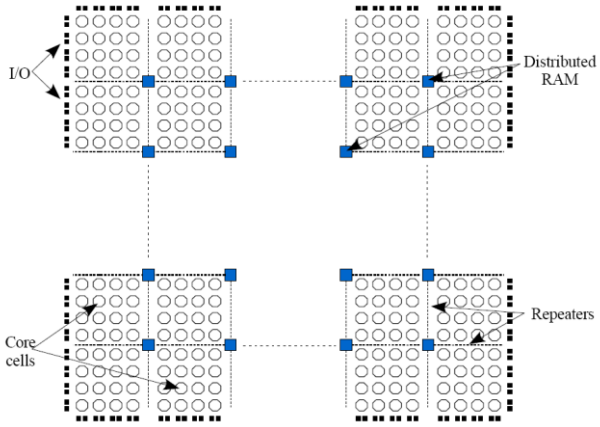
Figure 3-1. ATF280F Architecture Overview



3.1 FPGA Core

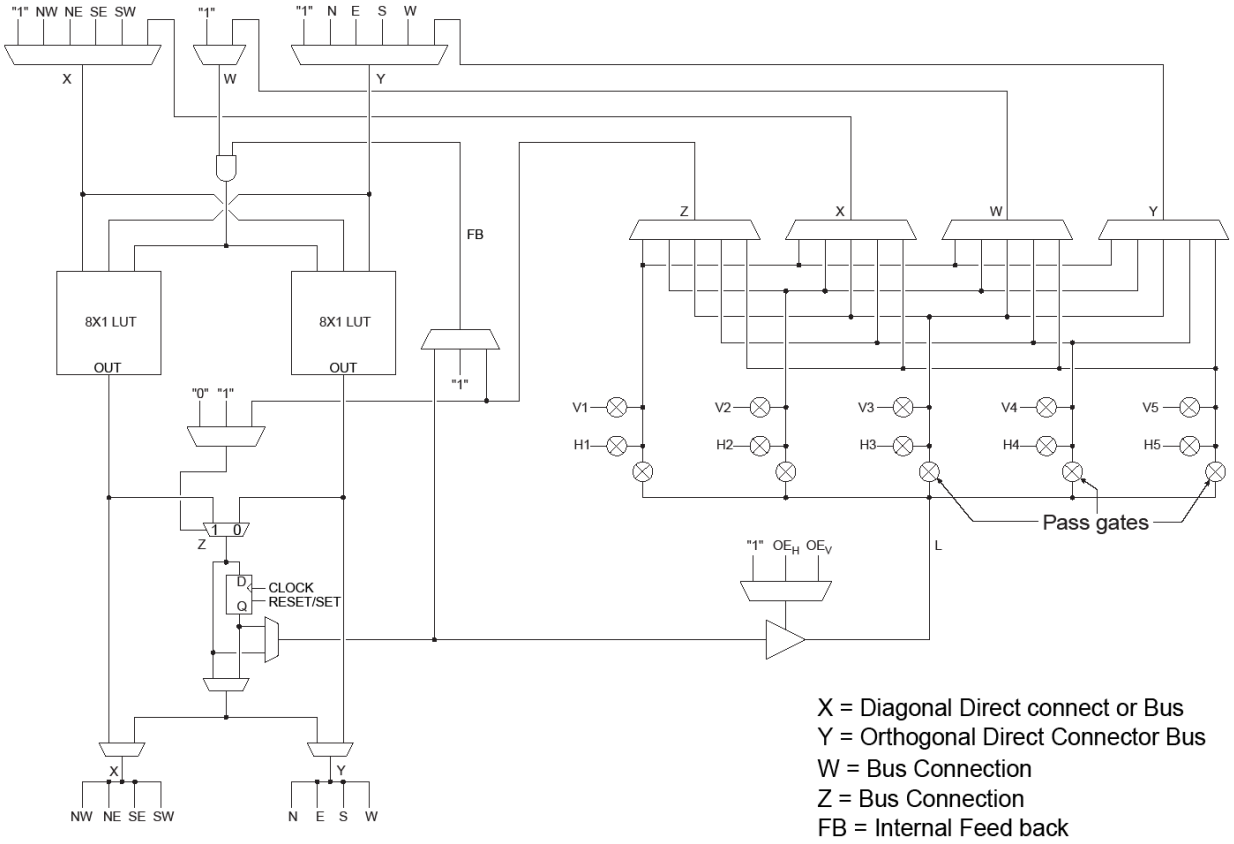
At the heart of the Atmel ATF280F architecture is a symmetrical array of identical cells. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells. At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses.

Figure 3-2. Core device overview



The following figure depicts the ATF280F cell which is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), and which can be combined to produce one 4-input LUT. This means that any cell can implement two functions of 3 inputs or one function of 4 inputs.

Figure 3-3. ATF280F Core Cell



Every cell includes a register element, a D-type flip-flop, with programmable clock and reset polarities. The initialization of the register is also programmable. It can be either SET or RESET. The flip-flop can be used to register the output of one of the LUT. It can also be exploited in conjunction with the feedback path element to implement a complete ripple counter stage in a single cell. The registered or unregistered output of each LUT can be feedback within the cell and treated as another input. This allows, for example, a single counter stage to be implemented within one cell without using external routing resources for the feedback connection.

There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers as the product and carry terms can both be generated within a single logic cell.

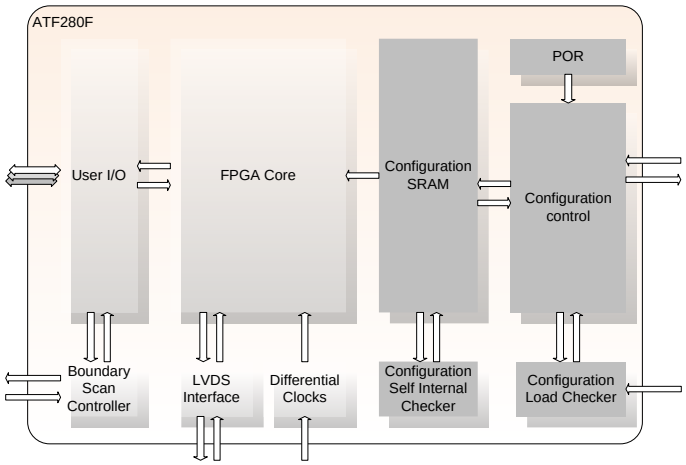
The cell flexibility makes the ATF280F architecture well suited for most of the digital design application areas.

3.2 Configuration Logic

The ATF280F FPGA embeds the configuration logic function which is responsible of the configuration download. The configuration download is the operation by which the FPGA configuration SRAM is written in order to load the FPGA application. The configuration download operation is fully detailed in **Configuration Download** section of this document.

The configuration logic is based on the 5 modules highlighted in the following figure.

Figure 3-4. Configuration Logic Highlight



3.2.2 POR

The POR module is an analogic structure which senses the rise of the VDD Power Supply. While VDD is under the POR threshold, all the FPGA logic is maintained in a reset state. Once, the Vdd rises above the POR threshold, all the FPGA logic is activated (leaves reset state) and the FPGA enters in ***Power-On Reset*** lifephase.

3.2.3 Configuration Control

The Configuration Control module is the main module of the configuration logic. It interfaces directly the POR module in order to manage the ***Power-On Reset*** lifephase. It also manages the configuration SRAM module and is capable to access SRAM cells in read or write mode. It drives the external configuration interface signals used to manage the configuration download. To finish, the configuration control is interconnected with the Configuration Load Checker module to ensure the integrity of the communication protocol.

3.2.4 Configuration SRAM

The configuration SRAM module is made of a large set of SRAM memory points distributed through the whole FPGA. The configuration SRAM is fully cleared during the ***Power-On Reset*** and ***Manual Reset*** lifephases. It is written during ***Configuration Download*** lifephase with the bitstream data in order to configure the FPGA matrix. The configuration SRAM can also be read for integrity verification when using special function such as CHECK function or CSIC function. Refer to **Configuration Integrity Management** section for detailed description of those functions.

3.2.5 Configuration Load Checker

The Configuration Load Checker module is responsible of the protection of the configuration download link. During the ***Configuration Download*** lifephase it manages the errors which are protocol relevant and informs the configuration control module of any error in such a way that the configuration control module can drive the appropriate error status signals to inform the system that an error occurred during the configuration.

3.2.6 Configuration Self Internal Checker

The Configuration Self Internal Checker module is responsible of the integrity of the data during the ***Run*** lifephase. Once the configuration SRAM is written with the appropriate data, the ATF280F FPGA is capable to check all its effective configuration data and to notify the user in case of errors inside the configuration SRAM. This mechanism is useful to detect SEU that occur on the configuration SRAM.

3.3 User I/O

Depending on the package selected, the ATF280F features up to 308 general purpose IO for end user application. Each IO can be individually adjusted to the application needs thanks to its extensive configurability. All the IOs are cold sparing, have PCI compliance capability…

Please refer to the General Purpose Interface section for detailed information on the User IOs.

3.4 LVDS I/O

The ATF280F provides a 200MHz LVDS interface with cold sparing feature. This interface can be used for high speed communication between the FPGA and its peripherals in order to exchange large amount of data.

Please refer to the LVDS Interface section for detailed information on the LVDS IOs

3.5 Clock

Please refer to the Clock section for detailed information on clock system implemented on the ATF280F.

3.6 JTAG

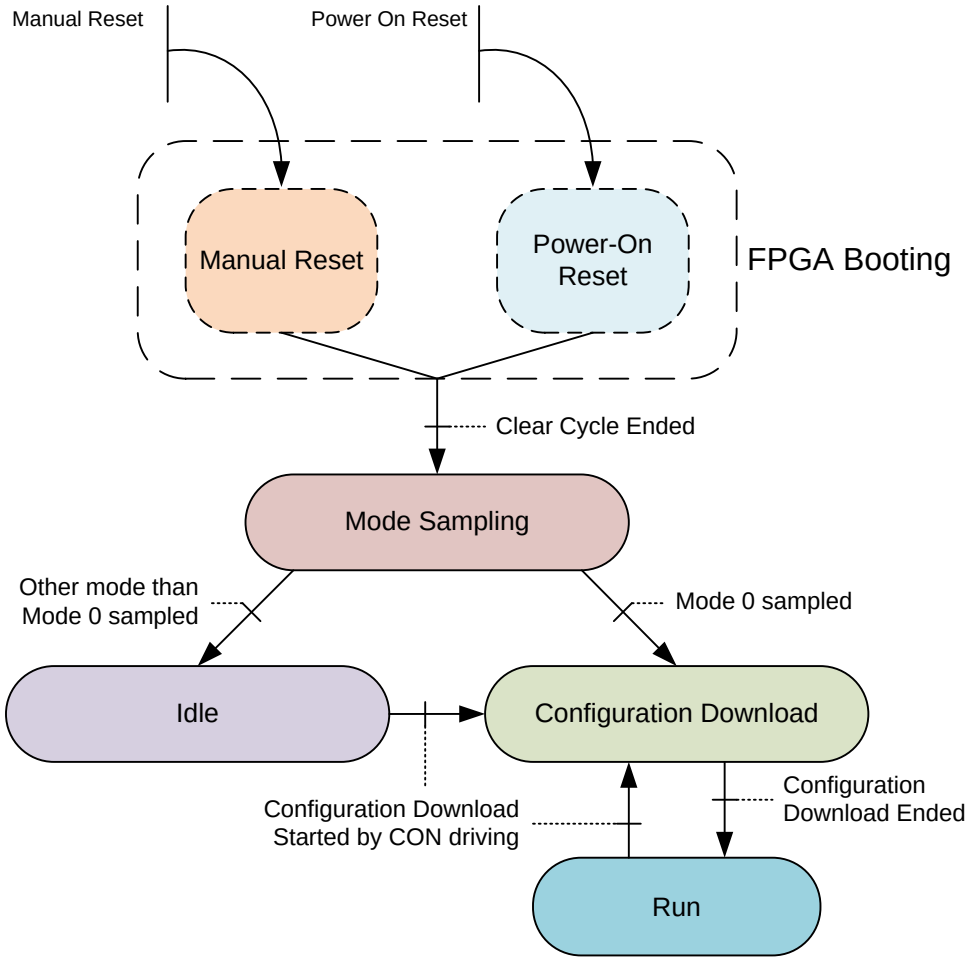
The ATF280F implements a standard interface compliant with the IEEE 1149.1 JTAG specification. This interface can be used for PCB testing using the JTAG boundary-scan capability.

Caution: Refer to Erratum 1: JTAG functionality.

4. Operating Modes / Lifephases

The ATF280F FPGA behaves following a deterministic life cycle. The complete life cycle of the FPGA refers to an optimized number of lifephases that are summarized in the following life cycle.

Figure 4-1. ATF280 FPGA: Life Cycle diagram



For some of the FPGA IOs, the general purpose function of the IO is multiplexed with other functions such as configuration function, clock function… as mentioned in the Pin Description section. For the multiplexed IOs, the function that is activated at a given time is directly dependent from the lifephase currently executed.

In each of the lifephase description here after, the multiplexed IO function availability is presented.

4.2 Power-On Reset

4.2.1 Description

This ***Power-On Reset*** lifephase occurs when power is first applied to the part. The FPGA initiates a complete clearing of its internal configuration SRAM (configuration clear cycle) prior entering in Mode Sampling lifephase. Before performing the configuration clear cycle, the power supply is sensed until the threshold voltage is reached then the internal logic activates.

In order to ensure the power supply stability to erase properly each configuration SRAM point, the ATF280F loops and perform configuration clear cycle during hardcoded silicon timing.

4.2.2 Pin Function Availability

Table 4-1. Pin Function during Power-On Reset

ATF280 Pin names	Lifephase = Power-On Reset
RESET*	[CFG]
M0, M1, M2	[CFG]
IO303_INIT	[CFG]
CON	[CFG]
CCLK	[CFG]
IO713_D0	[CFG]
IOx_Dy	[GPIO][1]
IO259_LDC	[CFG]
IO265_HDC	[CFG]
IO547_CS0	[GPIO][1]
IO743_A2_CS1	[GPIO][1]
IO720_GCK6_CSOUT	[GPIO][1]
IOx_Az	[GPIO][1]
IOx_GCKy_Az	[GPIO][1]
IO655_CHECKN	[GPIO][1]
IO225_OTSN	[GPIO][1]
IOx	[GPIO][1]
IOx_GCKy	[GPIO][1]
IOx_FCKy	[GPIO][1]

Notes: 1. During Power-On Reset lifephase, the ATF280F FPGA configuration SRAM is not configured, all GPIO functions remain in input with pull-up (by default).

4.3 Manual Reset

4.3.1 Description

This ***Manual Reset*** lifephase occurs when the RESET function is activated by the user. The FPGA initiates a configuration clear cycle prior entering Mode Sampling lifephase when RESET function is released. As power supplies are already stable, the configuration clear cycle is done once and takes a time which depends of the silicon intrinsic speed and the size of the FPGA matrix.

4.3.2 Pin Function Availability

Table 4-2. Pin Function during Manual Reset

ATF280 Pin names	Lifephase = Manual Reset
RESET*	[CFG]
M0, M1, M2	[CFG]
IO303_INIT	[CFG]
CON	[CFG]
CCLK	[CFG]
IO713_D0	[CFG]
IOx_Dy	[GPIO][1]
IO259_LDC	[CFG]
IO265_HDC	[CFG]
IO547_CS0	[GPIO][1]
IO743_A2_CS1	[GPIO][1]
IO720_GCK6_CSOUT	[GPIO][1]
IOx_Az	[GPIO][1]
IOx_GCKy_Az	[GPIO][1]
IO655_CHECKN	[GPIO][1]
IO225_OTSN	[GPIO][1]
IOx	[GPIO][1]
IOx_GCKy	[GPIO][1]
IOx_FCKy	[GPIO][1]

Notes: 1. During Manual Reset lifephase, the ATF280F FPGA configuration SRAM is not configured, all GPIO functions remain in input with pull-up (by default).

4.4 Mode Sampling

4.4.1 Description

This ***Mode Sampling*** lifephase is entered each time the FPGA has performed either Power-On-Reset or Manual Reset lifephases. In this state, the FPGA starts to drive the configuration logic interface approprietaly and samples the mode pins. Depending on the values sampled through the mode pins, the ATF280F FPGA can be configured in the following modes:

- Mode 0: Master Serial Mode
- Mode 1: Slave Serial Mode with the use of a chip select input
- Mode 7: Slave Serial Mode
- Mode 2: Parallel Serial Mode with the use of a chip select input
- Mode 6: Parallel Serial Mode with the use of an address bus output

These modes directly affect the ***Configuration Download*** lifephase and lead to five different contexts for these these lifephase.

4.4.2 Pin Function Availability

Table 4-3. Pin Function Mode Sampling

ATF280 Pin names	Lifephase = Mode Sampling
RESET*	[CFG]
M0, M1, M2	[CFG]
IO303_INIT	[CFG]
CON	[CFG]
CCLK	[CFG]
IO713_D0	[CFG]
IOx_Dy	[GPIO][1]
IO259_LDC	[CFG]
IO265_HDC	[CFG]
IO547_CS0	[GPIO][1]
IO743_A2_CS1	[GPIO][1]
IO720_GCK6_CSOUT	[GPIO][1]
IOx_Az	[GPIO][1]
IOx_GCKy_Az	[GPIO][1]
IO655_CHECKN	[GPIO][1]
IO225_OTSN	[GPIO][1]
IOx	[GPIO][1]
IOx_GCKy	[GPIO][1]
IOx_FCKy	[GPIO][1]

Notes: 1. During Manual Reset lifephase, the ATF280F FPGA configuration SRAM is not configured, all GPIO functions remained in input with pull-up (by default).

4.5 Idle

4.5.1 Description

This ***Idle*** lifephase is entered when the FPGA does no activitie. The FPGA enters in this state after Mode Sampling state when configured in slave mode. In Idle state, the configuration logic interface is released.

4.5.2 Pin Function Availability

Table 4-4. Pin Function during Idle

ATF280 Pin names	Lifephase = Idle
RESET*	[CFG]
M0, M1, M2	[CFG]
IO303_INIT	[GPIO][1]
CON	[CFG]
CCLK	[CFG]
IO713_D0	[GPIO][1]
IOx_Dy	[GPIO][1]
IO259_LDC	[GPIO][1]
IO265_HDC	[GPIO][1]
IO547_CS0	[GPIO][1]
IO743_A2_CS1	[GPIO][1]
IO720_GCK6_CSOUT	[GPIO][1]
IOx_Az	[GPIO][1]
IOx_GCKy_Az	[GPIO][1]
IO655_CHECKN	[GPIO][1]
IO225_OTSN	[GPIO][1]
IOx	[GPIO][1]
IOx_GCKy	[GPIO][1]
IOx_FCKy	[GPIO][1]

Notes: 1. During Idle lifephase, the ATF280F FPGA configuration SRAM is not configured, all GPIO functions remained in input with pull-up (by default).

4.6 Configuration Download

4.6.1 Description

This ***Configuration Download*** lifephase from a system point of view is a sequence of event managed by the FPGA in order to ensure the configuration of its internal SRAM. This lifephase is entered after Mode Samping state when configured in master mode. Else the FPGA enters this lifephase after Idle state when an external master triggers the start of configuration download (could be either in slave or master mode).

Five different contexts are defined for this lifephase regarding the mode sampled in Mode Sampling.

4.6.2 Pin Function Availability

Table 4-5. Pin Function during Configuration Download

ATF280 Pin names	Lifephase = Configuration Download				
	Mode 0	Mode 1	Mode 7	Mode 2	Mode 6
RESET*	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
M0, M1, M2	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
IO303_INIT	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
CON	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
CCLK	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
IO713_D0	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
IOx_Dy	[GPIO][1]	[GPIO][1]	[GPIO][1]	[CFG][4]	[CFG][4]
IO259_LDC	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
IO265_HDC	[CFG]	[CFG]	[CFG]	[CFG]	[CFG]
IO547_CS0	[GPIO][1]	[CFG]	[GPIO][1]	[GPIO][1]	[GPIO][1]
IO743_A2_CS1	[GPIO][1]	[GPIO][1]	[GPIO][1]	[CFG][2]	[CFG][2]
IO720_GCK6_CSOUT	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]
IOx_Az	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]
IOx_GCKy_Az	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]
IO655_CHECKN	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]
IO225_OTSN	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]	[CFG] or [GPIO][3]
IOx	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]
IOx_GCKy	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]
IOx_FCKy	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]	[GPIO][1]

Notes:
1. If entering Configuration lifephase from Idle then the ATF280F FPGA configuration SRAM is not configured: all GPIO functions remained in input with pull-up (by default). Else if entering Configuration lifephase from Run then the ATF280 FPGA configuration SRAM is already configured: all GPIO functions remained in their configured state.
2. IO743_A2_CS1 has two possibilities regarding [CFG] function. When slave parallel mode 2 is set, CS1 is used as chip select of the FPGA. When slave parallel mode 6 is set, A2 is used to address an external parallel EEPROM.

3. IO720_GCK6_CSOUT, IO655_CHECKN and IO225_OTSN are configured in [CFG] function during configuration download if the appropriate function is activated (respectively cascading mode, CHECK function, Output Tri-State) (Refer to bitstream configuration for more details)
4. IOx_Dy pins ensure the data wide access in 8 or 16 bits. When parallel mode is set (mode 2 or 6), I0x_D[1:7] are always configured as [CFG] function. By the way, IOx_D[8:15] are configured as [CFG] function only if 16 bits access is configured (refer to Bitstream configuration for more details) else they remain as [GPIO] function.

4.7 Run

4.7.1 Description

The ***Run*** lifephase is the operating state of the FPGA and is design dependent. It means that in this lifephase, the loaded design runs and its own lifephases are taken into account.

4.7.2 Pin Function Availability

Table 4-6. Pin Function during Run

ATF280 Pin names	Lifephase = Run			
	Nominal	OTS	CSIC	Free Run oscillator
RESET*	[CFG]	[CFG]	[CFG]	[CFG]
M0, M1, M2	[CFG]	[CFG]	[CFG]	[CFG]
IO303_INIT	[GPIO]	[GPIO]	[CFG]	[GPIO]
CON	[CFG]	[CFG]	[CFG]	[CFG]
CCLK	[CFG]	[CFG]	[CFG]	[CFG][1]
IO713_D0	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IOx_Dy	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO259_LDC	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO265_HDC	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO547_CS0	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO743_A2_CS1	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO720_GCK6_CSOUT	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]
IOx_Az	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IOx_GCKy_Az	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]
IO655_CHECKN	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IO225_OTSN	[GPIO]	[CFG]	[GPIO]	[GPIO]
IOx	[GPIO]	[GPIO]	[GPIO]	[GPIO]
IOx_GCKy	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]
IOx_FCKy	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]	[GPIO]or[CLOCK]

Notes: 1. When using the Free Run Oscillator in mode 0 only (refer to **Register** section about CR13), the CCLK pin is output as clock signal. The user shall take care of this at system level.

5. Configuration Download

Configuration is the process by which a design is loaded into an ATF280F FPGA. The ATF280F device is a SRAM based FPGA, this leads to an unlimited reprogrammability capability.

It is possible to configure either the entire device or only a portion of the device. Sections can be configured while others continue to operate undisturbed. The architecture of the ATF280F leads to a maximum bitstream size of 2.5M bits. It is possible to store configuration bit-streams of the ATF280F in one single 4Mbit EEPROM.

Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration data is transferred to the device in one of the five modes supported by the ATF280F. Three dedicated input pins M0, M1 and M2 are used to determine the configuration mode.

The ATF280F supports an auto-configuring Master serial mode, two Slave serial modes and two Slave parallel modes.

The following table summarizes the ATF280F configuration modes:

Table 5-1. Configuration Mode Overview

Configuration Download Mode						
Mode	**Description**	**M2**	**M1**	**M0**	**CCLK**	**Data**
0	Master serial	0	0	0	Output	Serial
1	Slave serial	0	0	1	Input	Serial
7	Slave serial	1	1	1	Input	Serial
2	Slave parallel	0	1	0	Input	8/16 bits Word
6	Slave parallel	1	1	0	Input	8/16 bits Word

5.2 Serial Configuration

5.2.1 Bitstream Structure

The configuration bitstream for the ATF280F FPGA consists in a flexible structured set of data that allows configuration of the FPGA structure but also protection of the configuration data link.

The following table shows the global structure of a bitstream for ATF280F FPGA.

Table 5-2. ATF280F Bitstream structure

Bitstream decomposition		
Description	Sub Zone	Zone Size (byte)
Null byte		1
Preamble		1
Configuration Registers	CR3	4
	CR2	
	CR1	
	CR0	
Number of Windows		2
Data Window1	Start Address	3
	Stop Address	3
	Data	Data Size
Data Window2	Start Address	3
	Stop Address	3
	Data	Data Size
Data WindowN [1]	Start Address	3
	Stop Address	3
	Data	Data Size
Checksum	Start Address	3
	Stop Address	3
	Data	1
Recurrent Checksum [2]	Start Address	3
	Stop Address	3
	Data	1
Postamble		1

Notes: 1. N could be at least 1, at maximum 65535.

2. Recurrent Cheksum (optional) is integrated by IDS into the bitstream by activating the appropriate option (CR8 in configuration Register)

5.2.1.2 Null Byte

The “null byte” is always present in the ATF280F bitstreams. It is used by the configuration download state machine as a download protocol start indicator.

Its value is always “00000000”.

5.2.1.3 Preamble

The “preamble” is always present in the ATF280F bitstreams. It is used by the configuration download state machine for verifying that the bitstream proposed on the configuration link is well suited for ATF280F FPGA type.

Its value is always set to “10110111”

5.2.1.4 Configuration Register

The configuration register is made of four eight-bit wide registers used to configure the FPGA embedded functions. These register allows configuration of FPGA functions such as clock configuration, IO configuration… options. For the details on the configuration register options content, please refer to the ***Registers*** section.

The configuration registers are always present in the ATF280F bitstreams.

5.2.1.5 Number of Windows

The number of windows section provides the exact number of windows used in the bitstream to be downloaded. Its value is computed by the FPGA Integrated Design System development tool and is fully dependent from the content of the FPGA application.

The number of windows is always present in an ATF280F bitstream.

5.2.1.6 Data Window

The windows are the zones used to configure the different internal applicative structures of the FPGA. Each window is e made of the following elements:

- A “Start Address” which is a 24 bits word (3 bytes). It is used to identify the starting point of the FPGA configuration SRAM mapping to be written
- A “Stop Address” which is a 24 bits word (3 bytes). It is used to delimit the end of the window, thus defining the number of data to be written in the configuration SRAM
- The “Data” section which contains the configuration data for the configuration memory itself. It is fully dependent upon the application being downloaded.

The ATF280F bitstream always embeds a minimum of one data windows.

5.2.1.7 Checksum Window

The FPGA Integrated Design System development tool calculates a checksum for each generated bitstream in order to provide the capability to secure the transfer of the data during configuration download. The checksum generated is one byte computed by data accumulation over the configuration registers data and the data of all the windows that precede the checksum window.

The checksum window is used to store this checksum into the FPGA at a defined location. That is why the checksum window is made of:

- A “Start Address” which is a 24 bits word (3 bytes). This address defines the location where the checksum will be written in the FPGA.
- A “Stop Address” which is a 24 bits word (3 bytes) to delimit the end of the window,
- The “Checksum Data”

The checksum window is always present in an ATF280F bitstream.

5.2.1.8 Recurrent Checksum

The FPGA Integrated Design System development tool is capable to calculate a recurrent checksum for each generated bitstream. The recurrent checksum is different from the simple checksum. It is used for self integrity checking. The recurrent checksum is computed by data accumulation over the configuration registers data and the data of all the windows that precede the recurrent checksum window.

The “Recurrent Checksum” window is made of the following elements:

- The “Start Address” which is a 24 bits word (3 bytes) to access the Recurrent Checksum location in the FPGA
- The “Stop Address” which is a 24 bits word (3 bytes) to delimit the end of the window
- The “Recurrent Checksum Data”

The recurrent checksum window is optional. It is only available when the recurrent checksum function is activated in the bitstream. For details on the recurrent checksum function usage, please refer to the **Self Integrity Checker function** section.

5.2.1.9 Postamble

The “postamble” is always present in the ATF280F bitstreams. It is used by the configuration download state machine as a download protocol stop indicator indicating the end of the transfer.

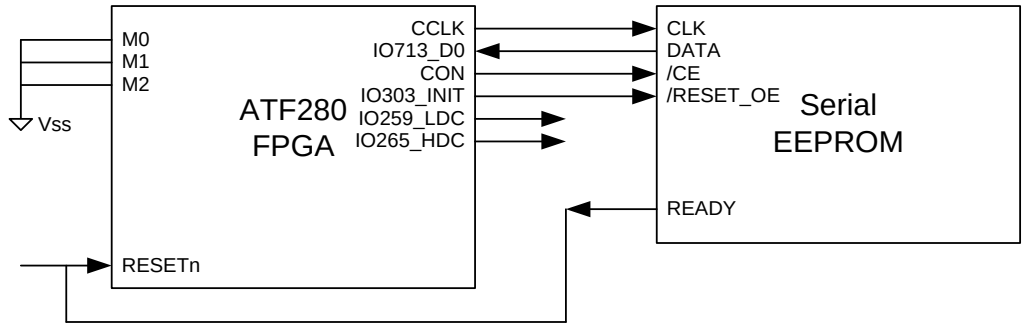
Its value is always “10110111”.

5.3 Master Mode – Mode 0

Mode 0 is a master mode. The Master Mode is auto-configuring; that is, after power-on-reset (POR) and the clearing of configuration memory, it self-initiates configuration. The Master Mode uses an internal oscillator to provide CCLK for clocking the external EEPROMs (configurators) which contain the configuration data. CCLK also drives the downstream devices (Slaves) in the configuration cascade chain. Master Serial Mode clocks and receives data from an EEPROM Serial Configuration Memory. After auto-configuration is complete, re-configuration can be initiated manually by the user.

In this mode, the ATF280F is coupled to a serial EEPROM and managed automatically the whole configuration download phase. The automatic configuration download always starts after a Power-On reset or a Manual Reset (Refer to Chapter 3). The following synoptic shows the required interface to be used for automatic configuration download purpose in mode 0.

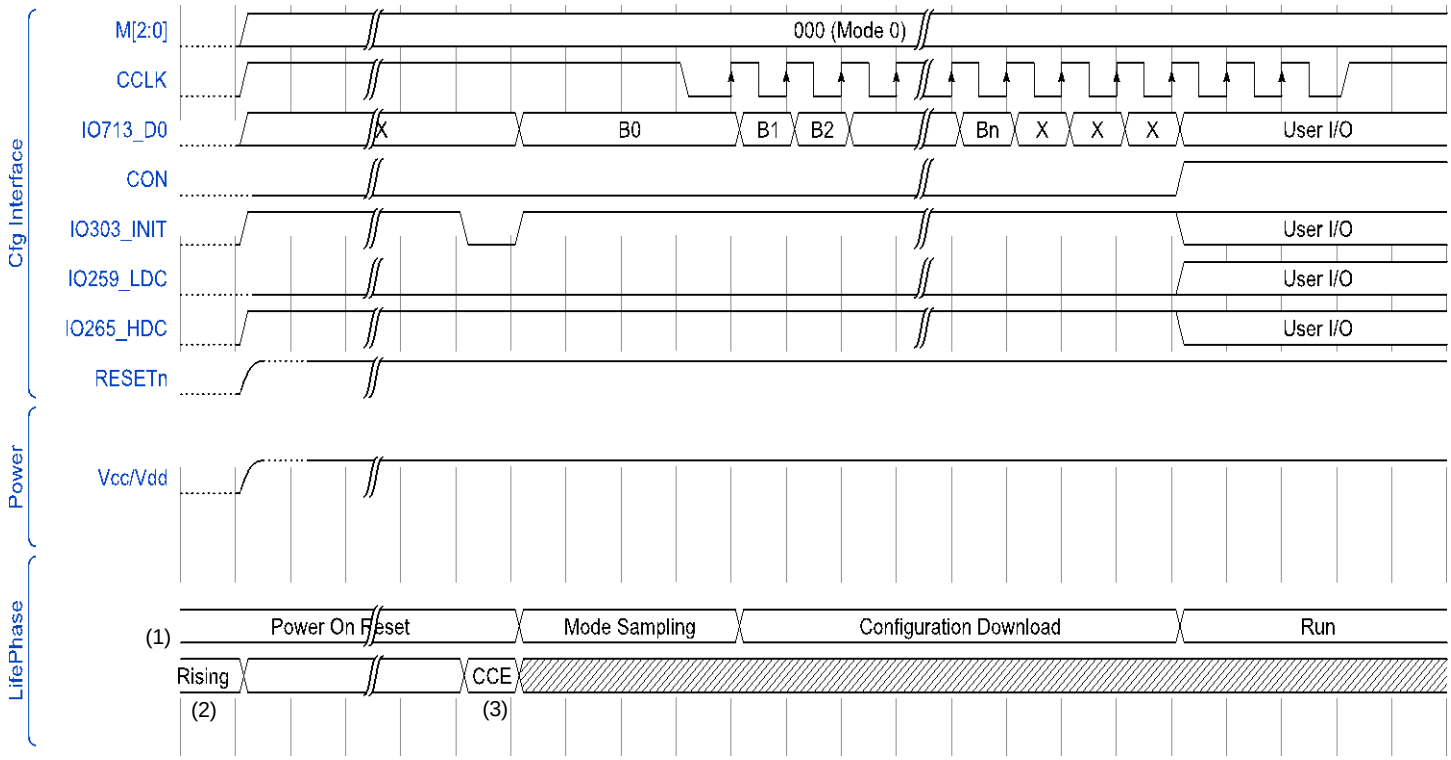
Figure 5-2. ATF280F automatic configuration download in mode 0



5.3.2 Configuration Download from Power-On Reset in mode 0

The chronogram described here after presents the sequence of ATF280F from a **Power-On Reset** until **Run**. This is the global overview of ATF280F automatic configuration download after a Power-On Reset.

Figure 5-3. ATF280F Configuration Download from Power-On Reset



Notes:
1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,
2. “Rising” means here the rising of power supplies line,
3. “CCE” means Clear Cycle End.

[**Power-On-Reset**]: During the Power-On Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. The end of this lifephase is marked by the rising edge of IO303_INIT pin:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up until the end of the Clear Cycle operation (CCE). At this time, IO303_INIT is driven to a low logic level during approximatively 1 us,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which has no effect during the Power-On Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.
- CCLK: this signal is internally pulled-up,

- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Configuration Download**]: During the Configuration Download lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces, this lifephase starts when CCLK pin is ouput:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is output as clock source for the serial EEPROM memory. At each rising edge of CCLK, the EEPROM memory outputs a new bit while the ATF280F senses the previous bit. By default, the CCLK frequency toggles at a frequency of approximatively 900 KHz.
- IO713_D0: this signal is sampled by the FPGA at each rising edge of CCLK. It is the DATA ouput of the EEPROM memory,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up and is used as an error monitoring pin. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

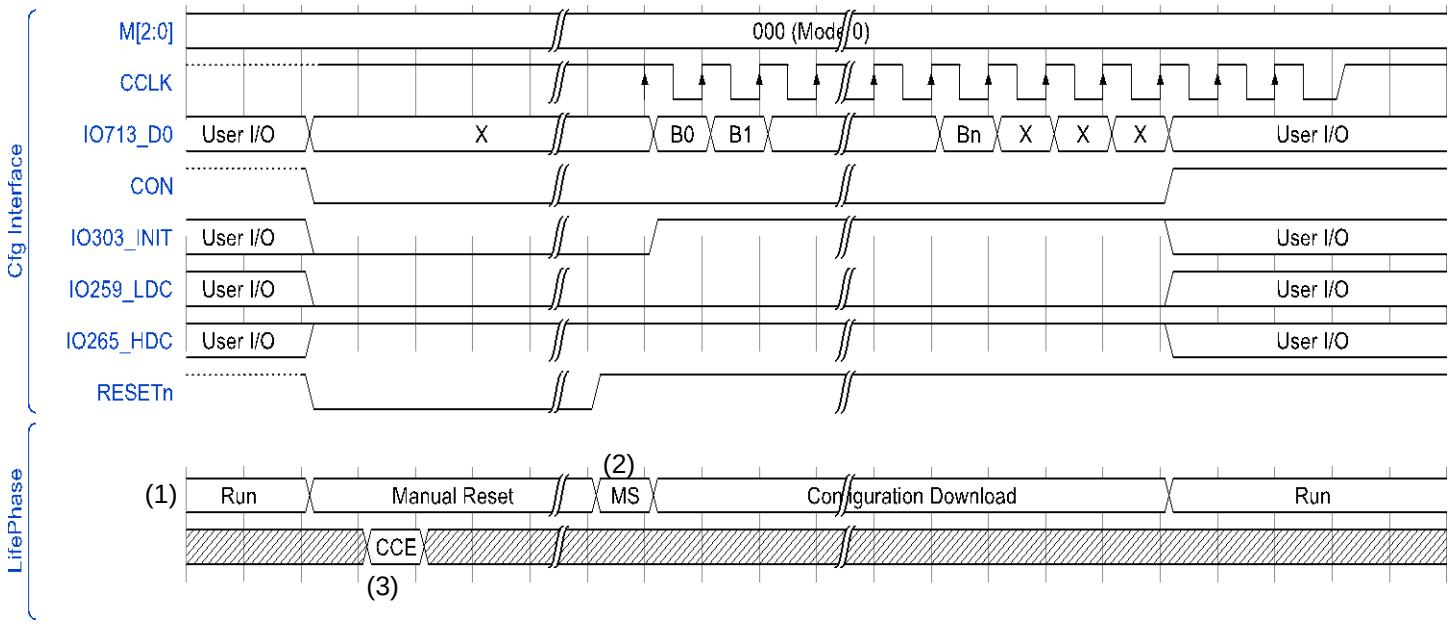
[**Run**]: Once configured, the ATF280F enters in Run lifephase. In this lifephase, the loaded application runs and its own lifephases are taken into account. This lifephase is entered few CCLK cycles after the ATF280F has sensed the postamble, it then releases the configuration interface signals and all multiplexed signals are set to their GPIO function:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input with pull-up and is not used anymore,
- IO713_D0: this signal becomes a User I/O and takes its application configuration,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal becomes a User I/O and takes its application configuration,
- IO259_LDC: this signal becomes a User I/O and takes its application configuration,
- IO265_HDC: this signal becomes a User I/O and takes its application configuration,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.3.3 Configuration Download from Manual Reset in mode 0

The chronogram described here after presents the sequence of ATF280F from a **Manual Reset** until **Run**. This is the global overview of ATF280F automatic configuration download after a Manual Reset.

Figure 5-4. ATF280F: Configuration Download from Manual Reset



Notes:
1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,
2. “MS” means ***Mode Sampling*** lifephase,
3. “CCE” means Clear Cycle End.

[**Manual Reset**]: During the Manual Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. This phase is entered when the RESETN pin is activated. The end of this lifephase is marked by the rising edge of IO303_INIT pin. During Manual Reset lifephase, the Clear Cycle operation (ended by CCE in the figure above) starts immediately and is performed in approximatively 2 ms. If the RESETN pin is activated during less than the 2 ms required for the Clear Cycle operation, the ATF280F remains in Manual Reset until CCE time:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is driven low until the RESETN pin is released,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which is active during Manual Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Configuration Download**]: During the Configuration Download lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces, this lifephase starts when CCLK pin is ouput:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is output as clock source for the serial EEPROM memory. At each rising edge of CCLK, the EEPROM memory outputs a new bit while the ATF280F senses the previous bit. By default, the CCLK frequency toggles at a frequency of approximatively 900 KHz.
- IO713_D0: this signal is sampled by the FPGA at each rising edge of CCLK. It is the DATA ouput of the EEPROM memory,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up and is used as an error monitoring pin Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

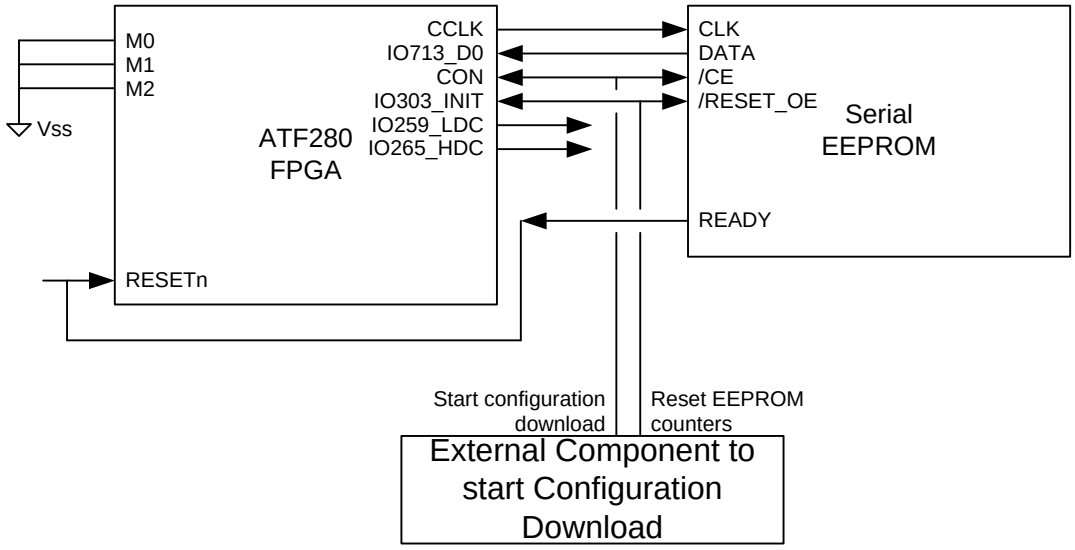
[**Run**]: Once configured, the ATF280F enters in Run lifephase. In this lifephase, the loaded application runs and its own lifephases are taken into account. This lifephase is entered few CCLK cycles after the ATF280F has sensed the postamble, it then releases the configuration interface signals and all multiplexed signals are set to their GPIO function:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input with pull-up and is not used anymore,
- IO713_D0: this signal becomes a User I/O and takes its application configuration,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal becomes a User I/O and takes its application configuration,
- IO259_LDC: this signal becomes a User I/O and takes its application configuration,
- IO265_HDC: this signal becomes a User I/O and takes its application configuration,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.3.4 Restart of Configuration Download in mode 0

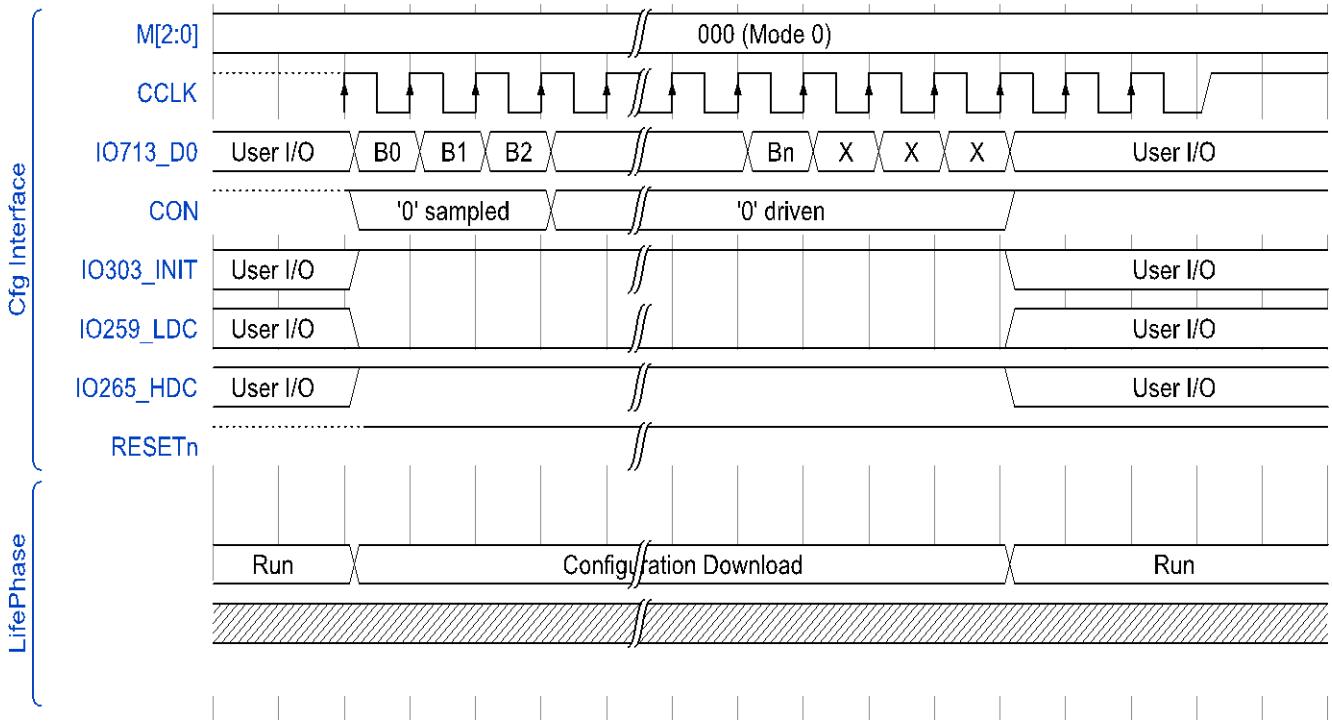
In mode 0, it is possible to restart the configuration download phase without proceding to a FPGA reboot (Power-On reset or Manual Reset). For this, it is required to use an external component in order to trig the start of the configuration download. The following synoptic shows the required signal to be used for restart of configuration download purpose in mode 0.

Figure 5-5. ATF280F restart configuration download in mode 0



The chronogram described here after presents the sequence of ATF280F from a **Run** until **Run**. This is the global overview of ATF280F restart of configuration download when in **Run**.

Figure 5-6. ATF280F: Restart of Configuration Download in mode 0



[**Run**]: In **Run** liefphase, the multiplexed pin of the ATF280F are in their GPIO function and as configured by the already loaded application. This lifephase is exiting to enter in **Configuration Download** as soon as the CON pin is driven to a low logic level by an external master:

- M0, M1, M2: these signals remain inputs and are not used anymore (Mode is already sampled),
- CCLK: this signal is an input with pull-up and is not used,
- IO713_D0: this signal remains a User I/O,
- CON: this signal is released to a high logic level by the ATF280F itself,
- IO303_INIT: this signal remains a User I/O,
- IO259_LDC: this signal remains a User I/O,
- IO265_HDC: this signal remains a User I/O,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Configuration Download**]: During the Configuration Download lifephase, the ATF280F starts to drive the signal regarding configuration download interfaces, this lifephase starts when CON is lowered by an external master component:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is output as clock source for the serial EEPROM memory. At each rising edge of CCLK, the EEPROM memory outputs a new bit while the ATF280F senses the previous bit. By default, the CCLK frequency toggles at a frequency of approximatively 900 KHz.
- IO713_D0: this signal is sampled by the FPGA at each rising edge of CCLK. It is the DATA ouput of the EEPROM memory,
- CON: this signal shall be first maintained to a low logic level by an external master component. The configuration download starts immediately and CCLK is directly output. Once the ATF280F has sampled the CON pin to low during three CCLK periods, it starts to drive the CON pin to a low logic level. Then the external master component shall release the CON signal,
- IO303_INIT: this signal is internally pulled-up and is used as an error monitoring pin. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Run**]: Once configured, the ATF280F enters in Run lifephase. In this lifephase, the loaded application runs and its own lifephases are taken into account. This lifephase is entered few CCLK cycles after the ATF280F has sensed the postamble, it then releases the configuration interface signals and all multiplexed signals are set to their GPIO function:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input with pull-up and is not used anymore,
- IO713_D0: this signal becomes a User I/O and takes its application configuration,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal becomes a User I/O and takes its application configuration,
- IO259_LDC: this signal becomes a User I/O and takes its application configuration,
- IO265_HDC: this signal becomes a User I/O and takes its application configuration,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4 Slave Modes

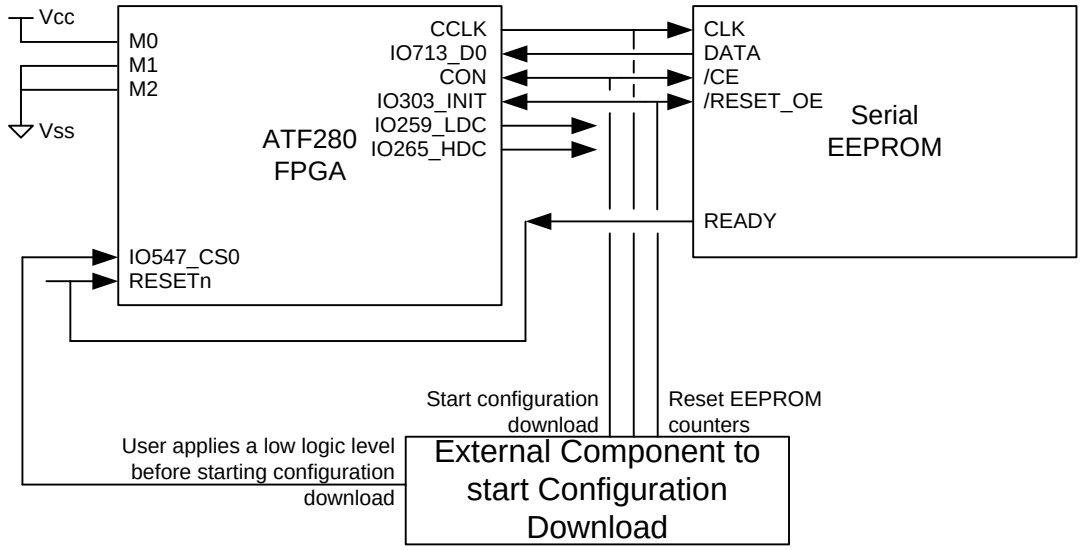
Slave Modes In slave modes, configuration is always initiated by an external signal. Data is applied to the device on the rising edge of CCLK. In Slave Serial Mode, the device receives serial configuration data. In Slave Parallel Mode, the device receives either 8-bit wide or 16-bit wide parallel data. In Slave Parallel Up Mode, the device receives either 8-bit or 16-bit wide parallel data and generates a 20-bit address up counter for use in addressing memories. CCLK is not generated in slave modes.

5.4.1 Mode 1

The mode 1 is one of the Slave Serial Mode configuration download. In this mode, the ATF280F is coupled to a serial EEPROM and shall be externally driven for configuration download purpose. The following synoptic shows the required interface to be used for configuration download purpose in mode 1.

Caution: Same mode than mode 7 but with the need of the chip select (CS0 signal).

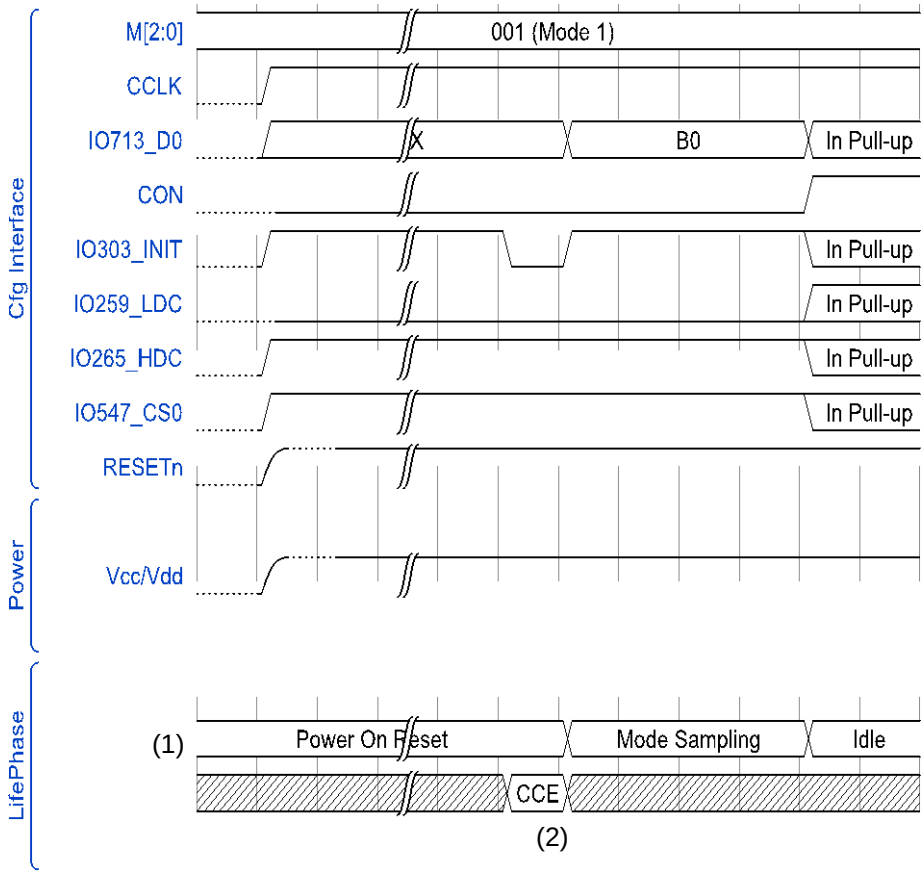
Figure 5-7. ATF280 FPGA environment : configuration download in mode 1



5.4.1.2 Power-On Reset in mode 1

The chronogram described here after presents the sequence of ATF280F from a **Power-On Reset** until **Idle**. This is the global overview of ATF280F Power-On Reset sequence. At the end of this sequence, the ATF280F remains unconfigured and is ready for configuration download in slave mode.

Figure 5-8. ATF280F Power-On Reset in mode 1



Notes: 1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,

2. "CCE" means Clear Cycle End.

[**Power-On-Reset**]: During the Power-On Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. The end of this lifephase is marked by the rising edge of IO303_INIT pin:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up until the end of the Clear Cycle operation (CCE). At this time, IO303_INIT is driven to a low logic level during approximatively 1 us,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- IO547_CS0: this signal is internally pulled-up,
- RESETN: this signal is an input which has no effect during the Power-On Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- IO547_CS0: this signal is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

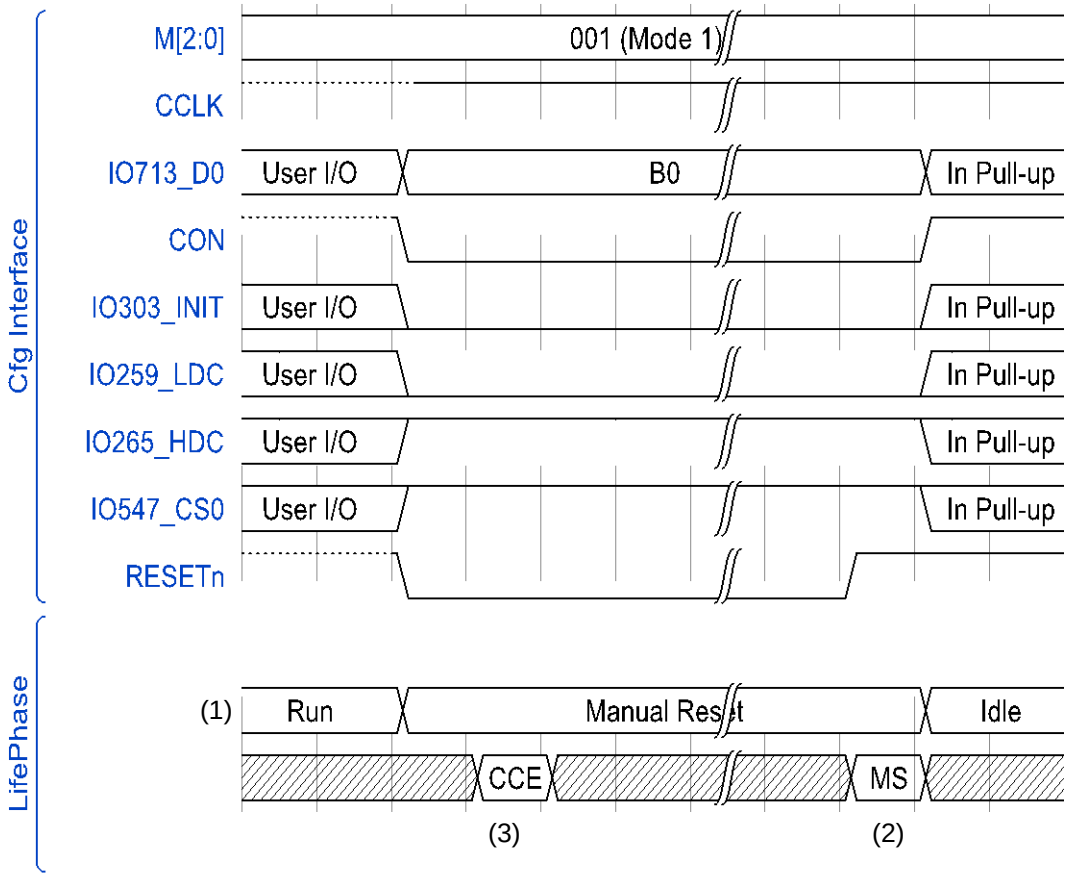
[**Idle**]: During the Idle lifephase, the ATF280F continues releases the configuration download interface, this lifephase starts when CON and IO303_INIT pins are released:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes its GPIO function and is internally pulled-up,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal takes its GPIO function and is internally pulled-up. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: this signal takes its GPIO function and is internally pulled-up,
- IO265_HDC: this signal takes its GPIO function and is internally pulled-up,
- IO547_CS0: this signal takes its GPIO function and is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.1.3 Manual Reset in mode 1

The chronogram described here after presents the sequence of ATF280F from a **Manual Reset** until **Idle**. This is the global overview of ATF280F Manual Reset sequence. At the end of this sequence, the ATF280F remains unconfigured and is ready for configuration download in slave mode.

Figure 5-9. ATF280F: Manual Reset in mode 1



Notes:
1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,
2. “MS” means ***Mode Sampling*** lifephase,
3. “CCE” means Clear Cycle End.

[**Manual Reset**]: During the Manual Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. This phase is entered when the RESETN pin is activated. The end of this lifephase is marked by the rising edge of IO303_INIT pin. During Manual Reset lifephase, the Clear Cycle operation (ended by CCE in the figure above) starts immediately and is performed in approximatively 2 ms. If the RESETN pin is activated during less than the 2 ms required for the Clear Cycle operation, the ATF280F remains in Manual Reset until CCE time:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,

- IO303_INIT: this signal is driven low until the RESETN pin is released,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- IO547_CS0: this signal is internally pulled-up,
- RESETN: this signal is an input which is active during Manual Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- IO547_CS0: this signal is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

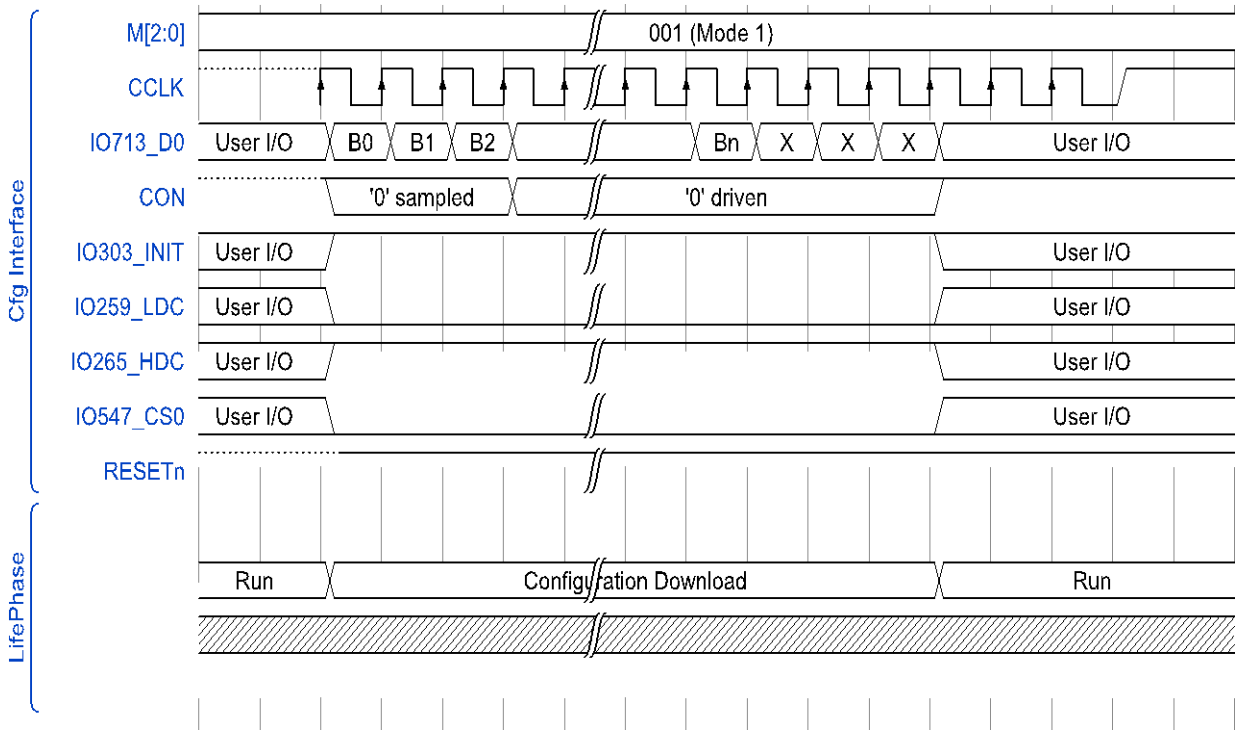
[**Idle**]: During the Idle lifephase, the ATF280F continues releases the configuration download interface, this lifephase starts when CON and IO303_INIT pins are released:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes its GPIO function and is internally pulled-up,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal takes its GPIO function and is internally pulled-up. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: this signal takes its GPIO function and is internally pulled-up,
- IO265_HDC: this signal takes its GPIO function and is internally pulled-up,
- IO547_CS0: this signal takes its GPIO function and is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.1.4 Configuration Download in mode 1

The chronogram described here after presents the sequence of ATF280F from **Run** or **Idle** until **Run**. This is the global overview of ATF280F Configuration Download sequence in mode 1. At the end of this sequence, the ATF280F is configured and the loaded application runs.

Figure 5-10. ATF280F: Configuration Download in mode 1



[**Run**]: In **Run** lifephase, the multiplexed pin of the ATF280F are in their GPIO function and as configured by the already loaded application. This lifephase is exiting to enter in **Configuration Download** as soon as the CON pin is driven to a low logic level by an external master:

- M0, M1, M2: these signals remain inputs and are not used anymore (Mode is already sampled),
- CCLK: this signal is an input with pull-up and is not used,
- IO713_D0: this signal remains a User I/O,
- CON: this signal is released to a high logic level by the ATF280F itself,
- IO303_INIT: this signal remains a User I/O,
- IO259_LDC: this signal remains a User I/O,
- IO265_HDC: this signal remains a User I/O,
- IO547_CS0: this signal remains a User I/O,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Configuration Download**]: During the Configuration Download lifephase, the ATF280F starts to drive the signal regarding configuration download interfaces, this lifephase starts when CON is lowered by an external master component:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input and shall be provided by the external master component as clock source for the serial EEPROM memory and the ATF280F. At each rising edge of CCLK, the EEPROM memory outputs a new bit while the ATF280F senses the previous bit.
- IO713_D0: this signal is sampled by the FPGA at each rising edge of CCLK. It is the DATA ouput of the EEPROM memory,

- CON: this signal shall be first maintained to a low logic level by an external master component. The configuration download starts immediately and CCLK is directly output. Once the ATF280F has sampled the CON pin to low during three CCLK periods, it starts to drive the CON pin to a low logic level. Then the external master component shall release the CON signal,
- IO303_INIT: this signal is internally pulled-up and is used as an error monitoring pin. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- IO547_CS0: this signal shall be driven low during the whole configuration download lifephase,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Run**]: Once configured, the ATF280F enters in Run lifephase. In this lifephase, the loaded application runs and its own lifephases are taken into account. This lifephase is entered few CCLK cycles after the ATF280F has sensed the postamble, it then releases the configuration interface signals and all multiplexed signals are set to their GPIO function:

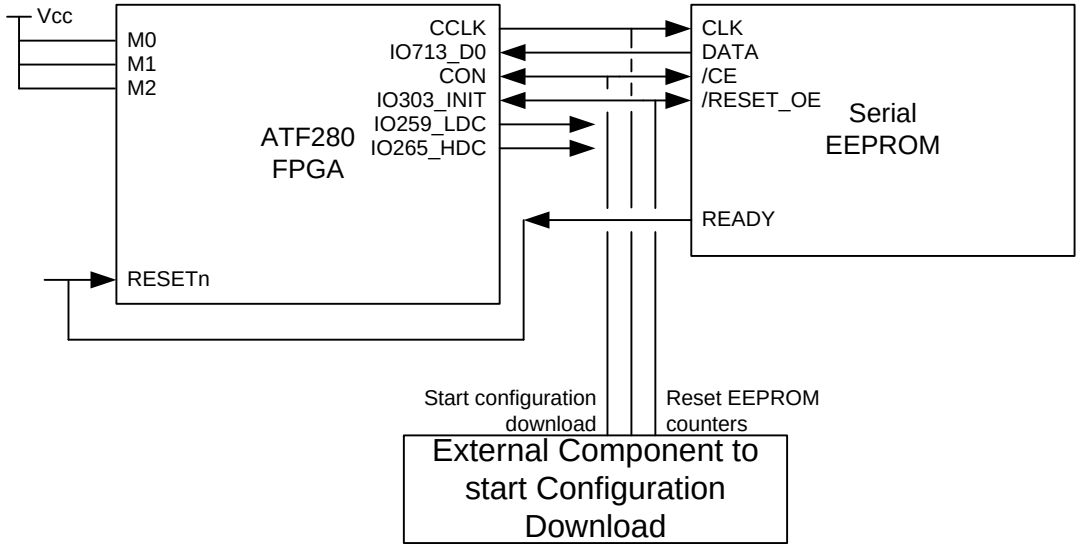
- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input with pull-up and is not used anymore,
- IO713_D0: this signal becomes a User I/O and takes its application configuration,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal becomes a User I/O and takes its application configuration,
- IO259_LDC: this signal becomes a User I/O and takes its application configuration,
- IO265_HDC: this signal becomes a User I/O and takes its application configuration,
- IO547_CS0: this signal becomes a User I/O and takes its application configuration,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.2 Mode 7

The mode 7 is one of the Slave Serial Mode configuration download. In this mode, the ATF280F is coupled to a serial EEPROM and shall be externally driven for configuration download purpose. The following synoptic shows the required signal to be used for configuration download purpose in mode 7.

Caution: Same mode than mode 1 but without the need of the chip select (CS0 signal).

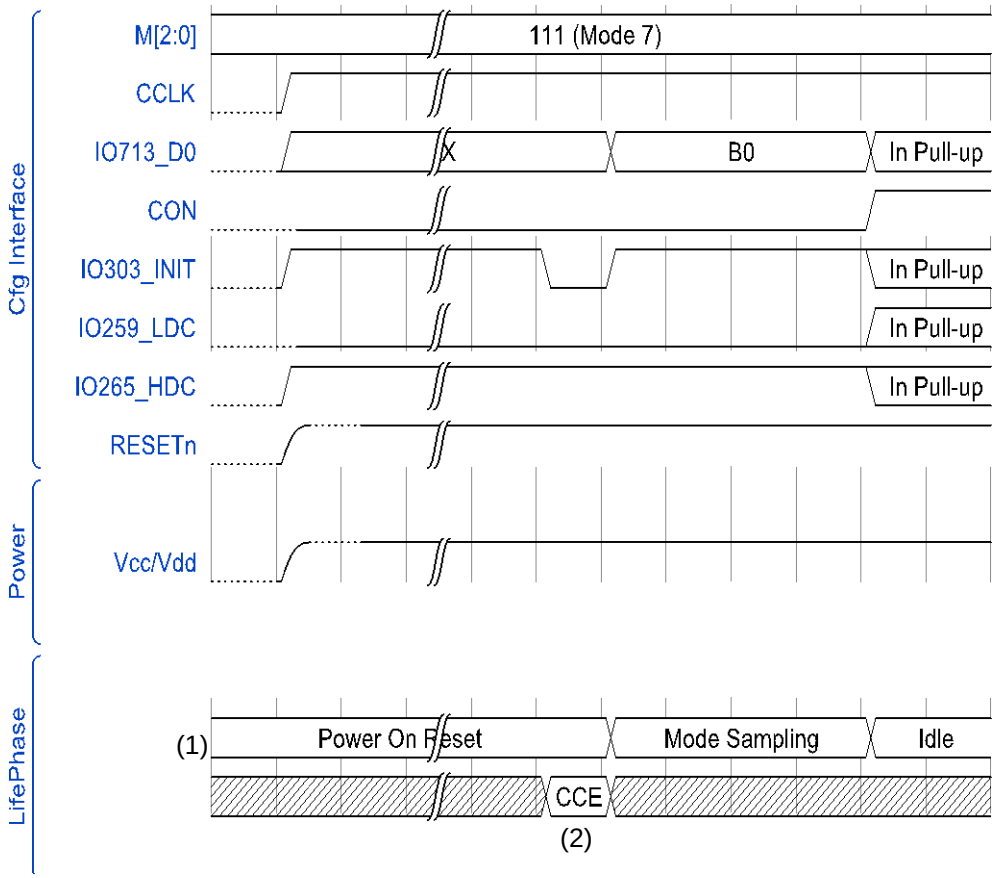
Figure 5-11. ATF280 FPGA environment : configuration download in mode 7



5.4.2.2 Power-On Reset in mode 7

The chronogram described here after presents the sequence of ATF280F from a **Power-On Reset** until **Idle**. This is the global overview of ATF280F Power-On Reset sequence. At the end of this sequence, the ATF280F remains unconfigured and is ready for configuration download in slave mode.

Figure 5-12. ATF280F Power-On Reset in mode 7



Notes: 1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,

2. "CCE" means Clear Cycle End.

[**Power-On-Reset**]: During the Power-On Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. The end of this lifephase is marked by the rising edge of IO303_INIT pin:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up until the end of the Clear Cycle operation (CCE). At this time, IO303_INIT is driven to a low logic level during approximatively 1 us,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which has no effect during the Power-On Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.

- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

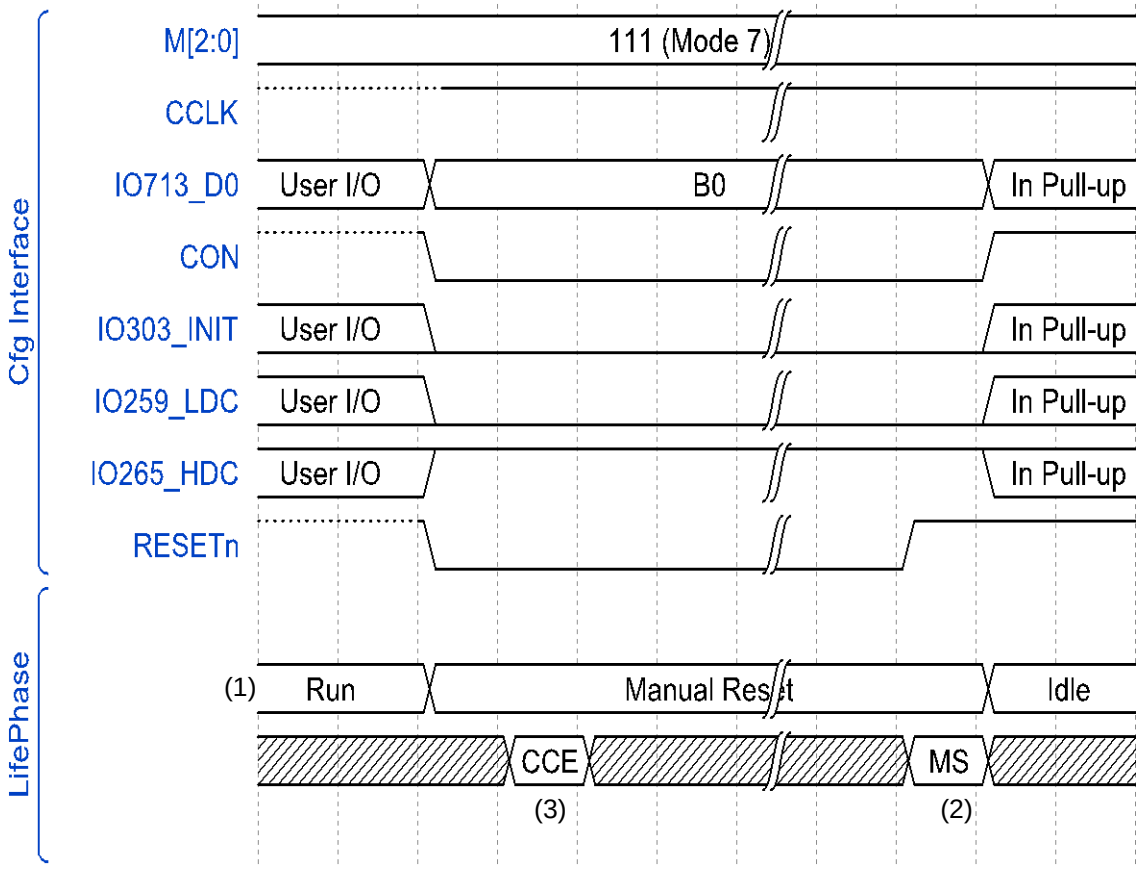
[**Idle**]: During the Idle lifephase, the ATF280F continues releases the configuration download interface, this lifephase starts when CON and IO303_INIT pins are released:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes its GPIO function and is internally pulled-up,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal takes its GPIO function and is internally pulled-up. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: this signal takes its GPIO function and is internally pulled-up,
- IO265_HDC: this signal takes its GPIO function and is internally pulled-up,
- IO547_CS0: this signal takes its GPIO function and is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.2.3 Manual Reset in mode 7

The chronogram described here after presents the sequence of ATF280F from a **Manual Reset** until **Idle**. This is the global overview of ATF280F Manual Reset sequence. At the end of this sequence, the ATF280F remains unconfigured and is ready for configuration download in slave mode.

Figure 5-13. ATF280F: Manual Reset in mode 7



Notes:
1. This line shows the different lifephase viewable in life cycle diagram described in **OperatingModes / Lifephases** section,
2. “MS” means ***Mode Sampling*** lifephase,
3. “CCE” means Clear Cycle End.

[**Manual Reset**]: During the Manual Reset lifephase, the ATF280F starts to drive the signal regarding the configuration download interfaces as defined below. This phase is entered when the RESETN pin is activated. The end of this lifephase is marked by the rising edge of IO303_INIT pin. During Manual Reset lifephase, the Clear Cycle operation (ended by CCE in the figure above) starts immediately and is performed in approximatively 2 ms. If the RESETN pin is activated during less than the 2 ms required for the Clear Cycle operation, the ATF280F remains in Manual Reset until CCE time:

- M0, M1, M2: these signals are inputs and not used,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal is internally pulled-up,
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is driven low until the RESETN pin is released,

- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which is active during Manual Reset lifephase.

[**Mode Sampling**]: During the Mode Sampling lifephase, the ATF280F continues to drive the signal regarding configuration download interfaces. In addition, Mode Pins (M0, M1, M2) are sensed:

- M0, M1, M2: these signals are inputs and sensed to determine the used mode. If mode 0 is sampled (as shown in the figure above), the automatic configuration download starts.
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes the value ouput by the EEPROM (first bit of the EEPROM),
- CON: this signal is driven to a low logic level,
- IO303_INIT: this signal is internally pulled-up,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

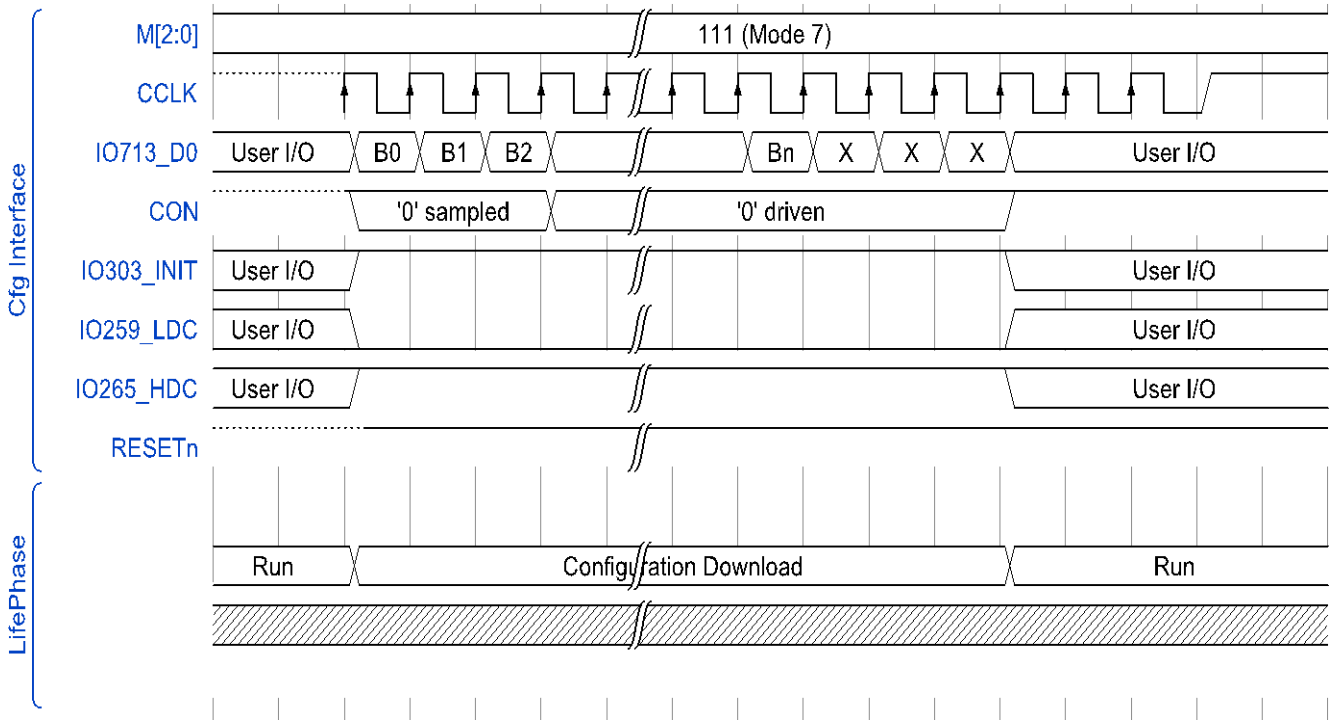
[**Idle**]: During the Idle lifephase, the ATF280F continues releases the configuration download interface, this lifephase starts when CON and IO303_INIT pins are released:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is internally pulled-up,
- IO713_D0: this signal takes its GPIO function and is internally pulled-up,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal takes its GPIO function and is internally pulled-up. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: this signal takes its GPIO function and is internally pulled-up,
- IO265_HDC: this signal takes its GPIO function and is internally pulled-up,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.2.4 Configuration Download in mode 7

The chronogram described here after presents the sequence of ATF280F from **Run** or **Idle** until **Run**. This is the global overview of ATF280F Configuration Download sequence in mode 1. At the end of this sequence, the ATF280F is configured and the loaded application runs.

Figure 5-14. ATF280F: Configuration Download in mode 7



[**Run**]: In **Run** lifephase, the multiplexed pin of the ATF280F are in their GPIO function and as configured by the already loaded application. This lifephase is exiting to enter in **Configuration Download** as soon as the CON pin is driven to a low logic level by an external master:

- M0, M1, M2: these signals remain inputs and are not used anymore (Mode is already sampled),
- CCLK: this signal is an input with pull-up and is not used,
- IO713_D0: this signal remains a User I/O,
- CON: this signal is released to a high logic level by the ATF280F itself,
- IO303_INIT: this signal remains a User I/O,
- IO259_LDC: this signal remains a User I/O,
- IO265_HDC: this signal remains a User I/O,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Configuration Download**]: During the Configuration Download lifephase, the ATF280F starts to drive the signal regarding configuration download interfaces, this lifephase starts when CON is lowered by an external master component:

- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input and shall be provided by the external master component as clock source for the serial EEPROM memory and the ATF280F. At each rising edge of CCLK, the EEPROM memory outputs a new bit while the ATF280F senses the previous bit.

- IO713_D0: this signal is sampled by the FPGA at each rising edge of CCLK. It is the DATA ouput of the EEPROM memory,
- CON: this signal shall be first maintained to a low logic level by an external master component. The configuration download starts immediately and CCLK is directly output. Once the ATF280F has sampled the CON pin to low during three CCLK periods, it starts to drive the CON pin to a low logic level. Then the external master component shall release the CON signal,
- IO303_INIT: this signal is internally pulled-up and is used as an error monitoring pin. Refer to **Data Link Protection** section for serial configuration,
- IO259_LDC: the Low During Configuration is driven to a low logic level,
- IO265_HDC: the High During Configuration is driven to a high logic level,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

[**Run**]: Once configured, the ATF280F enters in Run lifephase. In this lifephase, the loaded application runs and its own lifephases are taken into account. This lifephase is entered few CCLK cycles after the ATF280F has sensed the postamble, it then releases the configuration interface signals and all multiplexed signals are set to their GPIO function:

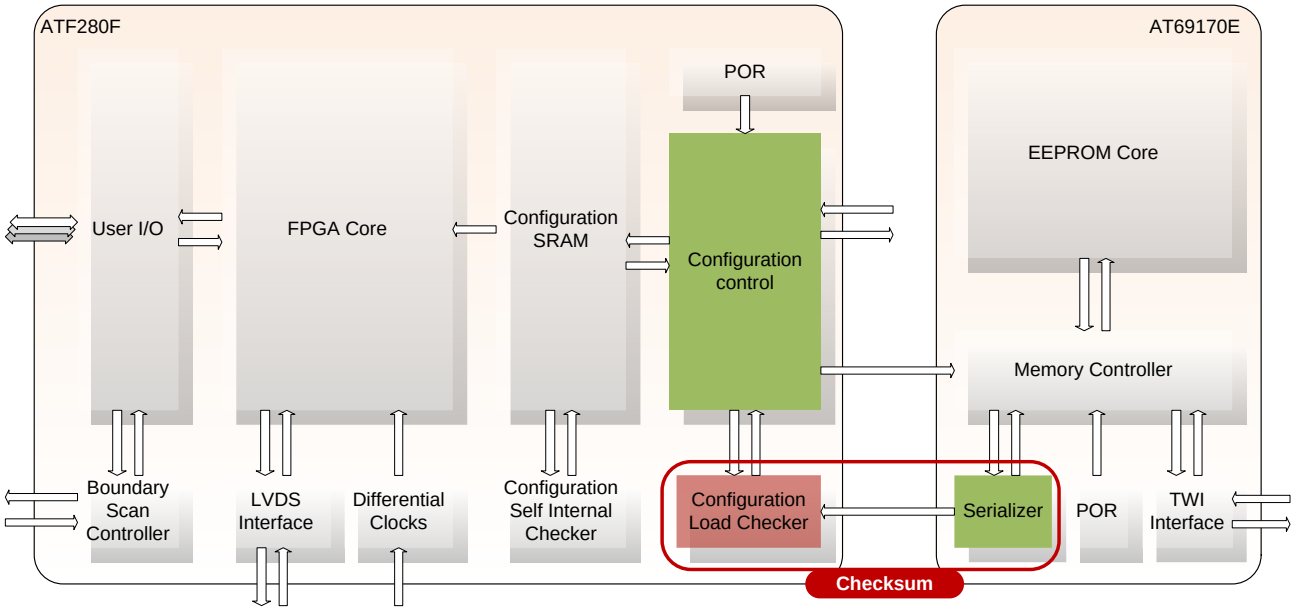
- M0, M1, M2: these signals remain inputs and are not used anymore,
- CCLK: this signal is an input with pull-up and is not used anymore,
- IO713_D0: this signal becomes a User I/O and takes its application configuration,
- CON: this signal is released to a high logic level,
- IO303_INIT: this signal becomes a User I/O and takes its application configuration,
- IO259_LDC: this signal becomes a User I/O and takes its application configuration,
- IO265_HDC: this signal becomes a User I/O and takes its application configuration,
- RESETN: this signal is an input which immediately reset the configuration logic to a Manual Reset lifephase.

5.4.3 Data Link Protection

The ATF280F is capable to secure the mechanism involved during the configuration download in order to prevent wrong configuration of the FPGA.

The following schematic represents an overview of the system made by the FPGA and a serial EEPROM memory. The highlighted modules show where the protection of the configuration download link takes place.

Figure 5-15. ATF280F Configuration Download Link



Two kinds of errors are managed during the configuration:

- Low Level Errors

  Such protection is used to warranty that the communication protocol on the FPGA serial communication link is correctly handled all along the configuration process. In addition, the low level error management ensures that no erroneous access to the FPGA configuration SRAM will be attempted.

  When detected, the low level results in “Aborting Download”. This means that all the steps from a configuration download are not performed. The consequence is that the bitstream is partially loaded and can result in an unoperating FPGA,

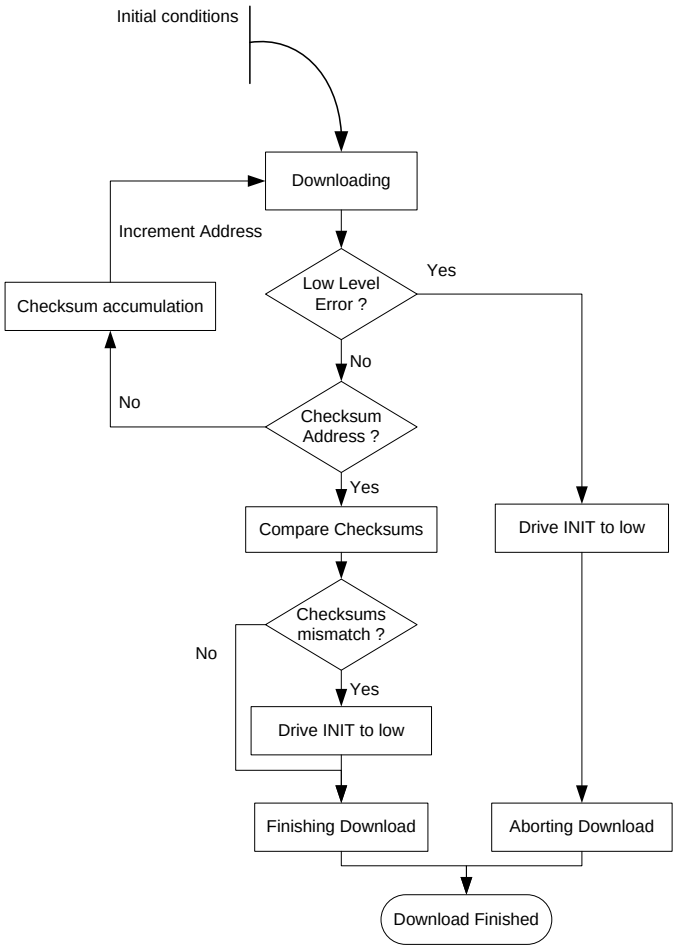
- Checksum Errors

  This protection is used at the end of the configuration download to verify that there were no corruptions of the data stream during the transfer.

  When detected, the checksum error results in “Finishing download”. This means that all the steps from a nominal configuration download are executed until entering in ***Run*** lifephase.

The error detection mechanism follows the flow chart presented here after.

Figure 5-16. Management of configuration download link protection



5.4.3.2 Low level Errors management

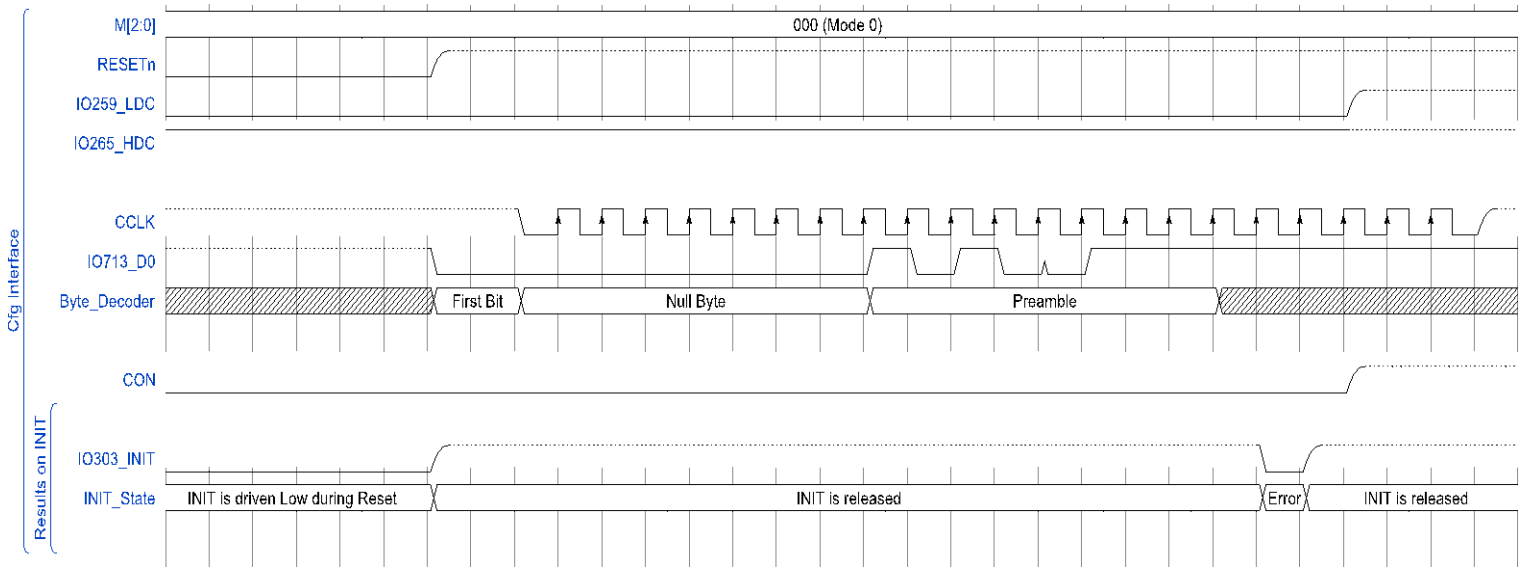
These errors have the highest priority and terminate by a configuration download abort. They are managed in the same way whatever is the used serial mode (Mode 0, 1 or 7).

The low level errors are detected in case of bad values regarding the following elements:

- “Preamble” mismatch → different from “10110111”
- “Start Address” mismatch → if the start address of a window is corrupted,
- “Stop Address” mismatch → if the stop address of a window is corrupted,
- “Postamble” mismatch →different from “11100111”.

In case of low level error, INIT is driven low during one CCLK clock period few clock cycles after the byte in default. Then, INIT is released and CON is released. The configuration download is so finished.

Figure 5-17. ATF280F - Preamble mismatch behavior in mode 0



5.4.3.3 Checksum Errors management

During the generation of an application bitstream, a checksum is computed with a specific algorithm by IDS tool and stored in the bitstream checksum zone. This checksum is the reference for checksum error management.

All along the configuration download, the “configuration load checker” calculates on-the-fly a checksum byte by accumulating all effective data of the downloaded bitstream with a hardcoded algorithm.

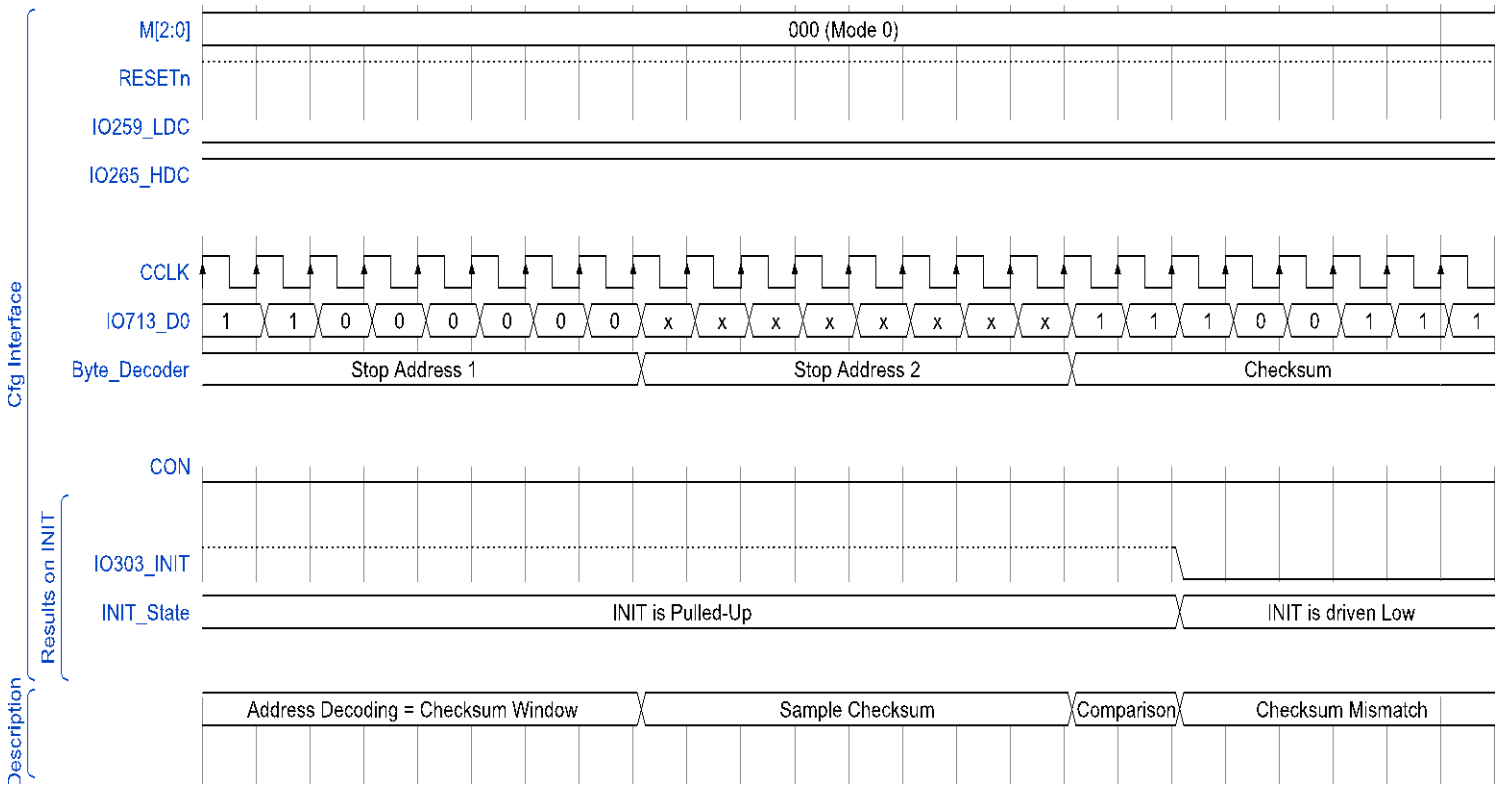
Once the FPGA configuration reaches the checksum zone, it compares the reference downloaded checksum together with the checksum accumulated during the configuration download. In case of mismatched values, INIT is driven low to notify that errors occur during the download procedure.

All data loaded in the FPGA configuration SRAM will be taken into account by the FPGA parts.

On ATF280F, the checksum window is addressed as follow and is one byte sized:

- Start Address: Byte0 = 0x00000000, Byte 1 = 0x00000000, Byte 2 = 0x11000000,
- Stop Address: Byte0 = 0x00000000, Byte 1 = 0x00000000, Byte 2 = 0x11000000

Figure 5-18. ATF280F - Checksum error behavior in mode 0



5.5 Parallel Configuration

5.5.1 Bitstream Structure

5.5.2 Slave Modes

In slave modes, configuration is always initiated by an external signal. Data is applied to the device on the rising edge of CCLK. In Slave Serial Mode, the device receives serial configuration data. In Slave Parallel Mode, the device receives either 8-bit wide or 16-bit wide parallel data. In Slave Parallel Up Mode, the device receives either 8-bit or 16-bit wide parallel data and generates a 20-bit address up counter for use in addressing memories. CCLK is not generated in slave modes.

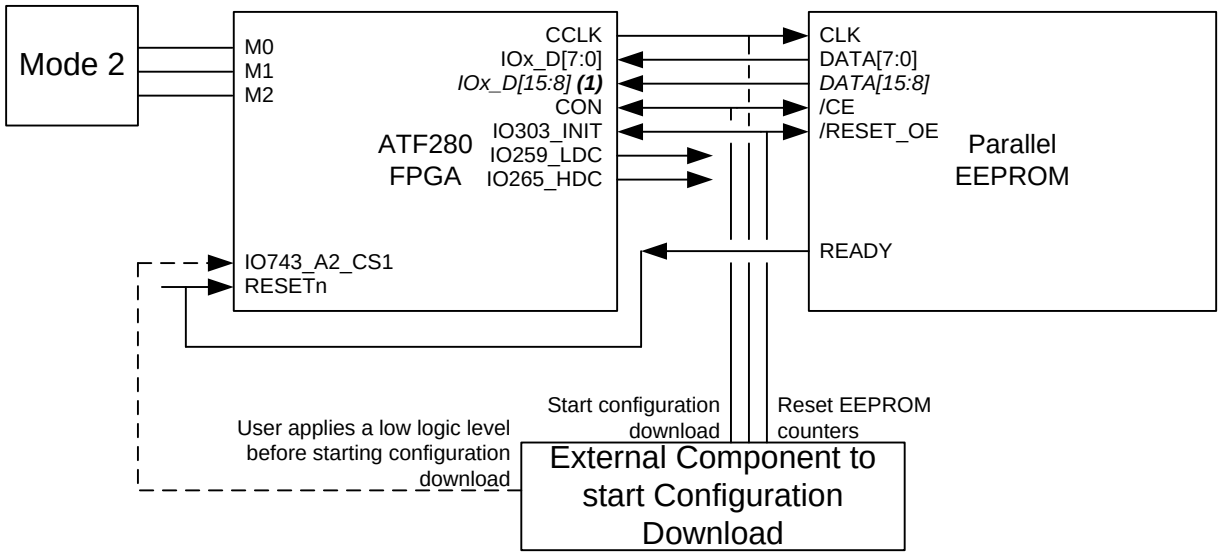
5.5.2.1 Mode 2

Warning:

The section below is for parallalel mode 2. This description is preliminary and will be more precise in next version.

The mode 2 is one of the Slave Parallel Mode configuration download. In this mode, the ATF280F is coupled to a parallel EEPROM (or equivalent) and shall be externally driven for configuration download purpose. The following synoptic shows the required interface to be used for configuration download purpose in mode 2.

Figure 5-19. ATF280 FPGA environment : configuration download in mode 2



Notes: 1. In parallel modes, ATF280F is capable to be accessed through a 16 bits wide data bus. Refer to **Register** section for configuration.

In Mode 2, CCLK is driven by an external device. On the rising edge of each CCLK, parallel data is clocked into the FPGA. To begin configuration, CON and the chip select (IO743_A2_CS1 pin) must be driven Low. Once the bitstream is completed, CON is released, indicating the device is completely ready for user operation.

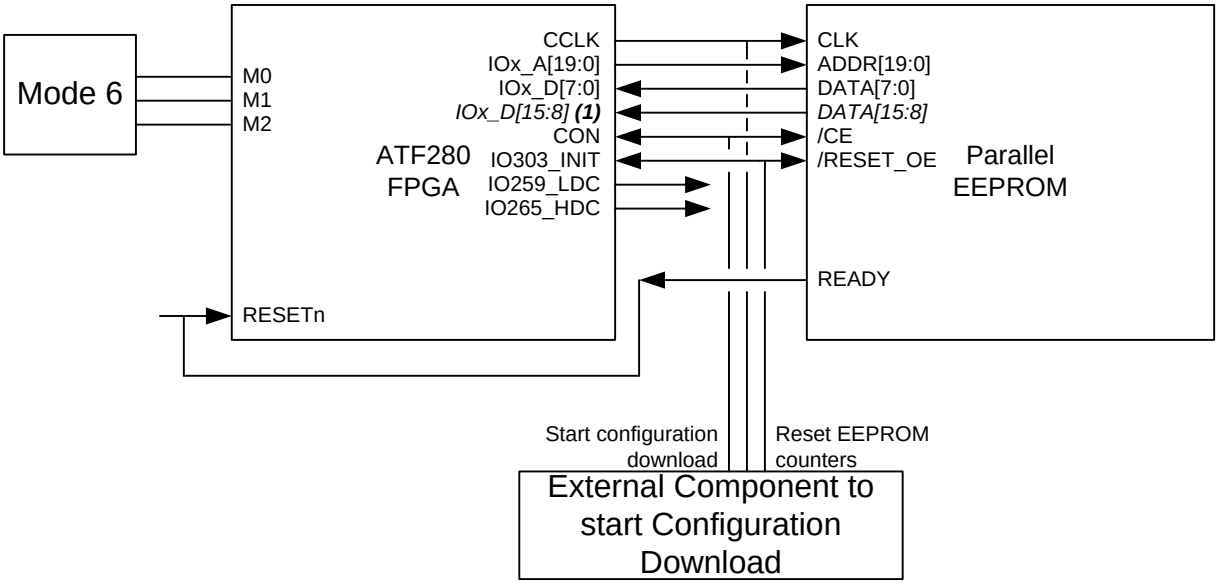
5.5.2.2 Mode 6

Warning:

The section below is for parallalel mode 6. This description is preliminary and will be more precise in next version.

The mode 6 is one of the Slave Parallel Mode configuration download. In this mode, the ATF280F is coupled to a parallel EEPROM (or equivalent) and shall be externally driven for configuration download purpose. The following synoptic shows the required interface to be used for configuration download purpose in mode 6.

Figure 5-20. ATF280 FPGA environment : configuration download in mode 6



Notes: 1. In parallel modes, ATF280F is capable to be accessed through a 16 bits wide data bus. Refer to **Register** section for configuration.

A Mode 6 Slave Parallel Up device is usually configured in a system whereby data comes from a parallel external memory, such as a PROM. Figure 18 shows a typical system application. In Mode 6, CCLK is driven by an external device. On the rising edge of each CCLK, an address is supplied by the FPGA to an external memory, and parallel data is clocked into the FPGA. To begin configuration, CON is driven Low. There is no chip select for Mode 6, since it is always configured as the most upstream device in a cascade chain. Once the bitstream is completed, CON is released by the FPGA, indicating the device is completely ready for user operation.

5.5.3 Data Link Protection

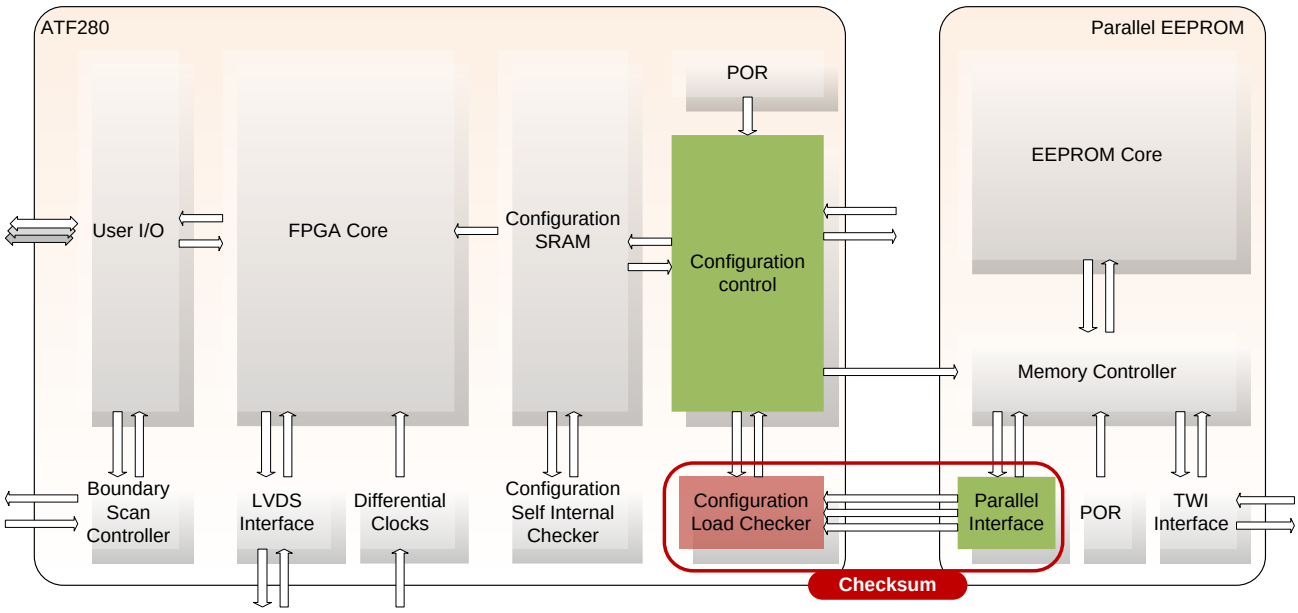
Warning:

The section below is about data link protection for parallel modes (2 and 6). This description is preliminary and will be more precise in next version

The ATF280F is capable to secure the mechanism involved during the configuration download in order to prevent wrong configuration of the FPGA.

The following schematic represents an overview of the system made by the FPGA and a parallalel EEPROM memory. The highlighted modules show where the protection of the configuration download link takes place.

Figure 5-21. ATF280F Configuration Download Link



Two kinds of errors are managed during the configuration:

- Low Level Errors

  Such protection is used to warranty that the communication protocol on the FPGA serial communication link is correctly handled all along the configuration process. In addition, the low level error management ensures that no erroneous access to the FPGA configuration SRAM will be attempted.

  When detected, the low level results in “Aborting Download”. This means that all the steps from a configuration download are not performed. The consequence is that the bitstream is partially loaded and can result in an unoperating FPGA,

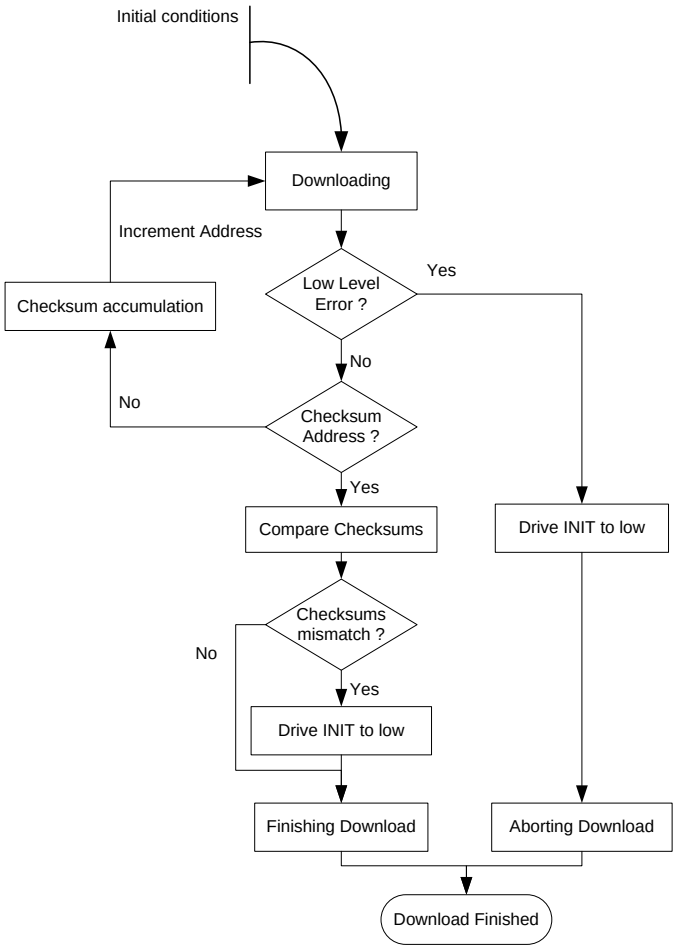
- Checksum Errors

  This protection is used at the end of the configuration download to verify that there were no corruptions of the data stream during the transfer.

  When detected, the checksum error results in “Finishing download”. This means that all the steps from a nominal configuration download are executed until entering in ***Run*** lifephase.

The error detection mechanism follows the flow chart presented here after.

Figure 5-22. Management of configuration download link protection



5.5.3.2 Low level Errors management

These errors have the highest priority and terminate by a configuration download abort. They are managed in the same way whatever is the used parallalel mode (Mode 2 or 6).

The low level errors are detected in case of bad values regarding the following elements:

- “Preamble” mismatch → different from “10110111”
- “Start Address” mismatch → if the start address of a window is corrupted,
- “Stop Address” mismatch → if the stop address of a window is corrupted,
- “Postamble” mismatch →different from “11100111”.

In case of low level error, INIT is driven low during one CCLK clock period few clock cycles after the byte in default. Then, INIT is released and CON is released. The configuration download is so finished.

5.5.3.3 Checksum Errors management

During the generation of an application bitstream, a checksum is computed with a specific algorithm by IDS tool and stored in the bitstream checksum zone. This checksum is the reference for checksum error management.

All along the configuration download, the “configuration load checker” calculates on-the-fly a checksum byte by accumulating all effective data of the downloaded bitstream with a hardcoded algorithm.

Once the FPGA configuration reaches the checksum zone, it compares the reference downloaded checksum together with the checksum accumulated during the configuration download. In case of mismatched values, INIT is driven low to notify that errors occur during the download procedure.

All data loaded in the FPGA configuration SRAM will be taken into account by the FPGA parts.

On ATF280F, the checksum window is addressed as follow and is one byte sized:

- Start Address: Byte0 = 0x00000000, Byte 1 = 0x00000000, Byte 2 = 0x11000000,
- Stop Address: Byte0 = 0x00000000, Byte 1 = 0x00000000, Byte 2 = 0x11000000

6. Configuration Integrity Management

While the download of the bit-stream from the EEPROM (or configuration master) to the FPGA is checked through communication link protection, the ATF280F also provides the features for verification of the configuration once the FPGA configuration is finished. Two services are provided to manage the integrity of the configuration.

6.1 Check function

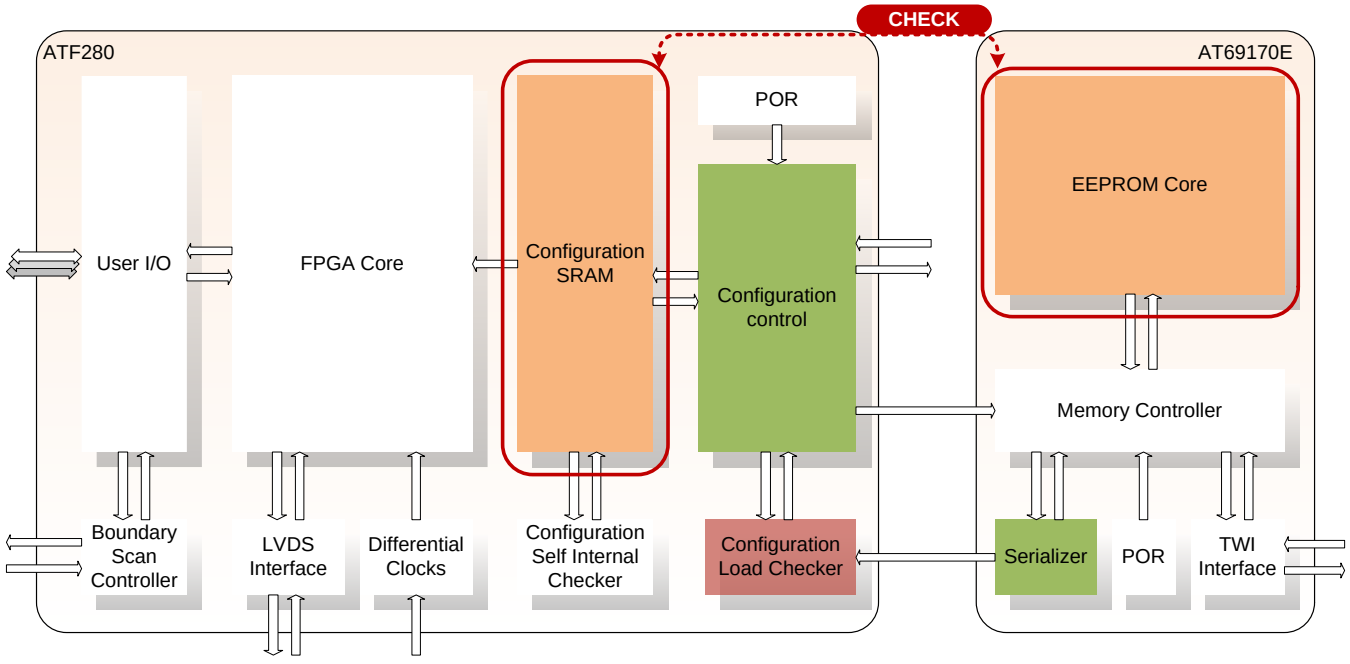
The ATF280F, through the configuration logic embeds a feature called CHECK function. This feature, if activated, is useable at any time when the FPGA is in **Run** phase. It provides a strong mechanism to ensure that loaded data are the same than the EEPROM source one.

6.1.1 Description

The following schematic represents an overview of the system made by the FPGA and a serial EEPROM memory. The highlighted modules show where the CHECK function takes place:

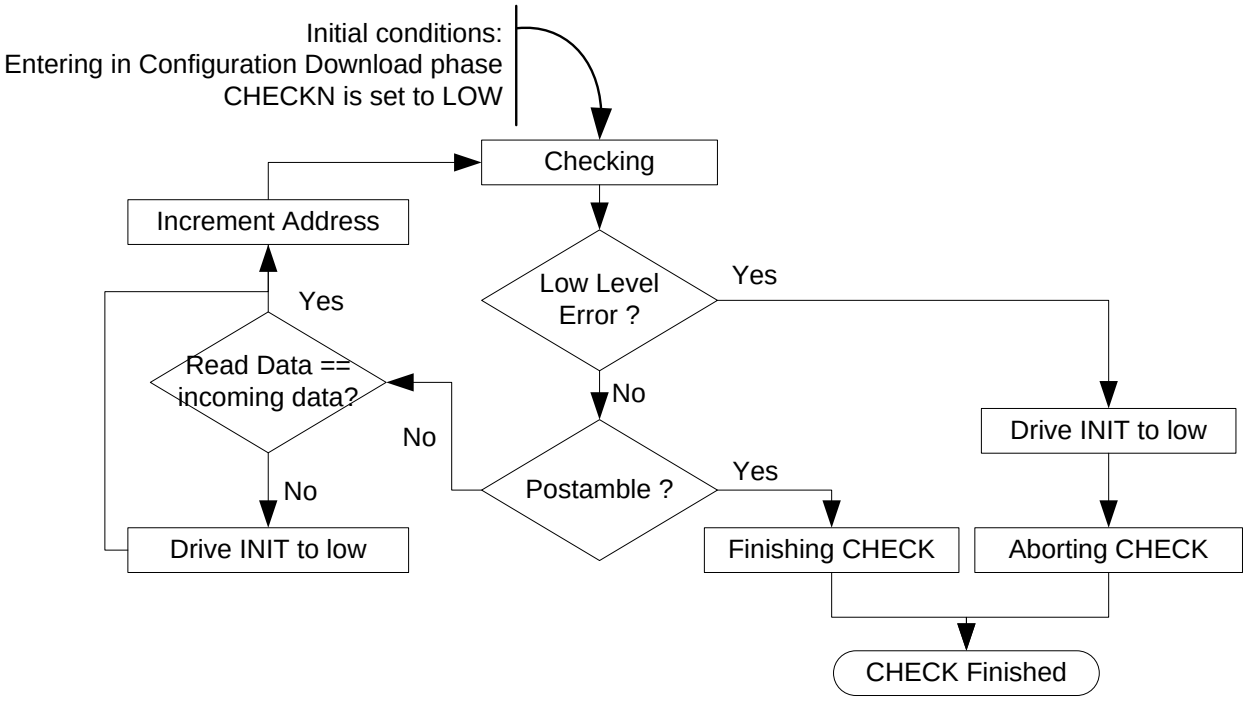
- The FGPA could be either in Mode 0, 1 or 7 for serial mode and in Mode 2 or 6 for parallel mode,
- The EEPROM has a serial interface for serial mode and a parallel interface for parallel mode,
- The EEPROM interface is compliant with the interface required by the ATF280F,
- The result of CHECK function reflets any differences between Configuration SRAM of ATF280F and EEPROM memory content.

Figure 6-1. ATF280F: CHECK function overview



The CHECK function obeys to the following workflow:

Figure 6-2. ATF280F CHECK function workflow



To verify the data, the ATF280F uses the CHECK function in parallel to a configuration download. The use of CHECK function is optional and can be bypassed by the user (Refer to Register Chapter for more details).

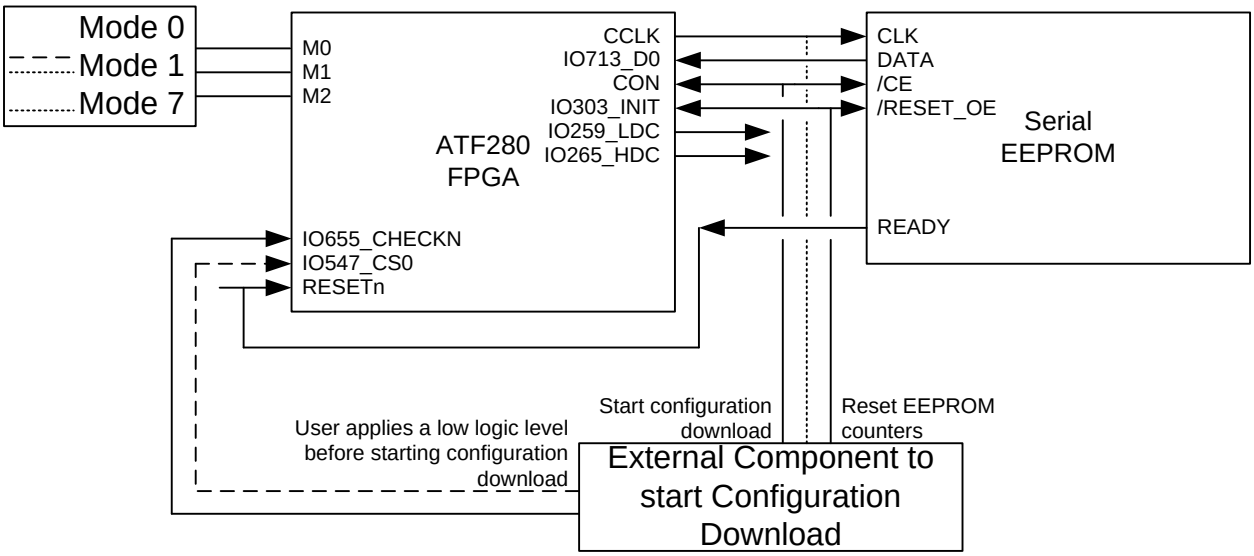
The differences between a nominal configuration download and a CHECK function is described below:

- When performing a configuration download, the “configuration control” module addresses the SRAM point and writes them as defined in the EEPROM bitstream,
- When performing a CHECK function, the “configuration control” module addresses the SRAM point, read them and compare their content to the value defined in the EEPROM bitstream,
- The “configuration load checker” module manages the protocol errors (low level errors) in the same way than for a configuration download, but checksums are not taken into account.

The following synoptics shows the required interface of ATF280F for the use of CHECK function in serial and parallel modes. For each of these cases, the required interface is strictly the same than the one required for the configuration download but with the use of IO655_CHECKN pin.

6.1.2 Serial Modes

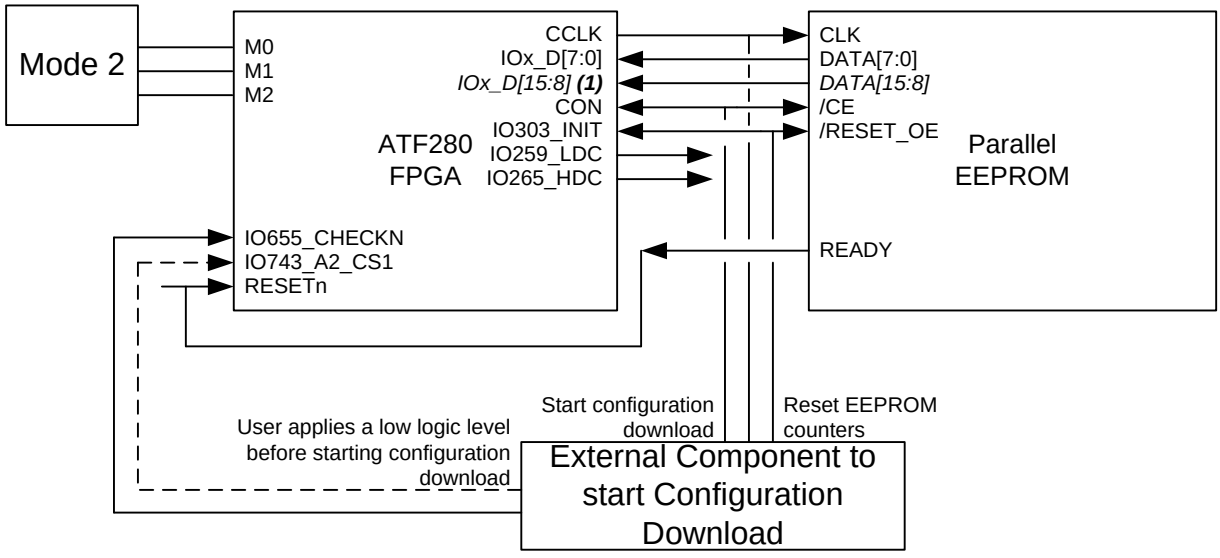
Figure 6-3. CHECK function in serial modes



Caution: In serial mode, the required interface for CHECK function is the same than for configuration download. It means that for Mode 1, the IO547_CS0 shall be used in parallel to the IO655_CHECKN pin when starting the configuration download (dotted line in figure above).

6.1.3 Parallel Modes

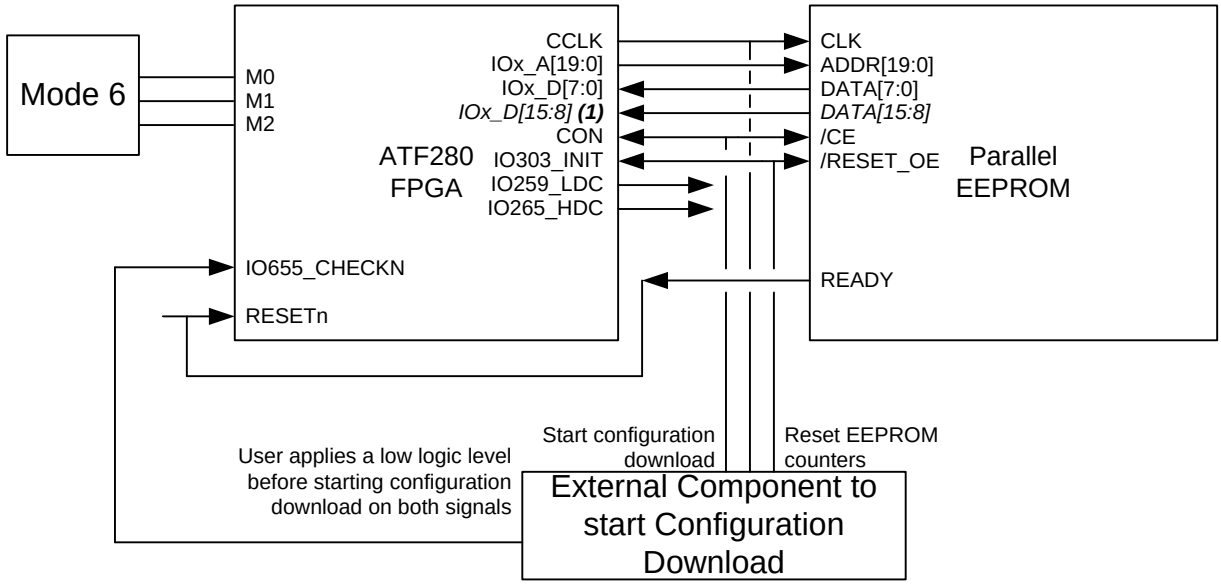
Figure 6-4. CHECK function in parallel mode 2



Notes: 1. In parallel modes, ATF280F is capable to be accessed through a 16 bits wide data bus. Refer to **Register** section for configuration.

Caution: In parallel mode, the required interface for CHECK function is the same than for configuration download. It means that for Mode 2, the IO743_A2_CS1 shall be used in parallel to the IO655_CHECKN pin when starting the configuration download (dotted line in figure above).

Figure 6-5. CHECK function in parallel mode 6



Notes: 1. In parallel modes, ATF280F is capable to be accessed through a 16 bits wide data bus. Refer to **Register** section for configuration.

Caution: In parallel mode, the required interface for CHECK function is the same than for configuration download. It means that for Mode 6, the IO743_A2_CS1 is used in the output address bus IOx_A[19:0]. The pin IO655_CHECKN pin shall be used when starting the configuration download.

6.1.4 Behavior

The use of CHECK function is done by launching in **Run** lifephase a configuration download while IO655_CHECKN pin is externally driven to a low logic level.

Figure 6-6. ATF280F CHECK function without error

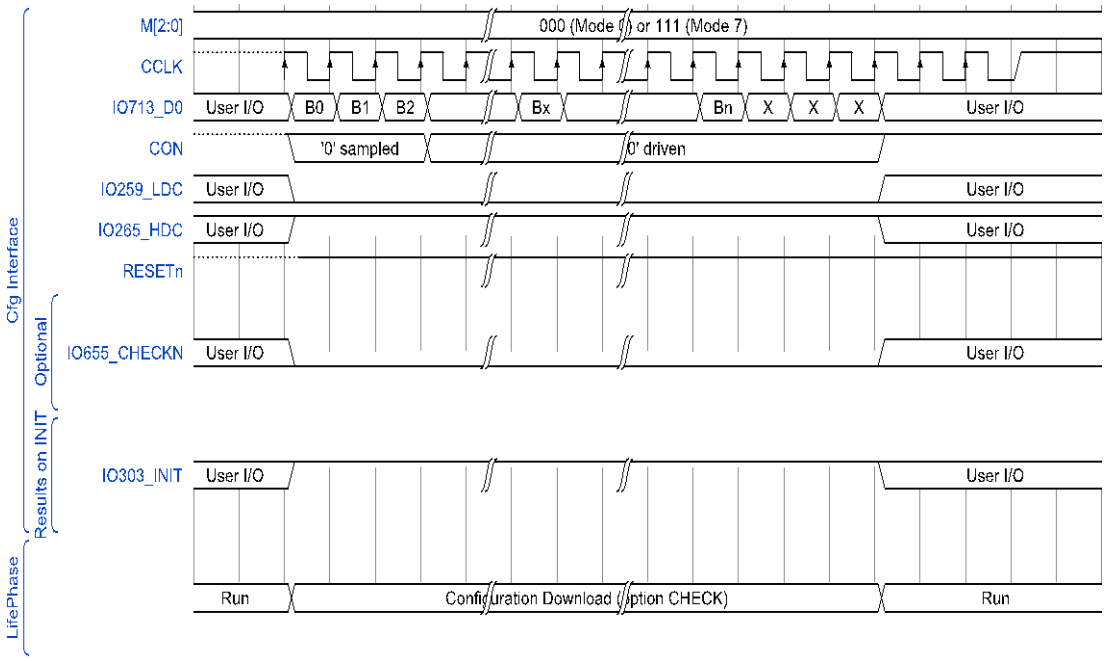
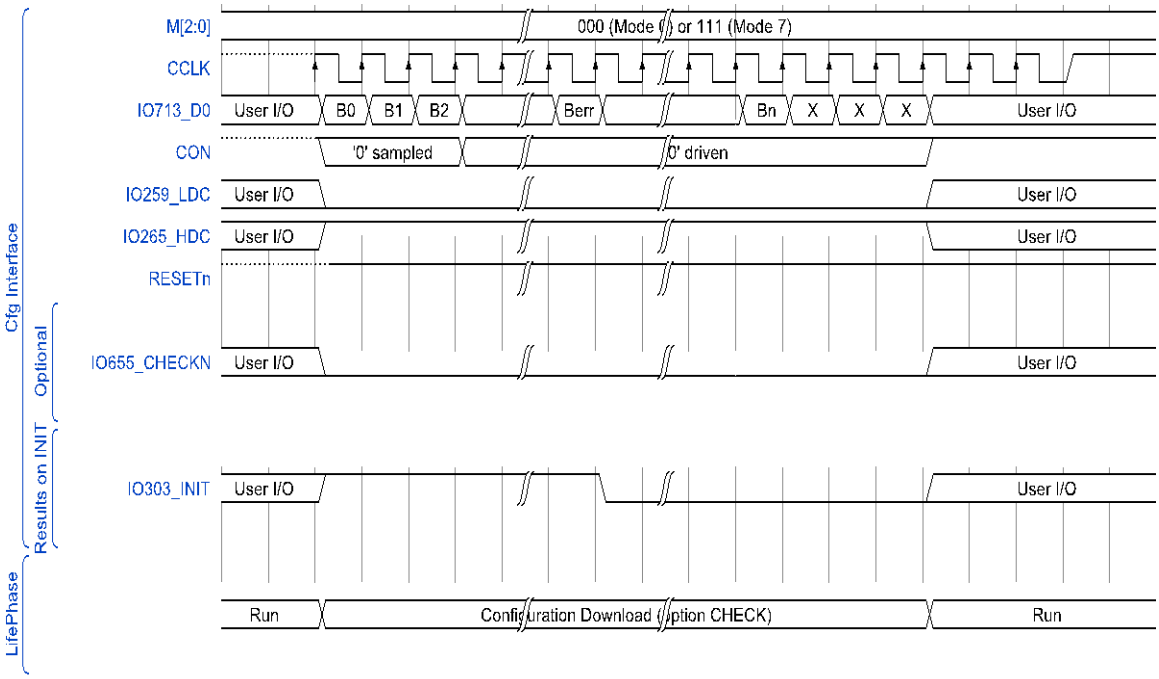


Figure 6-7. ATF280F CHECK function with error



Caution: It shall be noticed that in case of error detected during a CHECK function, two kinds of errors are possible:

- Low Level Error: the error that are protocol relevant and which bring the IO303_INIT to be driven low after some CCLK periods,
- CHECK comparison mismatch: the signature is a drive to low of the IO303_INIT two CCLK periods after the byte in default.

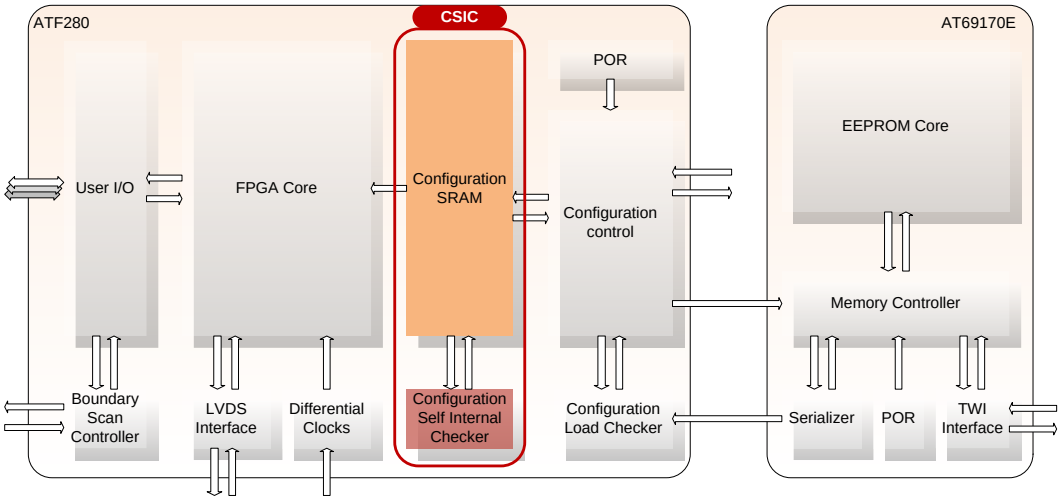
6.2 Self Integrity Checker function

The ATF280F, through the configuration logic embeds a feature called CSIC (for Configuration Self Integrity Checker). This feature, if activated, is useable in **Run** phase. It provides a strong mechanism to ensure the retention of the loaded data.

6.2.1 Description

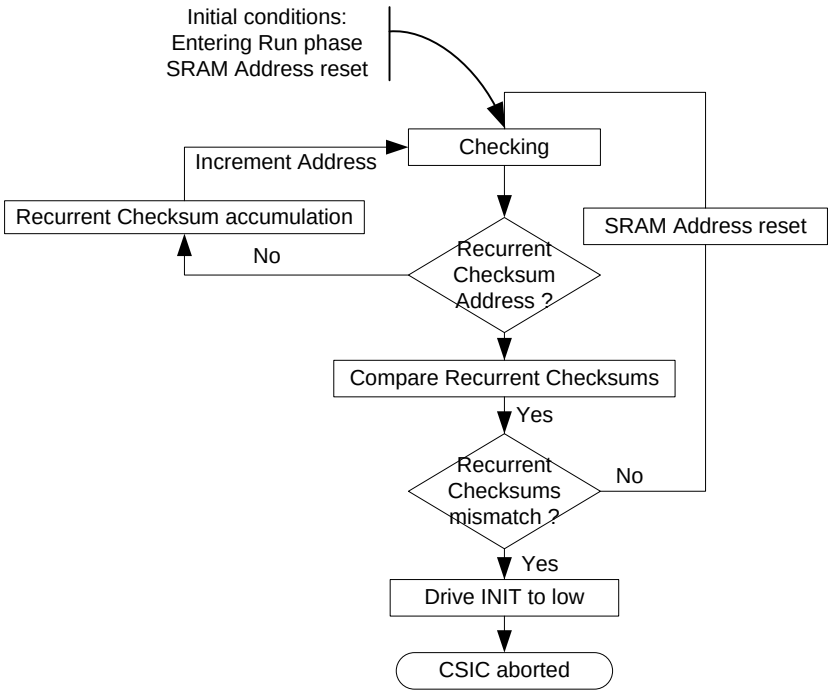
The following schematic represents an overview of the modules involved in the CSIC function:

Figure 6-8. ATF280F CSIC Overview



The CSIC function obeys to the following workflow:

Figure 6-9. ATF280F CSIC workflow



The following points described how the CSIC function could be used and how it works:

- The CSIC function is not mode dependent and is activated with the bit CR8 of the configuration register (Refer to Register Chapter for more details),
- The bitstream will contain a window called “Recurrent Checksum” with a stored byte calculated by the IDS Software during the bitstream generation,
- The ATF280F will calculate cyclically by the used of loaded data the value of this Recurrent Checksum and will compare the result with the one stored in the “Recurrent Checksum” window,
- In mode 0 (the only master mode), the CSIC function requires the activation of the bit CR13 of the configuration register (Refer to Register Chapter for more details). The continuous CCLK option is mandatory to clock the CSIC function,

Caution: CCLK will toggle during all the time of the Run phase.

- In all other modes (1, 7, 2 and 6), the CCLK shall be provided continuously after the configuration download by an external clock source. This continuous CCLK input is mandatory to clock the CSIC function,

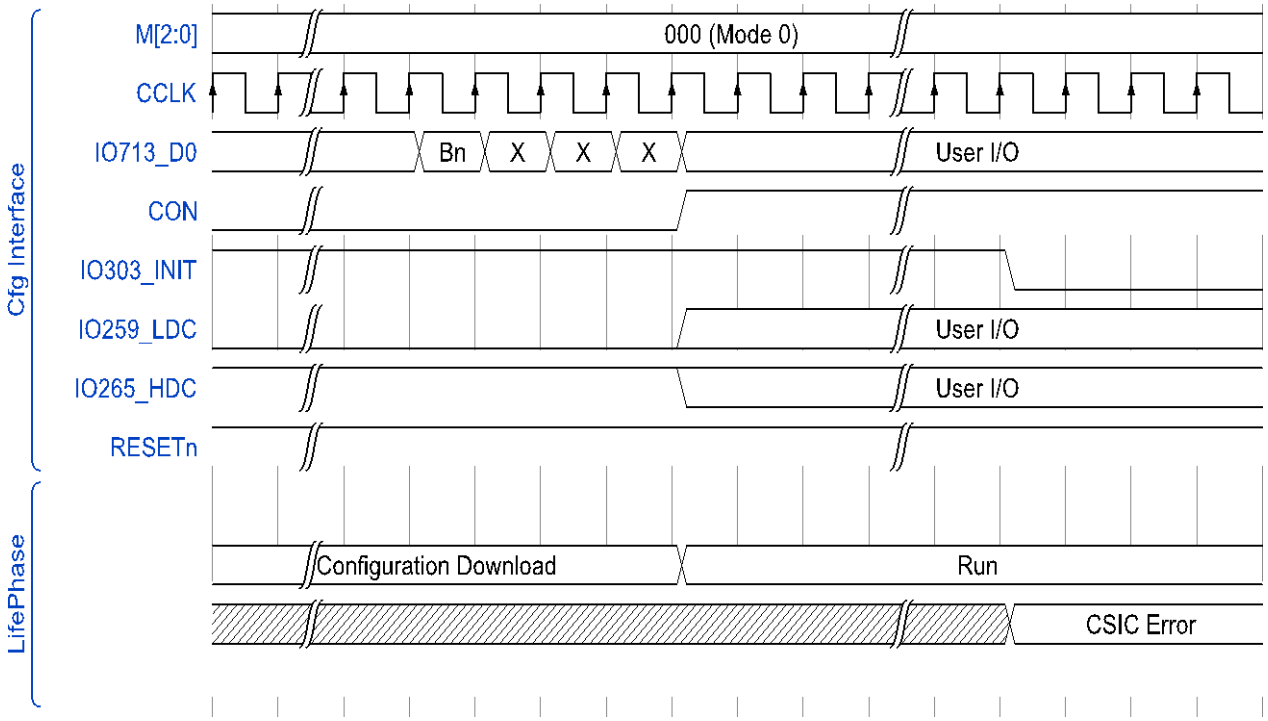
Caution: CCLK shall not be stop during all the time of the Run phase.

- When CSIC function is used, the IO303_INIT pin remains in [CFG] function and is released to a high logic level while no error is detected. If a bit flips, it will bring the calculated recurrent checksum to be different from the stored recurrent checksum. The result will be a drive to low logic level of the IO303_INIT until a Power-On Reset or a Manual Reset and the bitstream will continue to work.

Caution: IO303_INIT will remain in [CFG] function during all the time of Run phase and shall be taken into account at system level.

6.2.2 Behavior

Figure 6-10. CSIC function behavior on error

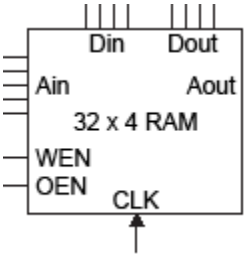


7. FreeRam™

The ATF280F offers 115Kbits of dual-port RAM called FreeRAM™. The FreeRAM™ is made of 32 x 4 dual-ported RAM blocks and dispersed throughout the array as shown in the figure hereafter. This FreeRAM™ is SEU and SET hardened.

A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows. A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows. A 5-bit Input Address Bus connects to five vertical express buses in same column. A 5-bit Output Address Bus connects to five vertical express buses in same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port.

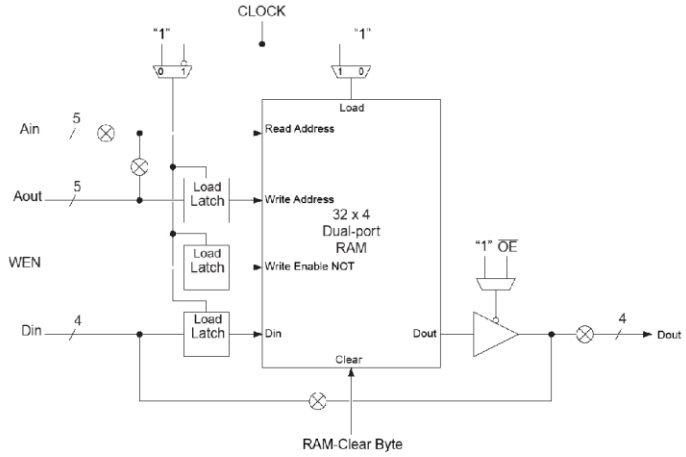
Figure 7-1. FreeRam™ Block Interface



Reading and writing of the 10ns 32 x 4 dual-port FreeRAM™ are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches on Write Address, Write Enable and Data In are transparent:

- when load is logic 1, data flows through
- when load is logic 0, data is latched.

Figure 7-2. RAM logic - Detailed



The latches are used to synchronize Write Address, Write Enable Not, and Din signals for a synchronous RAM.

Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble is (Write) addressed and LOAD is logic 1 and WE is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or WE is logic 1, data is latched in the nibble.

The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select “1” (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block.

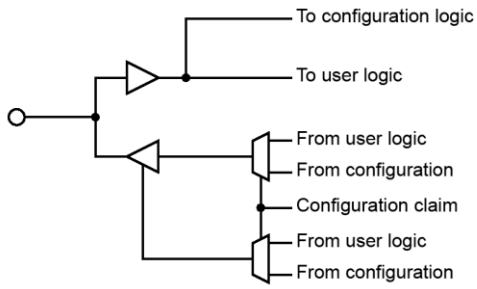
8. General Purpose Interface

The ATF280F provides a full set of highly configurable general purpose IOs.

For some of the FPGA IOs, the general purpose function of the IO is multiplexed with other functions such as mentioned in the Pin Description section. Please refer to the Pin Description section for details on the multiplexed functions of each IO.

It must be noted that while the configuration logic controls dual-use I/O pins during the ***configuration download*** lifephase, the configuration logic does not control the general purpose configuration.

Figure 8-1. Dual Use I/O principle



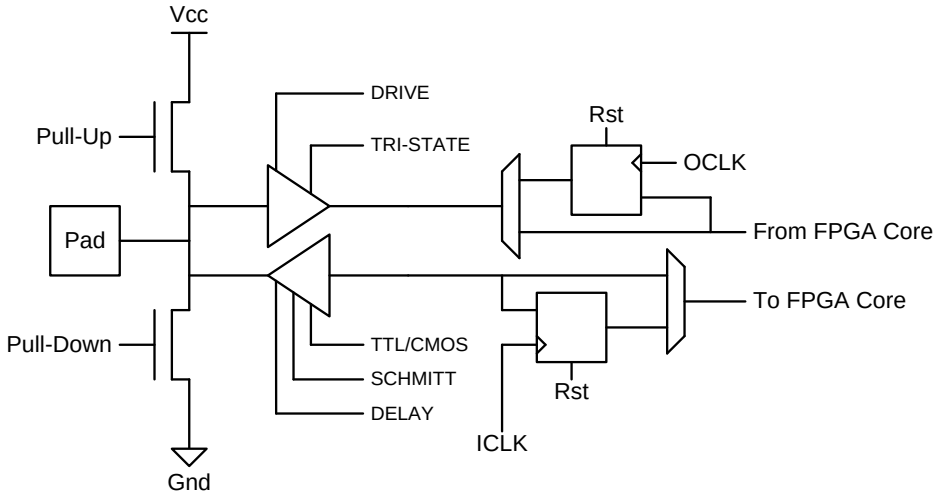
Caution: The user must be cautioned to avoid possible system problems with the use of dual-use I/O pins. For example, turning off the internal pull-up resistor for the open drain INIT pin would not apply the weak High required of an open drain driver. Conversely, disabling the pull-up and enabling the pull-down of the HDC pin might be a good idea, since the user may then actually see the pin go Low at the end of configuration.

Dual-use pins share input buffers. It should be noted that even when the configuration has claimed a pin for its own purposes, the user input buffer is still fully functional. This implies that any user logic tied to the input buffers of the pins in question will remain operational.

Each programmable I/O can be configured as input, output or bi-directional. When configured as input an optional Schmitt trigger can be enabled on the I/O. When configured as output optional PCI compatibility can be enabled. It is also possible to select the output buffer drive to optimize the performance of an interface in the application. In addition, the ATF280F provides pull-up and pull-down capability on each I/O.

Here is an overview of the IO structure.

Figure 8-2. ATF280F I/O structure



The following section presents all the possible configurations available for a programmable I/O.

8.2 Direction Configuration

Each of the general purpose IO can be individually configured in one of the following direction:

- Input,
- Output,
- Bidirectional.

8.3 Pull-up/Pull-down

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak “1” or “0” level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The pull-up and pull-down configuration is independent from any other configuration of the pad. The consequence is that it is possible to use the pull-up/pull-down configuration together with any of the other IO configuration.

The pull-up/pull-down configuration is available both for inputs and outputs.

Caution: By default, when an IO is not configured in the application bitstream of the FPGA, the IO pull-up is activated

8.4 Output Configuration

The ATF280F proposes a full set of configuration for the output management. Here are the descriptions for all the available settings.

8.4.1 Standard Configuration

In standard configuration, the IOs in output mode support a tri-state configuration. It is then possible to drive

- low level (logical 0)
- high level (logical 1)
- high impedance (logical Z)

8.4.2 Open Source

When configured in open source mode the IOs configured in output can only support

- high level (logical 1)
- high impedance (logical Z)

Note: In such a configuration, it is possible to drive a weak “0” by using the internal pull-down capability of the driver

8.4.3 Open Drain

When configured in open drain mode the IOs configured in output can only support

- low level (logical 0)
- high impedance (logical Z)

Note: In such a configuration, it is possible to drive a weak “1” by using the internal pull-up capability of the driver

8.4.4 Output drive

On the ATF280F, the output drive of each I/O configured in output is programmable. The drive capability is dependent upon the settings of the drive parameter inside the bitstream of the FPGA (FAST, MEDIUM and SLOW).

Three values are available for configuration of the drive for each output:

- FAST

When configured in FAST mode, the output buffer is capable to drive a high level of current. Such drive capability leads to fast slew rate whatever is the load on the pin

Note: In this mode, the current drive is compliant with the PCI specification.

- MEDIUM

When configured in MEDIUM mode, the output buffer is capable to drive an intermediate level of current.

- SLOW

When configured in SLOW mode, the output buffer is capable to drive a small level of current. Such drive capability leads to slow slew rate as soon as the load is important. SLOW configuration yields to standard buffer usage.

Table 8-1. Drive Capability for VCC = 3.3V

VCC=3.3V	I_{OH} (mA)		I_{OL} (mA)	
Config	Worst Case	Typical	Worst Case	Typical
SLOW	4	8	4	9
MEDIUM	10	17	10	23
FAST	14	22	14	28

Caution: When no modification is performed by the user on the IDS software, the default configuration of the drive for the I/Os is **FAST**.

8.5 Input Configuration

8.5.1 Schmitt

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 0.8V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

8.5.2 Delays

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

8.5.3 JTAG compliance

All programmable I/Os (including LVDS buffers) are IEEE1149.1 (Boundary scan) compliant. Each I/O may be included or excluded from boundary scan chain during the configuration of the FPGA.

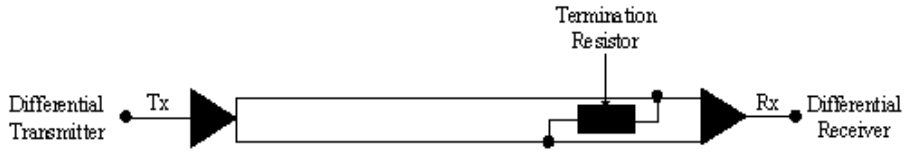
Caution: Refer to Erratum 1: JTAG functionality.

9. LVDS Interface

The ATF280F provides 16 pairs of LVDS IOs that comply with the **EIA-644 standard requirements**.

The basic LVDS interface consists in a single differential link interconnected between a transmiter and a receiver. Such a link requires a termination resistor on the receiver side to allow high frequency transfer usage. The nominal resistor value for the termination resistor 100 ohms.

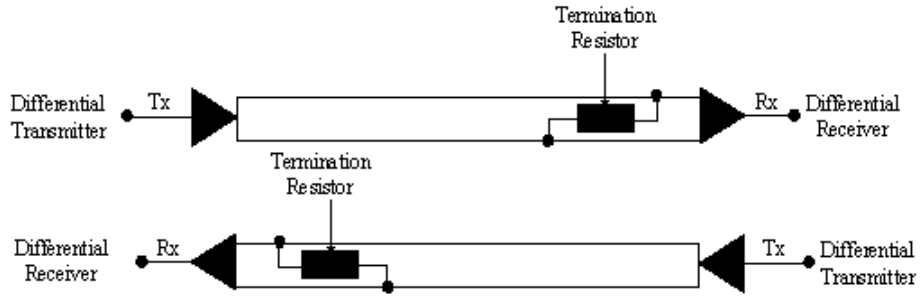
Figure 9-1. LVDS basic interface



The LVDS I/Os embedded on the ATF280F are composed of 8 LVDS transceiver (Tx) pairs, 8 receivers (Rx) pairs together with the reference voltages (Vref) that must be connected to an accurate 1.25V voltage to give references to the transceivers and to the receivers. They are spread in 4 clusters, each one consisting in

- 2x transceivers
- 2x receivers
- 1x reference voltage.
- Dedicated power pins (VCC and VSS)

Figure 9-2. LVDS bidirectional communication principle



10. Clock System

The ATF280F FPGA clock system consists in a fully SET hardened clocking scheme. It provides user with two types of clock

- 8 Global Clocks
- 4 Fast Clocks : FCK1 – FCK4

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks.

The clock can either come from the Column Clock or from the Plane 4 express bus. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration at power-up, constant “0” is provided to each register’s clock pins. After configuration at power-up, the registers either set or reset, depending on the user’s choice. The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Refer to **Registers** section about GCK and FCK activation or deactivation using IDS tools. All GCK and FCK lines are activated by default.

Figure 10-1. FPGA Clock repartition by column

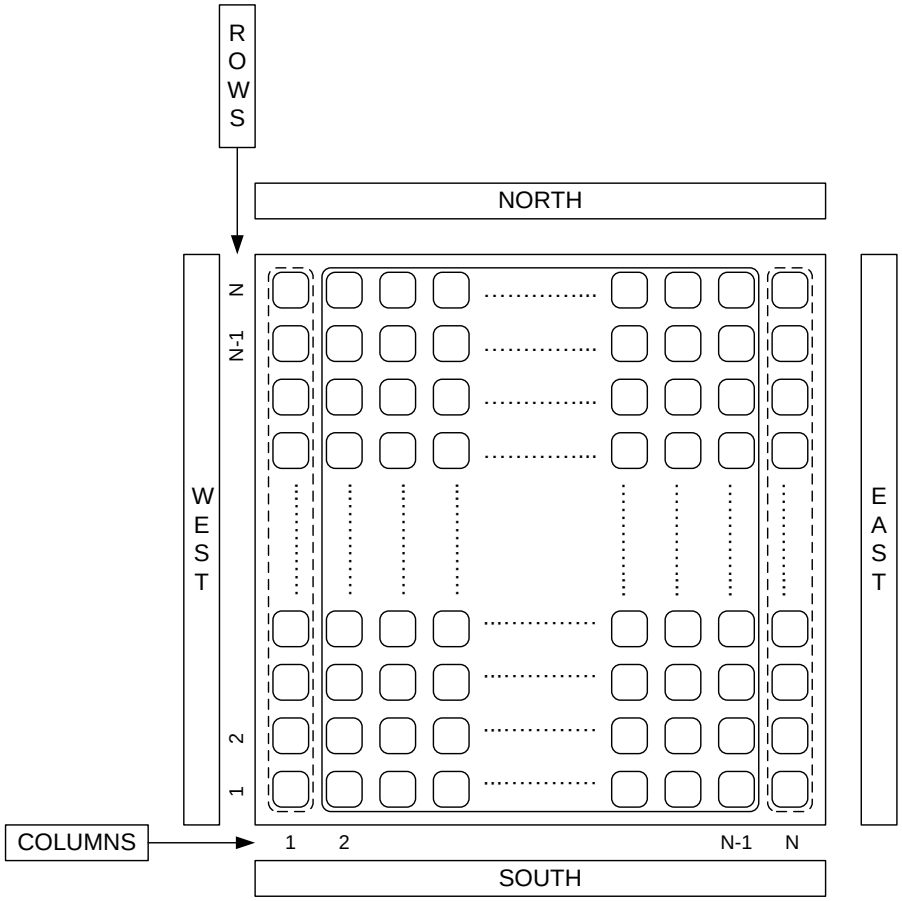
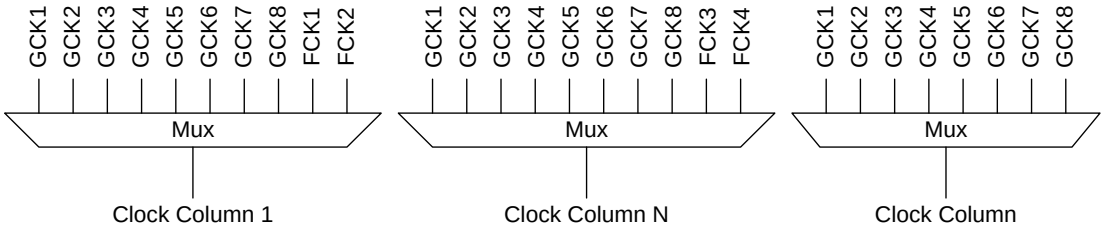


Figure 10-2. Column Clocking Overview



10.2 Global Clock

Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible. These signals are distributed across the top edge of the FPGA along special high-speed buses. Global Clock signals can be distributed throughout the overall FPGA with less than 1 ns skew.

This can be done by using Assign Pin Locks command in the IDS software to lock the clocks to the Global Clock locations.

10.3 Fast Clock

The fast clocks are used to provide fast clocking on the first/last stage of a structure close to the pad of the devices. They are only accessible on the far east/west area of the FPGA.

There are four Fast Clocks inputs (FCK1 - FCK4) on the ATF280F, two per edge column of the array. Even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network.

On the extreme west of the device, FCK1 and FCK2 inputs are internally multiplexed. This allows use of a fast clocking for the west-side I/Os. FCK1 and FCK2 are multiplexed: only one of these two FCKs can be used at a time.

On the extreme east of the device, FCK3 and FCK4 inputs are internally multiplexed. This allows use of a fast clocking for the east-side I/Os. FCK3 and FCK4 are multiplexed: only one of these two FCKs can be used at a time.

The IDS software tools handle derived clocks to global clock connections automatically if used.

Caution: Four FCK IOs are provided to allow flexible configuration of the clock system to user but only one east-side and one west-side can be used at a time.

11. Reset System

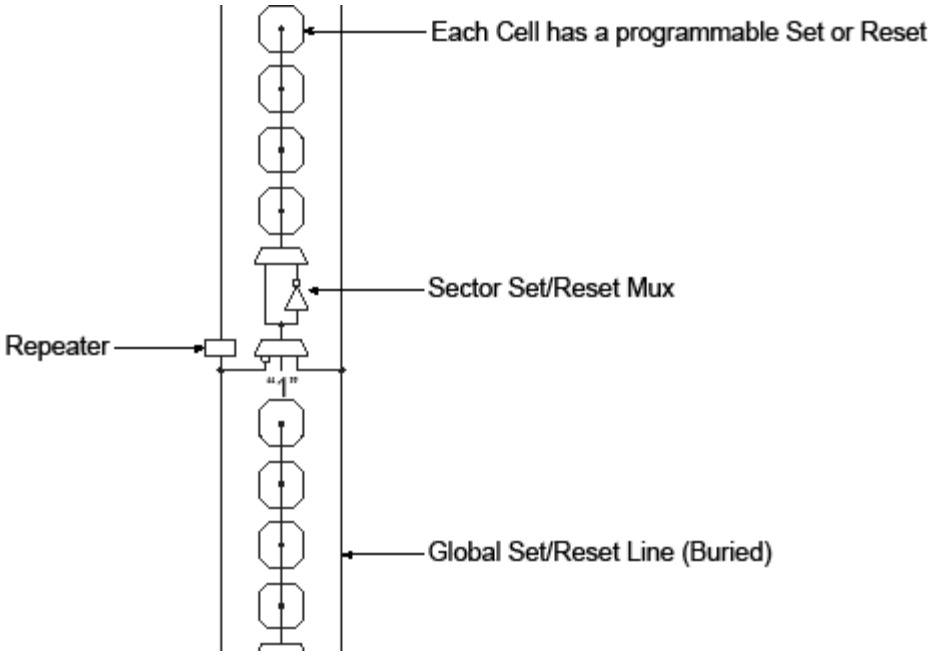
The ATF280F reset scheme is essentially the same as the clock scheme except that there is only one differential Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). Like the clocking scheme, set/reset scheme is SET hardened.

The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux (Figure 10). The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11-1. Set/Reset



12. Power Supply Management

12.1 Cold sparing

Cold sparing capability of the IOs allows to be electricaly connected to a bus while its power supply remains in the range [VSS-300mV/VSS+300mV], this without any risk of damage for the device. Cold-sparing allows a redundant spare to be electrically connected but unpowered until needed.

For applications requiring high reliability, the capability to use of a redundant device is a key feature. Cold sparing availability on the ATF280F makes the FPGA especially suitable for high reliability systems.

The cold sparing feature is available for all the IOs:

- All the General Purpose IOs
- All the LVDS IOs

They present an high input impedance when unpowered [VSS-300mV / VSS+300mV] and exhibit a negligible leakage current if exposed to a non-null input voltage at that time.

12.2 Power sequencing

The ATF280F is based on Atmel ATC18RHA 0.18 µm CMOS process. When the ATF280F needs to be powered "on/off" while other circuits in the application are still powered, the recommended “power on/off” sequences are:

- power-up
  - First power VCC33 (I/O),
  - Then power VDD18 (Core).
- power-down
  - First unpower VDD18 (Core),
  - Then unpower VCC33 (I/O).

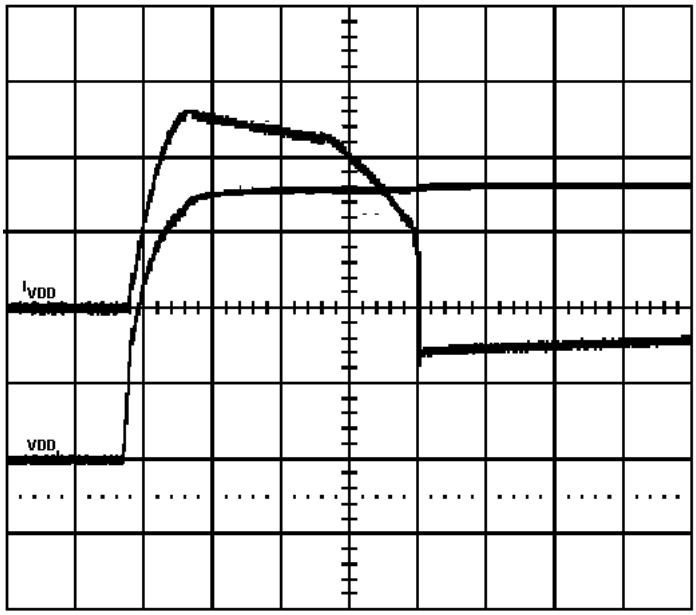
It is also recommended to stop all activity during these phases as a bi-directional could be in an undetermined state (input or output mode) and create bus contention.

12.3 Power-On Management

ATF280F has an inrush current during power-up phase that need to be considered with care by the board designer in order to adjust his power consumption budget. This inrush current is due to indeterminate states of configuration memory cells not already initialized which create an excessive leakage current.

The ATF280F design has been optimized in order to rminimize the leakage causing the inrush current.

Figure 12-1. Inrush current



The following table shows the ATF280F inrush characteristics

Table 12-1. Inrush Current

	Worst Case	Typical
125°C	2	1.8
90°C	2	1.7
25°C	2	1.7
-30°C	2	1.6
-55°C	2	1.5

Since the inrush current can reach more than 1.8A, we recommend users to dimension their power supply in order to be able to provide at least 2 Amps peak current.

13. JTAG

All I/Os are IEEE1149.1 compliant. Each I/O may be included or excluded from boundary scan chain during the configuration of the FPGA.

Caution: Refer to Erratum 1: JTAG functionality.

13.1 Overview

The ATF280F implements a standard interface compliant with the IEEE 1149.1 JTAG specification that can be used for PCB testing using the JTAG boundary-scan capability.

The JTAG interface is accessed through five dedicated pins. In JTAG terminology, these pins constitute the Test Access Port (TAP).

The following table summarizes the TAP pins and there function at JTAG level.

Table 13-1. TAP Pins

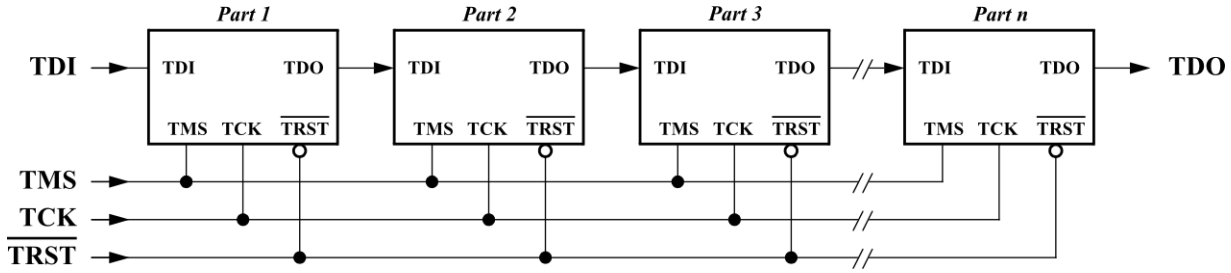
TCK	Test Clock	Input	Used to clock serial data boundary into scan latches and control sequence of the test state machine. TCK can be asynchronous with system clock.
TMS	Test Mode select	Input	Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.
TDI	Test Data Input	Input	Serial input data to the boundary scan latches. Synchronous with TCK.
TDO	Test Data Output	Output	Serial output data from the boundary scan latches. Synchronous with TCK.
TRST	Test Reset	Input	Resets the test state machine. can be asynchronous with TCK.

For more details, please refer to the 'IEEE Standard Test Access Port and Boundary Scan' specification.

Any ATF280 based system will contain several JTAG compatible chips. These are connected using the minimum (single **TMS** signal) configuration. This configuration contains three broadcast signals (**TMS**, **TCK**, and **TRST*** ,) which are fed from the JTAG master to all JTAG slaves in parallel, and a serial path formed by a daisy-chain connection of the serial test data pins (**TDI** and **TDO**) of all slaves.

The TAP supports a BYPASS instruction which places a minimum shift path (1 bit) between the chip's **TDI** and **TDO** pins. This allows efficient access to any single chip in the daisy-chain without board-level multiplexing.

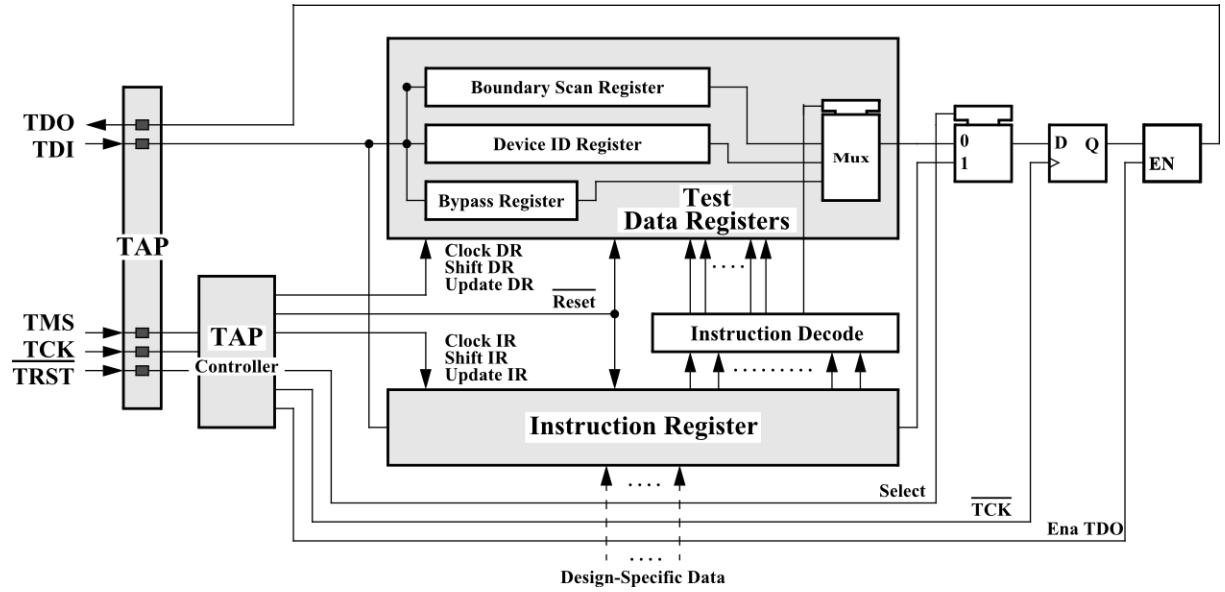
Figure 13-1. JTAG Serial connection using 1 TMS Signal



13.2 TAP Architecture

The TAP implemented in the ATF280F consists in a TAP interface, a TAP controller and a number of shift registers including an instruction register (IR) and some other registers.

Figure 13-2. AT697 TAP Architecture



13.2.2 TAP Instructions

The following instructions are supported by the TAP.

Table 13-2. TAP instruction set

000	EXTEST	Boundary scan register	Boundary scan chain
001	SAMPLE/PRELOAD	Boundary scan register	Boundary scan chain
010	BYPASS	Bypass register	Bypass scan chain
111	IDCODE	Device id register	ID register scan chain

13.2.2.2 BYPASS

This instruction is binary coded "**010**"

It is used to speed up shifting at board level through components that are not to be activated.

13.2.2.3 EXTEST

This instruction is binary coded "**000**"

It is used to test connections between components at board level. Components output pins are controlled by boundary scan register during Capture DR on the rising edge of **TCK**.

13.2.2.4 SAMPLE/PRELOAD

This instruction is binary coded "**001**"

It is used to get a snapshot of the normal operation by sampling I/O states during Capture DR on the rising edge of **TCK**. It allows also to preload a value on the output latches during Update DR on falling edge of **TCK**. It do not modify system behaviour.

13.2.2.5 IDCODE

This instruction is binary coded "**111**"

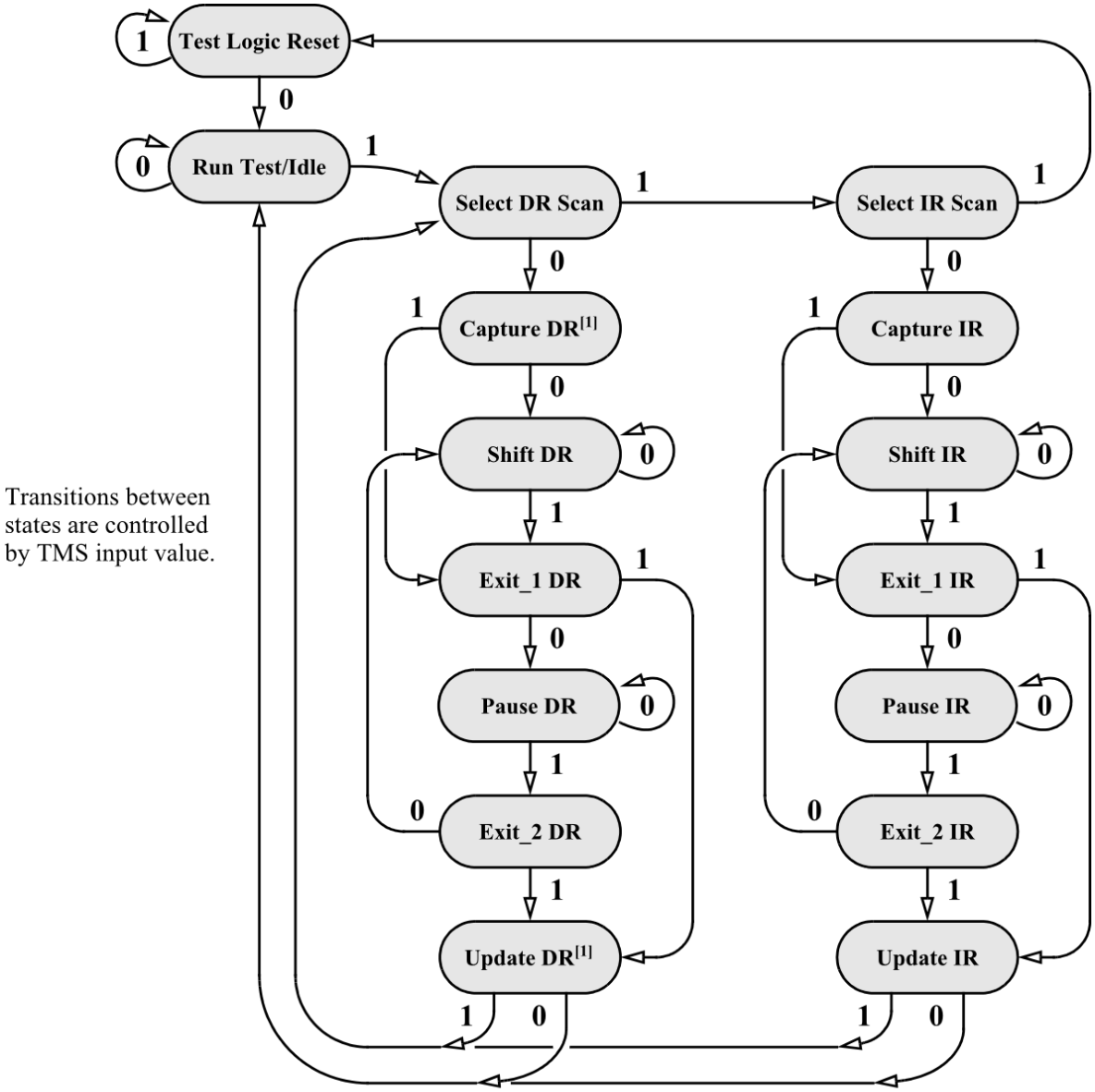
Value of the IDCODE is loaded during Capture DR.

13.2.3 TAP Controller

The TAP controller is a synchronous finite state machine (FSM) which controls the sequence of operations of the JTAG test circuitry, in response to changes at the JTAG bus. (Specifically, in response to changes at the **TMS** input with respect to the **TCK** input.)

The TAP controller FSM implements the state (16 states) diagram as detailed in the following diagram. The IR is a 3-bit register which allows a test instruction to be shifted into the AFT280. The instruction selects the test to be performed and the test data register to be accessed. Although any number of loops may be supported by the TAP, the finite state machine in the TAP controller only distinguishes between the IR and a DR. The specific DR can be decoded from the instruction in the IR.

Figure 13-3. TAP - State Machine



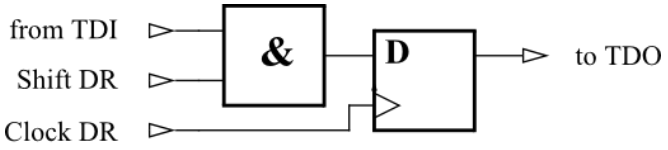
Due to the scan cell layout, "Capture DR" and "Update DR" are states without associated action during the scanning of internal chains.

13.2.4 TAP Data Registers

13.2.4.1 Bypass Register

Bypass register containing a single shift register stage is connected between **TDI** and **TDO**.

Figure 13-4. Bypass Register Cell



13.2.4.2 Device ID register

Device ID register is a read only 32-bit register. It is connected between **TDI** and **TDO**.

Table 13-3. Device ID

0001	1111 1111 1111 1111	000 0101 1000	1

ID register value: 0x1FFFF0B1

Field Definitions:

- [31:28]: Version – Version number – 0x1
- [27:12]: Part ID – Represent part number as assigned by Vendor – 0xFFFF
- [11:1]: Manufacturer's ID – Represent manufacturer's ID as per JEDEC – 0x058
- [0]: Constant – Constant tied to logic '1'

14. Register Description

The AT40K series devices have a 32-bit control register that is written at the beginning of a configuration download. These bits control various configuration sequence parameters. All bits are set to 0 during a configuration clear cycle. In parallel modes, byte 0 is loaded first. In serial modes, bit-31 is loaded first. The control register settings are made in the FPGA Designer IDS Software Options section:

- Go to the Options menu on the IDS (Figaro) main window and select Options.
- Choose AT40K Bitstream from the topics list(1)

Caution: IDS uses names "B0" ~ "B31" for "CR0" ~ "CR31" for the Control Register.

Table 14-1. Control Registers

Byte 3	CR_{31}	CR_{30}	CR_{29}	CR_{28}	CR_{27}	CR_{26}	CR_{25}	CR_{24}
Byte 2	CR_{23}	CR_{22}	CR_{21}	CR_{20}	CR_{19}	CR_{18}	CR_{17}	CR_{16}
Byte 1	CR_{15}	CR_{14}	CR_{13}	CR_{12}	CR_{11}	CR_{10}	CR_{9}	CR_{8}
Byte 0	CR_{7}	CR_{6}	CR_{5}	CR_{4}	CR_{3}	CR_{2}	CR_{1}	CR_{0}

14.2 Description

CR0 – Mode 6 Address Counter

- 0 = Reset Address Counter
- 1 = Retain Address Counter

CR0 controls the value of the Mode 6 device's memory address counter after each configuration sequence. The default resets the address up-counter to 000000 after each configuration download is completed. When this bit is set, the memory address counter retains its last value. This allows multiple designs to be stored sequentially in an external memory device for use in reconfigurable systems.

CR1 - Not used (ignored)

CR2 - Cascading

- 0 = Enable Cascading
- 1 = Disable Cascading

CR2 controls the operation of the dual-function I/O CSOUT. When CR2 is set, the CSOUT pin is not used by the configuration during downloads.

CR3 - Check

- 0 = Check Function enabled
- 1 = Check Function disabled

CR3 controls the operation of the CHECK pin and enables the Check Function. When CR3 is set, the CHECK pin is not used by the configuration during downloads.

CR4 - Memory Lockout

- 0 = Memory Lockout disabled
- 1 = Memory Lockout enabled

CR4 is the Security Flag and controls the writing and checking of configuration memory during any subsequent configuration download. When CR4 is set, any subsequent configuration download initiated by the user, whether a normal download or a CHECK function download, causes the INIT pin to immediately activate. CON is released, and no further configuration activity takes place. The download sequence during which CR4 is set is NOT affected. The Control Register write is also prohibited, so bit CR4 may only be cleared by a power-on-reset or manual reset.

CR5 - JTAG

- 0 = JTAG enable
- 1 = JTAG disable

CR6 – OTS

- 0 = OTS disabled
- 1 = OTS enabled

Setting CR6 makes the OTS pin an input which controls the global tri-state control for all user I/O.

CR7 – Parallel bus width

- 0 = 8-bit data access
- 1 = 16-bit (Wide) data access

CR7 is the Wide data control bit. Setting this bit immediately enables bits D8:D15 of the configuration interface as inputs for all parallel modes (2 and 6). All writes and checks of configuration memory are subsequently performed by 16 bits. Cr7 is ignored in serial modes (0, 1 and 7).

CR8 - Recurrent checksum

- 0 = no recurrent checksum
- 1 = activates the recurrent checksum

If configured in Master mode 0, it is mandatory to activate CR13 bit when using CR8 bit in order to clock the CSIC feature. For all other modes, CCLK shall be provided from the external.

CR9 - Function bad_state

- 0 = no function bad_state
- 1 = enables the function bad_state during the FPGA configuration

CR10 - Not used (ignored)

CR11 - Not used (ignored)

CR12 - Not used (ignored)

CR13 – CCLK operation

- 0 = CCLK normal operation
- 1 = CCLK continues after configuration

Setting bit CR13 allows the CCLK pin to continue to run after configuration download is completed. This bit is valid for Master Mode only.

CR14/CR15 – CCLK Frequency

- 00 = 1 MHz
- 01 = 4 MHz
- 10 = 8 MHz
- 11 = 16 MHz

Bits CR14 and CR 15 speed up the internal oscillator and allow the Master Mode to drive CCLK at 1, 4, 8 or 16 MHz. As soon as the values of these bits are sampled by the FPGA, the CCLK frequency is increased consequently.

CR16/CR23 – GCK enable

- 0 = GCK 0:7 always enabled
- 1 = GCK 0:7 disabled during configuration download.

Setting CR16:C23 allows the user to disable the input buffers driving the global clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective GCLK signal, and stop in a High (“1”) state. Setting one of these bits disables the appropriate GCLK input buffer only and has no effect on the connection from the input buffer to the FPGA array.

CR24/CR27 – FCK enable

- 0 = FCK 0:3 always enabled
- 1 = FCK 0:3 disabled during configuration download.

Setting CR24:C27 allows the user to disable the input buffers driving the fast clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective FCLK signal, and stop in a High (“1”) state. Setting one of these bits disables the appropriate FCLK input buffer only and has no effect on the connection from the input buffer to the FPGA array.

CR28 - Reserved

Caution: must be '0'

CR29 - Not used (ignored)

CR30 – Global Set/Reset

- 0 = Global set/reset normal
- 1 = Global set/reset active (Low) during configuration

CR30 allows the Global set/reset hold the core DFFs in set/reset during any configuration download. The Global set/reset net is released at the end of configuration download on the rising edge of CON.

CR31 – IO tristate

- 0 = Disable I/O tri-state
- 1 = I/O tri-state during configuration

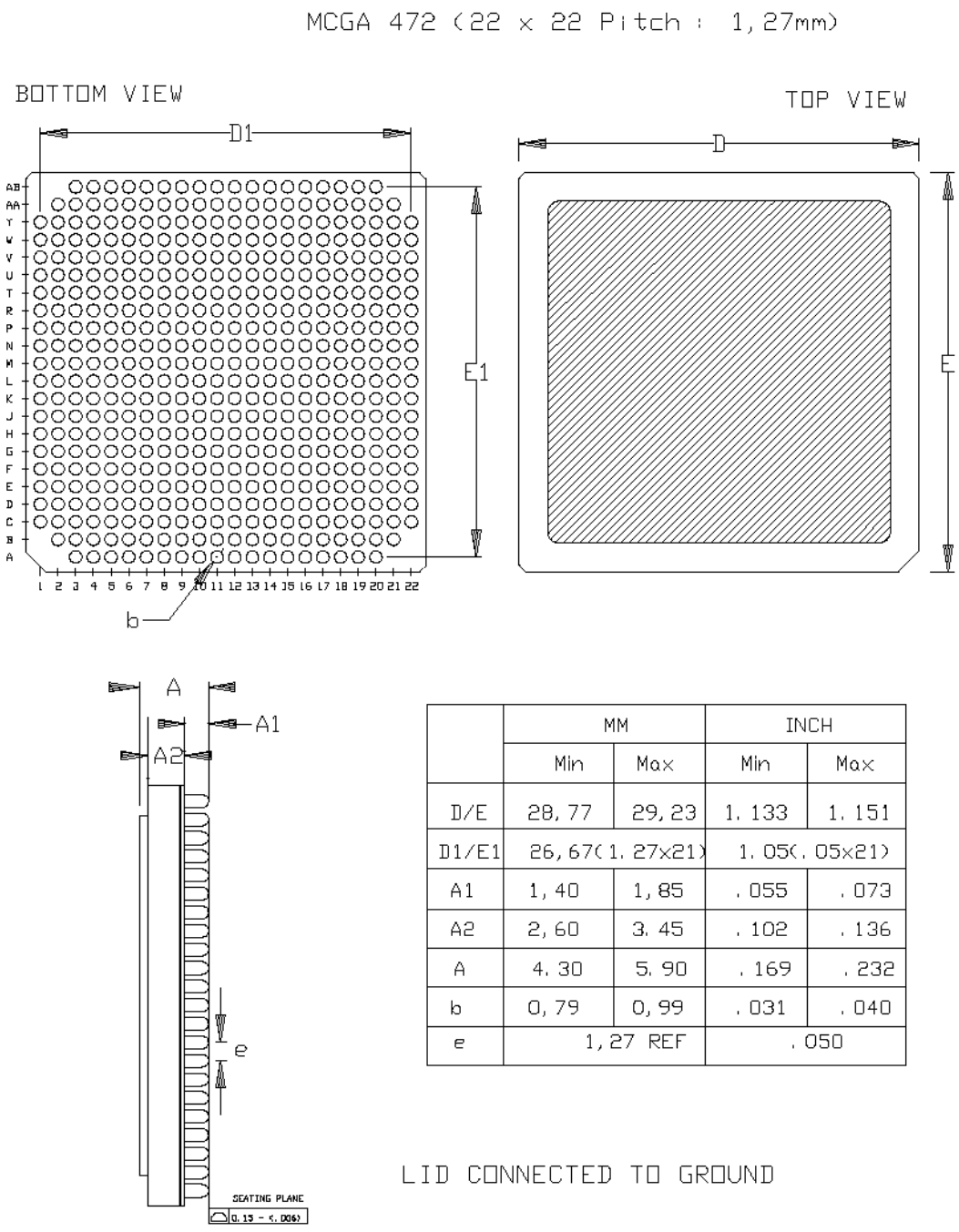
CR31 forces all user defined I/O pins to go tri-state during configuration download. tri-state is released at the end of configuration download on the rising edge of CON.

15. Package Information

15.1 Packages Outline

15.1.1 CCGA 472 outline

Figure 15-1. Mechanical description

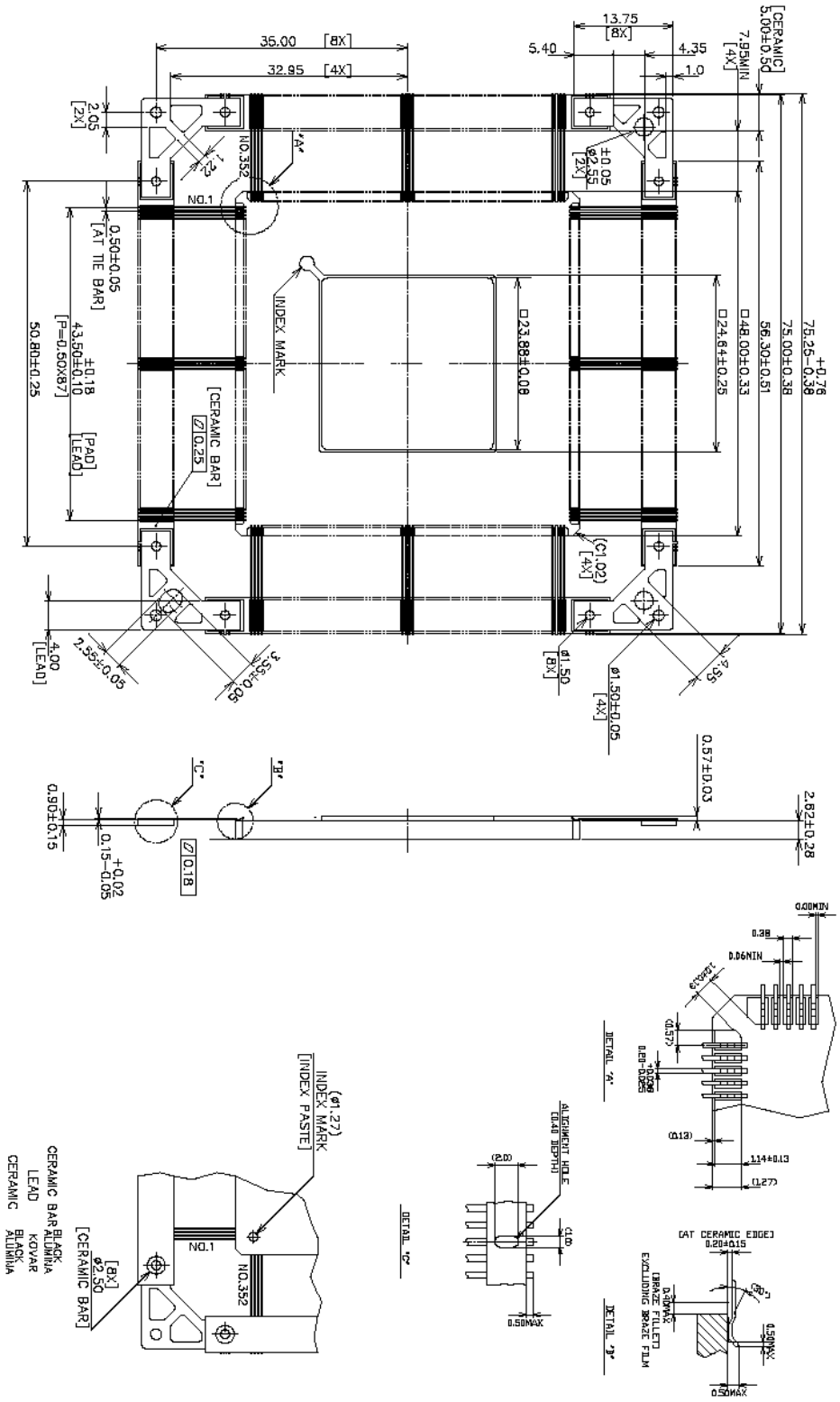


	MM		INCH	
	Min	Max	Min	Max
D/E	28,77	29,23	1,133	1,151
D1/E1	26,67(1,27x21)		1,05(,05x21)	
A1	1,40	1,85	,055	,073
A2	2,60	3,45	,102	,136
A	4,30	5,90	,169	,232
b	0,79	0,99	,031	,040
e	1,27 REF		,050	

LID CONNECTED TO GROUND

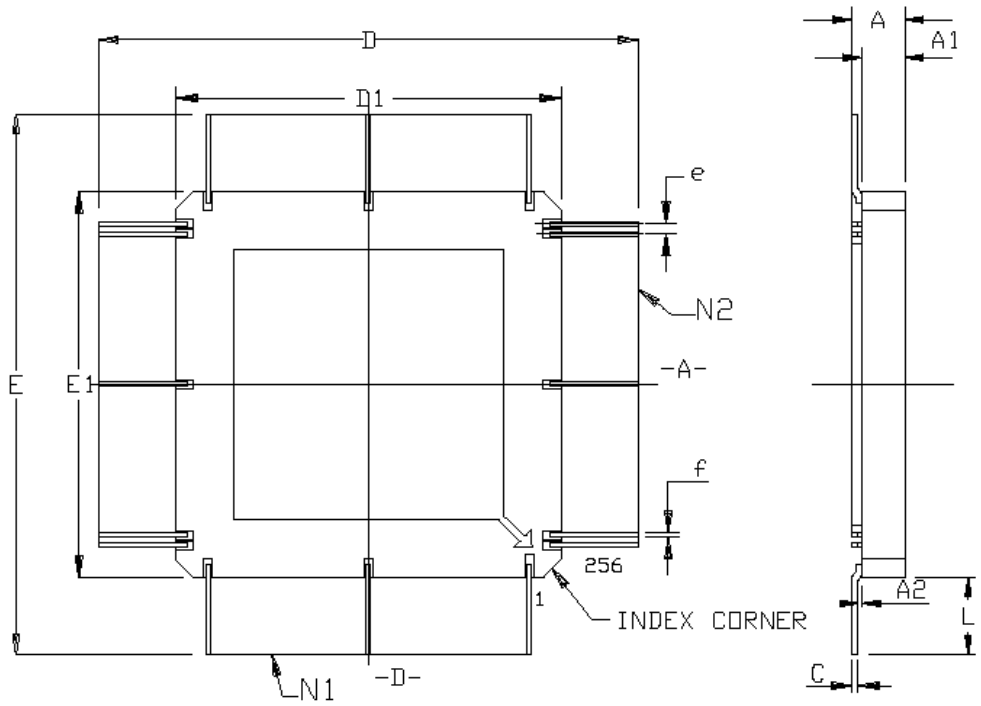
15.1.2 QFP 352 outline

Table 15-1. Mechanical description



15.1.3 QFP 256 outline

Table 15-2. Mechanical description



	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

15.2 Pin Assignment

The core of the FPGA is supplied through VDD pins that are linked all together in a dedicated power cluster.

The ATF280F periphery is divided into 12 clusters. Eight clusters are dedicated to programmable I/Os and four clusters are dedicated to LVDS. Each cluster consists in a set of I/O together with its dedicated power supply source. The following tables summarized the pin assignment cluster by cluster.

The ground planes between core and periphery are linked together and are described as a “Gnd” cluster.

15.2.1 Core Power and Ground Cluster

Table 15-3. Core Power and Ground Cluster

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
Core	VDD	A3	122	184	Gnd	VSS	A4	121	183
Core	VDD	A20	72	258	Gnd	VSS	A19		
Core	VDD	B3			Gnd	VSS	B2	71	257
Core	VDD	B20	58	272	Gnd	VSS	B21		
Core	VDD	C1			Gnd	VSS	C3		271
Core	VDD	C2			Gnd	VSS	C20		
Core	VDD	C21	8	346	Gnd	VSS	D1	7	345
Core	VDD	C22			Gnd	VSS	D22		
Core	VDD	Y1			Gnd	VSS	W1	57	7
Core	VDD	Y2	250	8	Gnd	VSS	W22	249	
Core	VDD	Y21	200	82	Gnd	VSS	Y3	199	81
Core	VDD	Y22			Gnd	VSS	Y20		
Core	VDD	AA3			Gnd	VSS	AA2	185	95
Core	VDD	AA20	186	96	Gnd	VSS	AA21		
Core	VDD	AB3	136	170	Gnd	VSS	AB4	135	169
Core	VDD	AB20			Gnd	VSS	AB19		

15.2.2 IO clusters

Table 15-4. IO cluster 1

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
1	IO722_GCK7_A1	G6	130	178	1	IO793	K7		202
1	IO725	J9			1	IO797_A5	J4	147	203
1	IO727_A0	F4	131	179	1	IO799	J1		204
1	IO731	H7			1	IO803	J2	149	206
1	IO733	J7	134	181	1	IO805	L11		207
1	IO737	H6	137		1	IO807	J3		208
1	IO739	D3		182	1	IO811_A6	L10	150	209
1	IO743_A2_CS1	D2	138	185	1	IO813	K5		210
1	IO745	E3			1	IO817	K1	151	
1	IO747	E2	139	186	1	IO819	J5		211
1	IO751	E4			1	IO823	L6	152	212
1	IO753	F3	140	187	1	IO825_A7	L1	154	214
1	IO757	E5	141	189	1	IO831	M1	155	
1	IO759	G3		190	1	IO833	L7		215
1	IO763	F2			1	TCK	K10	129	177
1	IO765	G1		191	1	VCC	H8	132	180
1	IO767_A3	G4	142	192	1	VCC	E1		188
1	IO771	K9		193	1	VCC	G2	144	196
1	IO773	F5	143	194	1	VCC	H5		205
1	IO777	H3		195	1	VCC	K4	153	213
1	IO779	H4		197	1	VCC	J8	133	
1	IO783_A4	H1	145	198	1	VCC	F1		
1	IO785	G5		199	1	VCC	J6		
1	IO787	K8	146	200	1	VCC	K6	148	
1	IO791	H2		201	1	VCC	L4		

Table 15-5. IO cluster 3

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
3	IO847	M5		226	3	IO923_A12	N8	181	252
3	IO851	N1	166	227	3	IO925	U2		253
3	IO853	M6		228	3	IO927	V1	182	254
3	IO857_A8	L8	167	229	3	IO931	V4		
3	IO859	M7		230	3	IO937_A13	P7	183	255
3	IO863	L9	168	231	3	IO939	V2		256
3	IO865	M8		232	3	IO943	V3		
3	IO867	N4	169	233	3	IO945	M10		260
3	IO871	N6		235	3	IO947	W3	188	
3	IO873_A9	N5	172	236	3	IO951	N9		
3	IO879	M9		237	3	IO953_A14	T7	189	261
3	IO883	P3	173	238	3	IO957	R6		
3	IO885	P2	174		3	IO960_GCK8_A15	U6	190	262
3	IO887	R1		239	3	TDI	U4	192	264
3	IO891_A10	R5	175	240	3	TDO	T6	191	263
3	IO893	R3	176	242	3	VCC	U3	180	250
3	IO897	R2		243	3	VCC	W2	187	259
3	IO899	P6	177	244	3	VCC	R7		
3	IO903	T5			3	VCC	P5	171	234
3	IO905_A11	T1	178	245	3	VCC	P4		241
3	IO907	R4		246	3	VCC	P8		
3	IO911	T3		247	3	VCC	P1	170	
3	IO913	T2	179	248	3	VCC	N7		
3	IO917	U1		249	3	VCC	U5		
3	IO919	T4		251	3	VCC	W4	184	

Table 15-6. IO cluster 4

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
4	IO1_GCK1_A16	P9	195	267	4	IO67	AA8	213	288
4	IO103	W10		300	4	IO7	T8		
4	IO105_A20	T11	220	301	4	IO71	T10		289
4	IO11	T9	201		4	IO73	W9	214	290
4	IO111	AB11		302	4	IO77	AB9		291
4	IO13	U8		268	4	IO79	AA9	215	293
4	IO17	Y4		269	4	IO83	M11		
4	IO19_A17	AA4	202	270	4	IO85	Y9	216	294
4	IO23	Y5			4	IO87	N11		295
4	IO25	AA5	203	273	4	IO93	AB10	217	296
4	IO27	W5		274	4	IO97	V10		297
4	IO31	Y6	204	275	4	IO99	U11	218	298
4	IO33	V5	205	277	4	TMS	N10	193	265
4	IO37	Y7		278	4	TRST	U7	194	266
4	IO39_A18	AA6	206	279	4	VCC	R8	197	
4	IO43	AB7		280	4	VCC	AB5		276
4	IO45	W7	207	281	4	VCC	AA7	209	284
4	IO47	P10		282	4	VCC	V8		292
4	IO5	W6	196		4	VCC	V9	219	299
4	IO51	V6	208	283	4	VCC	R9	198	
4	IO53	Y8			4	VCC	AB6		
4	IO57	W8		285	4	VCC	U9	210	
4	IO61_FCK1	AB8	211	286	4	VCC	U10		
4	IO63_A19	V7	212	287	4	VCC	W11		
4	IO65	R10							

Table 15-7. IO cluster 6

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
6	IO125	V12	231	313	6	IO199	R13		340
6	IO127	W12		314	6	IO203_A23	AA17	247	341
6	IO131	AB13		315	6	IO205	AB18	248	342
6	IO133_A21	AB12	232	316	6	IO207	W18		343
6	IO137	U12		317	6	IO213	T14		344
6	IO139	P11	233	318	6	IO217	AA18	251	347
6	IO143	T12		319	6	IO219	Y18		349
6	IO145	W13	234	320	6	IO223	N12		
6	IO147	AB14	237	322	6	IO225_OTSN	Y19	254	350
6	IO151	V13		323	6	IO227	P13		
6	IO153	U13	238		6	IO231	T16		
6	IO157	Y14		324	6	IO233	U15		
6	IO159	P12	239	325	6	IO237	U17		
6	IO163	AA14		326	6	IO240_GCK2	U16	255	351
6	IO165	AB15	240	327	6	M0	W17	256	352
6	IO167	V15		328	6	VCC	V14	236	321
6	IO171	Y15	242	330	6	VCC	W14	241	329
6	IO173	AA15		331	6	VCC	Y17		
6	IO175	U14		332	6	VCC	AA19	253	348
6	IO177_A22	V16	243	333	6	VCC	T15		
6	IO180_FCK2	AB16	244	334	6	VCC	R12	235	
6	IO185	W15		335	6	VCC	T13		
6	IO187	Y16	245	336	6	VCC	V17		339
6	IO191	AA16		337	6	VCC	W19	252	
6	IO193	AB17	246	338	6	VCC	R14		
6	IO197	W16							

Table 15-8. IO cluster 7

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
7	IO241_GCK3	P14	3	3	7	IO313	P19		26
7	IO245	U19			7	IO317	P22	21	27
7	IO247	R16			7	IO319	P21		29
7	IO251	P16	6		7	IO323_D14	M12	22	30
7	IO253	R17			7	IO325	P20		31
7	IO257	W20			7	IO327	M13	23	32
7	IO259_LDC	W21	9	5	7	IO331	N18		33
7	IO263	V20		6	7	IO333	N22	24	
7	IO265_HDC	V21	10	9	7	IO337	P18		34
7	IO267	V19		10	7	IO339	M17	25	35
7	IO271	U20	11	11	7	IO343	M22		37
7	IO273	V18		13	7	IO345_D13	M16	27	38
7	IO277	T20		14	7	IO351	L22		39
7	IO279_D15	U21	12	15	7	M1	N13	1	1
7	IO283	T22	13	16	7	M2	T17	2	2
7	IO285	T19		17	7	VCC	R15	4	4
7	IO287	N14	14		7	VCC	V22		12
7	IO291	U18		18	7	VCC	T21	16	20
7	IO293	R20	15	19	7	VCC	R18		28
7	IO297	R19		21	7	VCC	N19	26	36
7	IO299	R22			7	VCC	P15	5	
7	IO303_INIT	T18	18	22	7	VCC	U22		
7	IO305	N15		23	7	VCC	P17	17	
7	IO307	R21	19	24	7	VCC	N17		
7	IO311	N16	20	25	7	VCC	M19		

Table 15-9. IO cluster 9

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
9	CON	F19	64	88	9	IO437	G19		75
9	IO365	L18		50	9	IO439	K15		76
9	IO367	L19	38	51	9	IO443_D9	F21	53	77
9	IO371	K22		52	9	IO445	E22	54	78
9	IO373_D12	M14	39	53	9	IO447	E19		79
9	IO377	L17		54	9	IO453	J16		80
9	IO379	K19	40	55	9	IO457	E21	55	83
9	IO383	L16		56	9	IO459	E20	60	85
9	IO385	J18	41	57	9	IO463	L13		
9	IO387	J22	44	59	9	IO465_D8	D20	61	86
9	IO393	K17		60	9	IO467	K14		
9	IO397_D11	J20	45	61	9	IO471	G16	62	
9	IO399	L14			9	IO473	H17		
9	IO403	J21	46	62	9	IO477	F17		
9	IO405	H22		63	9	IO480_GCK4	G17	63	87
9	IO407	H18	47	64	9	VCC	K18	43	58
9	IO411	H20	49	66	9	VCC	J19	48	65
9	IO413	H21		67	9	VCC	F20		74
9	IO417	J17		68	9	VCC	D21	59	84
9	IO419_D10	G18	50	69	9	VCC	H16		
9	IO423	G22		70	9	VCC	L15	42	
9	IO425	H19	51	71	9	VCC	K16		
9	IO427	G20			9	VCC	F18		
9	IO431	G21		72	9	VCC	D19	56	
9	IO433	F22	52	73	9	VCC	J15		

Table 15-10. IO cluster 10

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
10	RESERVED	F16	66	90	10	IO553	D14	85	115
10	IO482_GCK5	J14	67	91	10	IO557	G13		116
10	IO485	D17			10	IO559	B14		118
10	IO487	G15	68	92	10	IO563	F13	86	119
10	IO491	G14	73		10	IO565	C14		120
10	IO493_D7	F15	74	94	10	IO567	L12	87	121
10	IO497	C19			10	IO571	E13		122
10	IO503	C18			10	IO573	K12	88	123
10	IO505	B19	75	97	10	IO577	E14		124
10	IO507	D18		98	10	IO579	A13	89	125
10	IO511	B18	76	99	10	IO583	A12		
10	IO513_D6	E18	77	101	10	IO585_D4	D12	91	127
10	IO517	A17		102	10	IO591	G12		
10	IO519	B17		103	10	RESETN	K13	65	89
10	IO523	C16		104	10	VCC	H15	69	93
10	IO525	D16	78	105	10	VCC	A18		100
10	IO527	A16		106	10	VCC	B16	80	109
10	IO531_D5	E17	79	107	10	VCC	E15		117
10	IO533	J13		108	10	VCC	D13	90	126
10	IO537	D15	82	110	10	VCC	H14	70	
10	IO539	F14		111	10	VCC	C17		
10	IO543_FCK3	E16	83	112	10	VCC	C15	81	
10	IO545	A15			10	VCC	A14		
10	IO547_CS0	B15	84	113	10	VCC	F12		
10	IO551	H13		114					

Table 15-11. IO cluster 12

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
12	CCLK	D6	127	176	12	IO679	C6	117	164
12	IO605	E11		138	12	IO683	B6		165
12	IO607	H12	102		12	IO685	H10		166
12	IO611	D11	103	139	12	IO687	D5	118	167
12	IO613	J12		140	12	IO691	A5		
12	IO617_D3	A10	104	141	12	IO693_D1	G9	119	168
12	IO619	D10		142	12	IO697	B5		171
12	IO623	F11		143	12	IO699	C5	123	173
12	IO625	E9	105	144	12	IO703	K11		
12	IO627	H11	108	146	12	IO705	C4	124	
12	IO633	A9		147	12	IO707	J10		
12	IO637	C9	109	148	12	IO711	G7		
12	IO639	F10		149	12	IO713_D0	F8	125	174
12	IO643	B9		150	12	IO717	F6		
12	IO645	J11	110	151	12	IO720_GCK6_CSOUT	F7	126	175
12	IO647	E8		152	12	VCC	G8	128	
12	IO651	G10	111	154	12	VCC	E10	107	145
12	IO653	B8		155	12	VCC	D9		153
12	IO655_CHECKN	C8	112	156	12	VCC	A6	116	162
12	IO658_FCK4	E7	113	157	12	VCC	B4		172
12	IO661	F9			12	VCC	G11	106	
12	IO665	D8	114	158	12	VCC	A8		
12	IO667	A7		159	12	VCC	E6		
12	IO671	B7		160	12	VCC	D4	120	
12	IO673_D2	C7	115	161	12	VCC	H9		
12	IO677	D7		163					

15.2.3 LVDS clusters

Table 15-12. LVDS cluster – Channel 1, 2, 3 and 4

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
5	ILVDS1	Y10	221	303	8	ILVDS3	N20	28	40
5	ILVDS1N	Y11	222	304	8	ILVDS3N	M20	29	41
5	ILVDS2	AA10	223	305	8	ILVDS4	N21	30	42
5	ILVDS2N	AA11	224	306	8	ILVDS4N	M21	31	43
5	OLVDS1	AA12	226	308	8	OLVDS3	L21	33	45
5	OLVDS1N	AA13	227	309	8	OLVDS3N	K21	34	46
5	OLVDS2	Y12	228	310	8	OLVDS4	L20	35	47
5	OLVDS2N	Y13	229	311	8	OLVDS4N	K20	36	48
5	REFWest	V11	225	307	8	REFSouth	M18	32	44
5	VCC	R11	230	312	8	VCC	M15	37	49

Table 15-13. LVDS cluster – Channel 5, 6, 7 and 8

		Packages					Packages		
Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352	Cluster	Pin Name	CCGA472/ CLGA472	CQFP256	CQFP352
11	ILVDS5	C13	92	128	2	ILVDS7	K3	156	216
11	ILVDS5N	C12	93	129	2	ILVDS7N	L3	157	217
11	ILVDS6	B13	94	130	2	ILVDS8	K2	158	218
11	ILVDS6N	B12	95	131	2	ILVDS8N	L2	159	219
11	OLVDS5	B11	97	133	2	OLVDS7	M2	161	221
11	OLVDS5N	B10	98	134	2	OLVDS7N	N2	162	222
11	OLVDS6	C11	99	135	2	OLVDS8	M3	163	223
11	OLVDS6N	C10	100	136	2	OLVDS8N	N3	164	224
11	REFEast	E12	96	132	2	REFNorth	L5	160	220
11	VCC	A11	101	137	2	VCC	M4	165	225

16. Electrical Characteristics

16.1 Absolute Maximum Ratings

Table: Absolute rating Itside Supply Voltage I/Os (VCC buffers)……..... -0.3V to +4V Supply Voltage Core (VDD array).....…….....-0.3V to +2V Storage Temperature.....-65°C to +150°C All Output Voltages with respect to Ground..... -0.3V to 4V ESD for I/O ..... > 2000V ESD for LVDS .....> 1000V Junction to Case Thermal resistance (Rjc) – CLGA/CCGA …..... 1°C /W Junction to Case Thermal resistance (Rjc) – CQFP ..... 2°C /W	*Notice: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

16.2 Operating Range

Table 16-1. Operating Range

Operating Temperature	-55°C to +125°C
VCC – IO Power Supply	3.3V ± 0.3V
VCCB - LVDS I/O Power Supply	3.3V ± 0.3V
VREF - LVDS Reference Voltage	1.25 ± 0.1V
VDD - Core Power Supply	1.8V ± 0.15V

16.3 DC characteristics

Table 16-2. DC characteristics

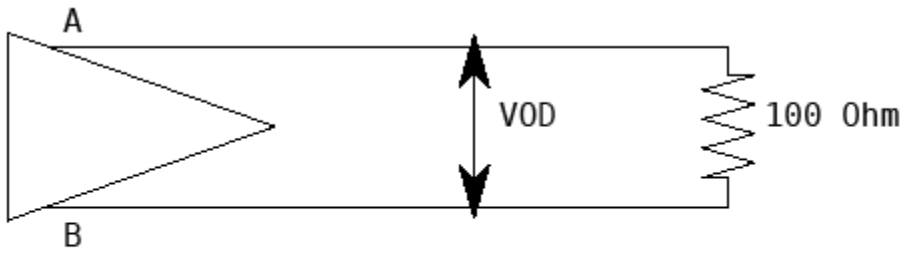
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% Vcc	V
V_{IH}	High-level Input Voltage	CMOS	2.0		Vcc + 0.8V	V
V_{OL}	Low-level Output Voltage	IOL = +4 mA VCC = 3.0V			0.4	V
		IOL = +10 mA VCC = 3.0V			0.4	V
		IOL = +14 mA VCC = 3.0V			0.4	V
V_{OH}	High-level Output Voltage	IOH = -4 mA VCC = 3.0V	Vcc - 0.4V			V
		IOH = -10 mA VCC = 3.0V	Vcc - 0.4V			V
		IOH = -14 mA VCC = 3.0V	Vcc - 0.4V			V
I_{IH}	High-level Input Current	VIN = VCC max	-1		1	µA
		With pull-down, VIN = VCC	20	75	240	µA
I_{IL}	Low-level Input Current	VIN = VSS	-1		1	µA
		With pull-up, VIN = VSS	-500	-100	-20	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, VOUT =VCC max	-1		1	µA
		With pull-down, VOUT = VCC max	20	75	240	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, VOUT = VSS	-1		1	µA
		With pull-up, VOUT = VSS for CON	-220	-108	-60	µA
I_{CCSB1}	Standby Current Consumption	All cells configured - no floating nodes			50	mA
I_{CCSB2}	Standby Current Consumption	Configuration state machine in Idle - cells not configured			200	mA
C_{IN}	Input Capacitance	All pins			10	pF
I_{ICS}	Cold sparing leakage Input current	Vdd = Vss = 0V Vin = 0 to VDD Max	-1		1	µA
I_{OCS}	Cold sparing leakage output current	Vdd = Vss = 0V Vin = 0 to VDD Max	-1		1	µA
V_{CSTH}	Supply threshold of cold sparing buffers	I_{ICS} < 4 µA		0.5		V

16.4 LVDS AC/DC characteristics

Table 16-3. LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Units	Comments
|VOD|	Output differential voltage	Rload = 100Ω	247	454	mV	see Figure below
VOS	Output offset voltage	Rload = 100Ω	1125	1375	mV	see Figure below
|ΔVOD|	Change in VOD between "0" and "1"	Rload = 100Ω	0	50	mV	–
|ΔVOS|	Change in VOS between "0" and "1"	Rload = 100Ω	0	50	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1	6.2	mA	
ISAB	Output current	Drivers shorted together	2.6	4.8	mA	–
F Max.	Maximum operating frequency	VDD = 3.3V ± 0.3V	–	200	MHz	Consumption 20.9 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	445	838	ps	see Figure below
Trise	Rise time 20-80%	Rload = 100Ω	445	841	ps	see Figure below
Tp	Propagation delay	Rload = 100Ω	1120	2120	ps	see Figure below
Tsk1	Duty cycle skew	Rload = 100Ω	0	80	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Figure 16-1. Test Termination Measurments



$$VOS = \frac{(VA + VB)}{2}$$

Figure 16-2. Rise and Fall time measurements

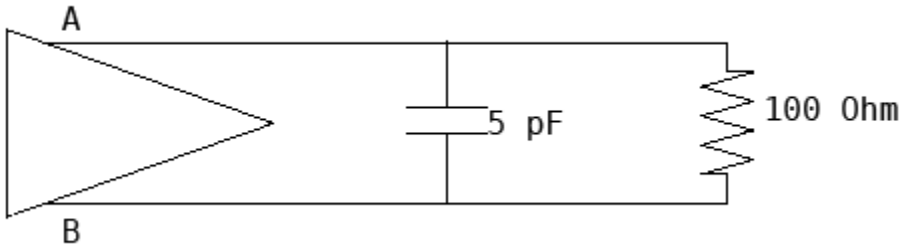


Table 16-4. LVDS Receiver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Units	Comments
VID	Input differential voltage	-	200	600	mV	–
VCM	Input offset range	-	400	2000	mV	–
Tp	Propagation delay	Cout = 50 pF, VDD = 3.3V ± 0.3V	0.7	2.4	Ns	–
Tskew	Duty cycle distortion	Cout = 50 pF	-	500	ps	–

16.5 AC parameters

All the timings are given at the worst case corner.

- All input I/O characteristics measured from V_{IH} of 50% of V_{CC} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}.
- All output I/O characteristics are measured as the average of T_{PDLH} and T_{PDHL} to the pad V_{IH} of 50% of V_{CC}.
- Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
- Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

All the values provided here after are simulation values. They are not measured on production environment.

Table 16-5. Propagation Delay characteristics

Cell Function	Parameter	Path	Value	Units	Notes
IO					
Input 3.3V	t_{PD}	pad -> q	3.6	ns	propagation delay from **pad** to **q**, no extra delay
Input 3.3V	t_{PD}	pad -> q	3.7	ns	propagation delay from **pad** to **q**, extra delay 1
Input 3.3V	t_{PD}	pad -> q	4.1	ns	propagation delay from **pad** to **q**, extra delay 3
Input 3.3V	t_{PD}	pad -> q	4.6	ns	propagation delay from **pad** to **q**, extra delay 5
Output, 3.3V, slow	t_{PD}	a -> pad	7.1	ns	propagation delay from **a** to **pad**, 40 pF load
Output, 3.3V, medium	t_{PD}	a -> pad	6.2	ns	propagation delay from **a** to **pad**, 40 pF load
Output, 3.3V, fast	t_{PD}	a -> pad	6.0	ns	propagation delay from **a** to **pad**, 40 pF load
Output, 3.3V, slow	t_{PD}	oe -> pad	8.2	ns	propagation delay from **oe** to **pad**, 40 pF load
Output, 3.3V, medium	t_{PD}	oe -> pad	7.4	ns	propagation delay from **oe** to **pad**, 40 pF load
Output, 3.3V, fast	t_{PD}	oe -> pad	7.1	ns	propagation delay from **oe** to **pad**, 40 pF load

Table 16-6. Clock – Set/Reset AC characteristics

Function	Parameter	Path	Value	Units	Notes
Global Clocks and Set/Reset					
GCK Input pad at 3.3V	t_{PD}	pad -> clk	9.5	ns	delay from GCKx global clock pad to flop on the rising edge clock
FCK Input pad at 3.3V	t_{PD}	pad -> clk	8	ns	delay from FCKx fast clock pad to flop on the rising edge clock. **Warning:** Flops must be placed on first or last column of the matrix
Reset Input pad at 3.3V	t_{PD}	pad -> sn | rn	10	ns	delay from any pad to the set/reset flop pin

GCK input pad to output pad (3.3V, fast)	t_{PD}	pad -> pad	22	ns	delay from GCKx global clock pad to an output pad loaded at 40pF **Warning:** flop is placed close to the output pad
FCK input pad to output pad (3.3V,fast)	t_{PD}	pad -> pad	20	ns	delay from FCKx fast clock pad to an output pad loaded at 40pF **Warning:** Flops must be placed on first or last column of the matrix

Table 16-7. FreeRam™ AC characteristics – Asynchronous mode

Async RAM					
Write	T_{WEL}, T_{WEH}	we	1.7	ns	**we** min pulse width high or low
Write	T_{AWS}	we -> ain | a	4.2	ns	setup time of address input before **low** transition at the **we** input
Write	T_{AWH}	we -> ain | a	1.7	ns	hold time of address input before **high** transition at the **we** input
Write	T_{DS}	we -> din | d	0	ns	setup time of data input before **rising** transition at the **we** input
Write	T_{DH}	we -> din | d	0	ns	hold time of data input before **rising** transition at the **we** input
Write /Read	T_{DD}	din -> dout	6.4	ns	propagation delay between **din** and **dout** on double port ram when **ain** = **aout**
Read	T_{AD}	ain -> dout	4.9	ns	propagation delay from **ain** to **dout**
Read	T_{OZX}	oe -> dout	2.9	ns	propagation delay from **oe** to **dout** for a transition from z to 0|1
Read	T_{OXZ}	oe -> dout	2.9	ns	propagation delay from **oe** to **dout** for a transition from 0|1 to z

Figure 16-3. Single-port Write/Read

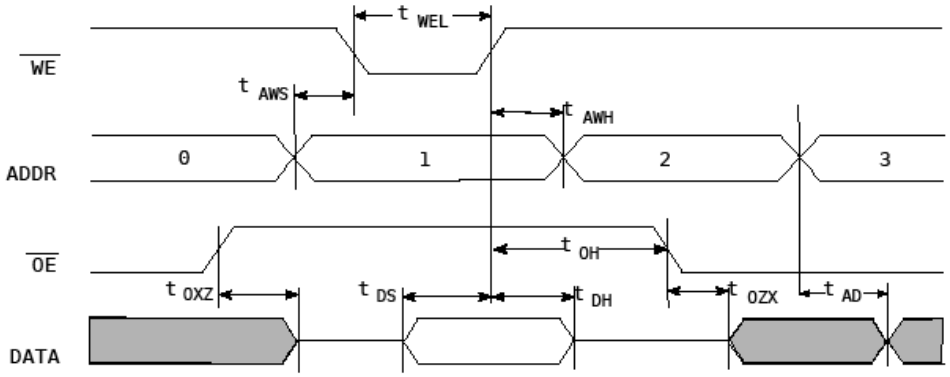


Figure 16-4. Dual-port Write with Read

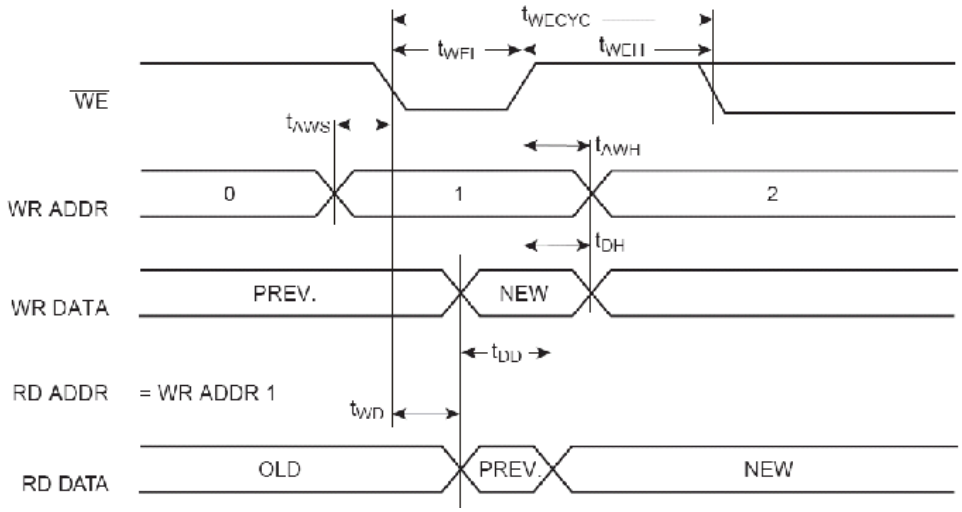


Figure 16-5. Dual-port Read

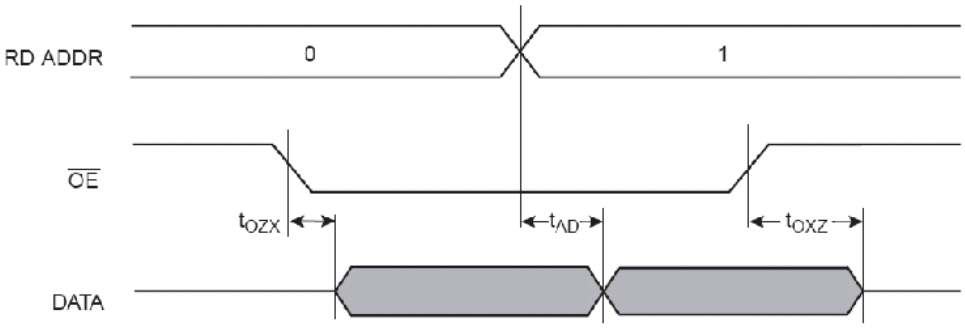


Table 16-8. FreeRam™ AC characteristics – Synchronous mode

Sync RAM					
Write	t_{CLKL}, t_{CLKH}	clk	1.2	ns	**ck** min pulse width high or low
Write	t_{WCS}	clk -> we	2.7	ns	setup time of **we** input before active transition at the clk input
Write	t_{WCH}	clk -> we	0	ns	hold time of **we** input before active transition at the clk input
Write	t_{ACS}	clk -> ain | a	3.2	ns	setup time of adress input before active transition at the **clk** input
Write	t_{ACH}	clk -> ain | a	3.3	ns	hold time of adress input before active transition at the **clk** input
Write	t_{DCS}	clk -> din | d	1.5	ns	setup time of data input before active transition at the **clk** input
Write	t_{DCH}	clk -> din | d	0	ns	hold time of data input before active transition at the **clk** input
Write/Read	t_{CD}	clk -> dout	5.8	ns	propagation delay from **clk** to **dout**
Read	t_{AD}	aout -> dout	4.9	ns	propagation delay from **aout** to **dout**
Read	t_{OZX}	oe -> dout	2.9	ns	propagation delay from **oe** to **dout** for a transition from z to 0|1
Read	t_{OXZ}	oe -> dout	2.9	ns	propagation delay from **oe** to **dout** for a transition from 0|1 to z

Figure 16-6. Single-port Write/Read

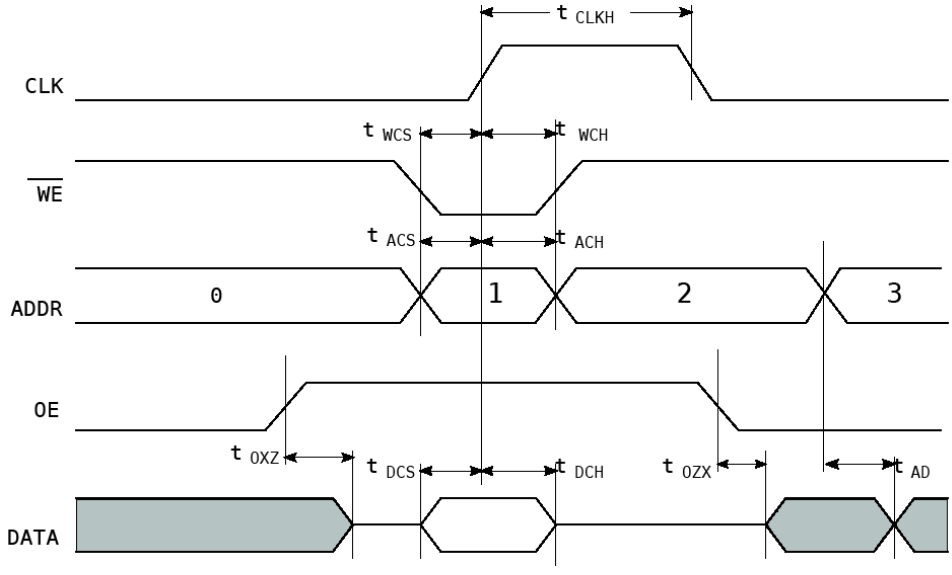


Figure 16-7. Dual-port Write with Read

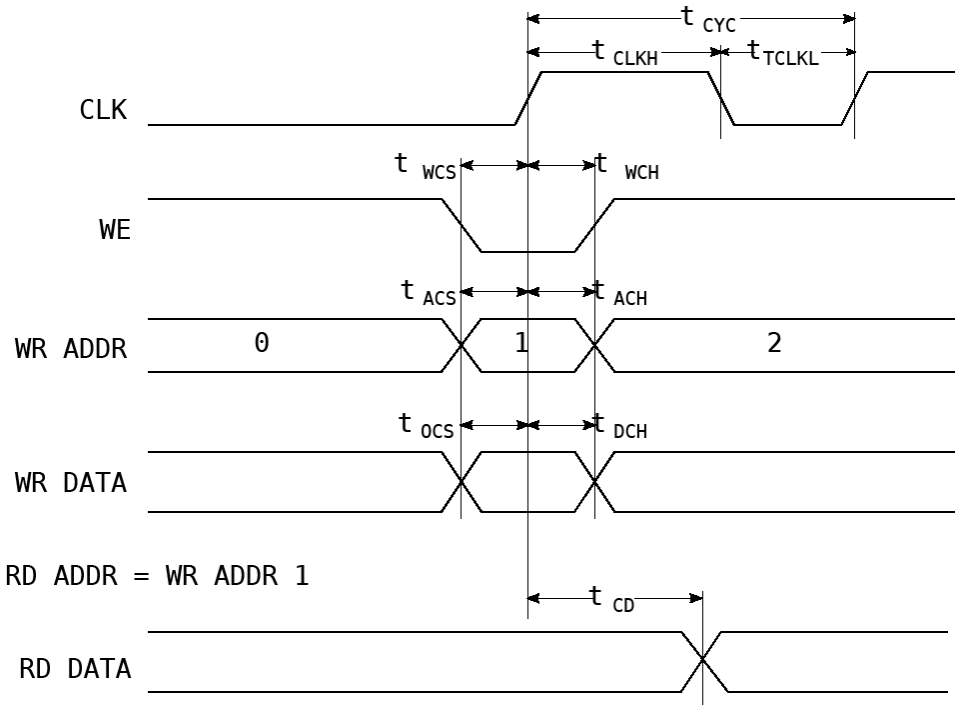
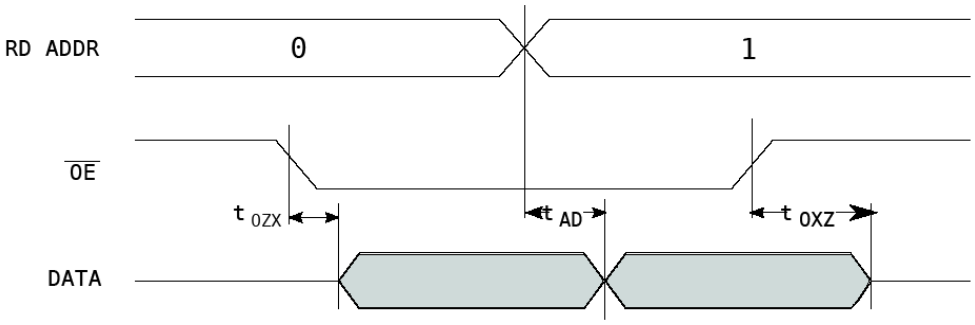


Figure 16-8. Dual-port Read



17. Ordering Information

17.1 ATF280F Ordering Codes

Atmel Ordering Code	Package Type	IO pins	Temperature Range	Quality Level
ATF280F-2J-E	CCGA472	308+32	25°C	Engineering Samples
ATF280F-2V-E	CLGA472	308+32	25°C	Engineering Samples
ATF280F-YF-E	CQFP352	249+32	25°C	Engineering Samples
ATF280F-YJ-E	CQFP256	148+32	25°C	Engineering Samples
5962-1222501QXB	CCGA472	308+32	-55°C / +125°C	QMLQ
5962-1222501QYC	CLGA472	308+32	-55°C / +125°C	QMLQ
5962-1222501QZC	CQFP352	249+32	-55°C / +125°C	QMLQ
5962-1222501QUC	CQFP256	148+32	-55°C / +125°C	QMLQ
5962-1222501VXB	CCGA472	308+32	-55°C / +125°C	QMLV
5962-1222501VYC	CLGA472	308+32	-55°C / +125°C	QMLV
5962-1222501VZC	CQFP352	249+32	-55°C / +125°C	QMLV
5962-1222501VUC	CQFP256	148+32	-55°C / +125°C	QMLV
5962R1222501VXB	CCGA472	308+32	-55°C / +125°C	QMLV RHA
5962R1222501VYC	CLGA472	308+32	-55°C / +125°C	QMLV RHA
5962R1222501VZC	CQFP352	249+32	-55°C / +125°C	QMLV RHA
5962R1222501VUC	CQFP256	148 +32	-55°C / +125°C	QMLV RHA

17.2 ATF280F Evaluation Kit Ordering Codes

Atmel Ordering Code	Description
ATF280-EK	Evaluation Kit for ATF280

18. Revision History

Doc. Rev.	Date	Comments
7750H	11/2015	[Configuration Interface]: - INIT pin description updated. [Pin Assignment]: - Table 15-3. Core Power and Ground Cluster [Errata]: - Chapter added regarding JTAG issues. Non functionality of the JTAG feature and active polarity of the TRST pin.
7750G	07/2014	[Bitstream Structure]: - Missing referenced not added [Configuration Download][Configuration Integrity Management]: - Diagram corrected regarding CCLK mapping. - Differenciation between mode 1 and 7 added in mode highlights [FreeRamTM]: - SET hardened information added [JTAG]: - Erroneous reference to ATFS450 removed - Figure 13.1 erroneours reference corrected [Pin Assignment]: - Table 15-11. IO cluster 12 corrected [DC characteristics]: - Table 16-2. DC characteristics corrected [LVDS AC/DC characteristics]: - Table 16-4. LVDS Receiver DC/AC Characteristics corrected [Ordering Information]: - Part numbers updated according to SMD [Overall]: - Template updated - 80 Mev replaced by 95 Mev
7750F	08/2012	Add thermal resistance for all packages Add SMD part numbers
7750E	04/2012	Full Rework Majors : Configuration Mode Description, Configuration Integrity Check Following pin names corrected IO303_INIT, IO259_LDC, IO265_HDC, IO720_GCK6_CS0, IO655_CHECKN, IO225_OTSN, IO743_A2_CS1 in the whole document, Typography errors corrected through the whole document. New Template
7750D	10/2010	Initial document release

19. Errata

19.1 Erratum 1: JTAG functionality

Issue: **JTAG functionality is not operational on the ATF280.**

This erratum concerned following chapters:

- Chapter 3.6 JTAG.
- Chapter 8.5.3 JTAG compliance.
- Chapter 13 JTAG.

Workaround: In order to completely deactivate the JTAG functionality in the final application whatever the configuration state, the following steps shall be performed:

- TCK, TDI and TMS input pins shall be tied to a high level.
- Configuration bit CR5 [JTAG disable] shall be tied to a high level.

19.2 Erratum 2: TRST JTAG pin

Issue: **TRST JTAG pin polarity is active high.**

This erratum councerned following chapters:

- Chapter 2.5 JTAG.

Workaround: JTAG standard requires the TRST pin be active low if implemented. ATF280 TRST JTAG pin is active high and has an internal pull-down. In other words, to maintain an active reset on JTAG tap, a pull-up with a much lower resistor value than the internal pulled-down shall be applied if bit CR5 is not tied to a high level by the application.

In order to completely deactivate the JTAG functionality in the final application whatever the configuration state, the following steps shall be performed:

- TRST input pins shall be tied to a high level.

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan G.K.
16F Shin-Osaki Kangyo Bldg.
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
Tel: (+81)(3) 6417-0300
Fax: (+81)(3) 6417-0370