ATtiny828

8-bit AVR Microcontroller
with 8K Bytes In-System Programmable Flash

DATASHEET APPENDIX B

Appendix B – ATtiny828 Specification at 125°C

This document contains information specific to devices operating at temperatures up to 125°C. Only deviations are covered in this appendix, all other information can be found in the complete datasheet. The complete datasheet can be found at www.atmel.com.

1. Memories

The EEPROM has an endurance of at least 50,000 write/erase cycles.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{RESET}$ with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on $\overline{RESET}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 DC Characteristics

Table 1. DC Characteristics. T = -40°C to +125°C

Symbol	Parameter	Condition	Min	Typ [1]	Max	Units
V_{IL}	Input Low Voltage	V_{CC} = 1.8V – 2.4V V_{CC} = 2.4V – 5.5V	-0.5		$0.2V_{CC}$[3] $0.3V_{CC}$[3]	V
V_{IH}	Input High-voltage Except $\overline{RESET}$ pin	V_{CC} = 1.8V – 2.4V V_{CC} = 2.4V – 5.5V	$0.7V_{CC}$[2] $0.6V_{CC}$[2]		V_{CC} +0.5	V
	Input High-voltage $\overline{RESET}$ pin	V_{CC} = 1.8V to 5.5V	$0.9V_{CC}$[2]		V_{CC} +0.5	V
V_{OL}	Output Low Voltage [4] $\overline{RESET}$ pin as I/O [6]	V_{CC} = 5V, I_{OL} = 2 mA [5]			0.6	V
		V_{CC} = 3V, I_{OL} = 1 mA[5]			0.5	
		V_{CC} = 1.8V, I_{OL} = 0.4mA[5]			0.4	
	Output Low Voltage [4] Standard Sink I/O Pin [7]	V_{CC} = 5V, I_{OL} = 10 mA [5]			0.6	
		V_{CC} = 3V, I_{OL} = 5 mA [5]			0.5	
		V_{CC} = 1.8V, I_{OL} = 2mA [5]			0.4	
	Output Low Voltage [4] High Sink I/O Pin [8]	V_{CC} = 5V, I_{OL} = 20 mA [5]			0.7	
		V_{CC} = 3V, I_{OL} = 10 mA[5]			0.6	
		V_{CC} = 1.8V, I_{OL} = 4mA [5]			0.5	
	Output Low Voltage [4] Extra High Sink I/O Pin [9]	V_{CC} = 5V, I_{OL} = 20 mA [5]			0.7	
		V_{CC} = 3V, I_{OL} = 20 mA [5]			0.7	
		V_{CC} = 1.8V, I_{OL} = 8mA[5]			0.6	

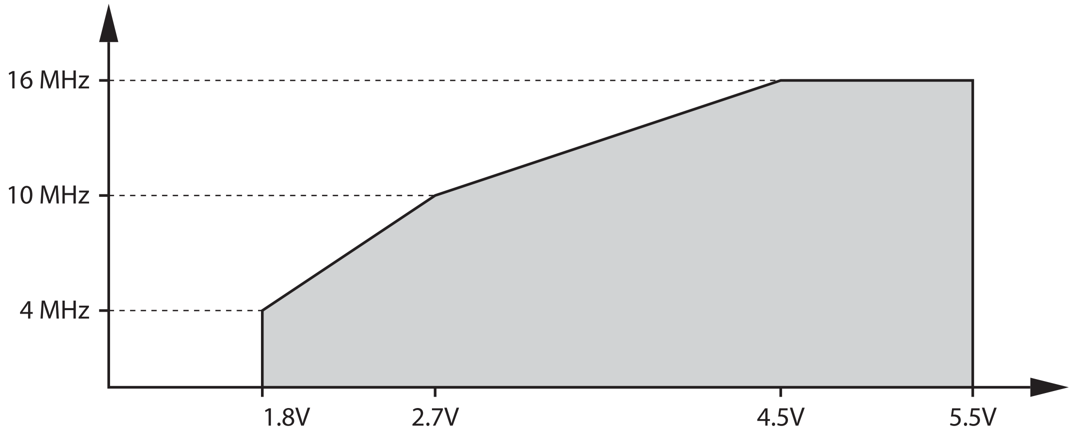
Symbol	Parameter	Condition	Min	Typ [1]	Max	Units
V_{OH}	Output High-voltage[4] Except $\overline{\text{RESET}}$ pin[6]	V_{CC} = 5V, I_{OH} = -10 mA [5]	4.3			V
		V_{CC} = 3V, I_{OH} = -5 mA [5]	2.5			
		V_{CC} = 1.8V, I_{OH} = -2 mA [5]	1.4			
I_{LIL}	Input Leakage Current, I/O Pin (absolute value)	V_{CC} = 5.5V, pin low		<0.05	1	µA
I_{LIH}	Input Leakage Current, I/O Pin (absolute value)	V_{CC} = 5.5V, pin high		<0.05	1	µA
I_{LIAC}	Input Leakage Current, Analog Comparator	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
R_{RST}	Reset Pull-up Resistor	V_{CC} = 5.5V, input low	30		60	kΩ
R_{PU}	I/O Pin Pull-up Resistor	V_{CC} = 5.5V, input low	20		50	kΩ
I_{CC}	Power Supply Current[10]	Active 1 MHz, V_{CC} = 2V		0.2	0.4	mA
		Active 4 MHz, V_{CC} = 3V		1.2	2	mA
		Active 8 MHz, V_{CC} = 5V		3.9	5	mA
		Idle 1 MHz, V_{CC} = 2V		0.03	0.1	mA
		Idle 4 MHz, V_{CC} = 3V		0.2	0.4	mA
		Idle 8 MHz, V_{CC} = 5V		0.9	1.5	mA
	Power-down mode[11]	WDT enabled, V_{CC} = 3V		1.8	15	µA
		WDT disabled, V_{CC} = 3V		0.1	10	µA

Notes:
1. Typical values at 25°C.
2. “Min” means the lowest value where the pin is guaranteed to be read as high.
3. “Max” means the highest value where the pin is guaranteed to be read as low.
4. Under steady-state (non-transient) conditions I/O ports can sink/source more current than the test conditions, however, the sum current of PORTA and PORTB mustn’t exceed 100mA. Also, the sum current of PORTC and PORTD mustn’t exceed 120mA. V_{OL}/V_{OH} is not guaranteed to meet specifications if pin or port currents exceed the limits given.
5. Pins are not guaranteed to sink/source currents greater than those listed at the given supply voltage.
6. The $\overline{\text{RESET}}$ pin must tolerate high voltages when entering and operating in programming modes and, as a consequence, has a weak drive strength as compared to regular I/O pins. See “Reset Pin as I/O” on page 27, and “Reset Pin as I/O” on page 33.
7. Ports with standard sink strength: PORTD0, PORTD3.
8. Ports with high sink strength: PORTA[7:0], PORTB[7:0], PORTC[7:0], PORTD1.
9. Ports with extra high strength: PORTC[7:0].
10. Results obtained using external clock and methods described in “Minimizing Power Consumption”. Power reduction fully enabled (PRR = 0xFF) and with no I/O drive.
11. BOD Disabled.

2.3 Speed

The maximum operating frequency of the device is dependent on supply voltage, V_{CC} . The relationship between supply voltage and maximum operating frequency is piecewise linear, as shown in Figure 1.

Figure 1. Maximum Operating Frequency vs. Supply Voltage



2.4 Clock Characteristics

2.4.1 Accuracy of Calibrated Internal Oscillator

Table 2. Calibration Accuracy of Internal 8MHz Oscillator

Calibration Method	Target Frequency	V_{CC}	Temperature	Accuracy [1]
Factory Calibration	8.0 MHz	3V	25°C	±2% [2] ±10% [2]
User Calibration [3]	Within: 7.3 – 8.1 MHz	Within: 1.8V – 5.5V	Within: -40°C to +125°C	±1%

Notes: 1. Accuracy of oscillator frequency at calibration point (fixed temperature and voltage).
2. See device ordering codes on page 45 for alternatives.
3. Not available in ATtiny828R devices.

2.4.2 Accuracy of Calibrated 32kHz Oscillator

Table 3. Calibration Accuracy of Internal 32kHz Oscillator

Calibration Method	Target Frequency	V_{CC}	Temperature	Accuracy
Factory Calibration	32kHz	1.8 – 5.5V	-40°C to +125°C	±35%

2.4.3 External Clock Drive

Table 4. External Clock Drive Characteristics

Symbol	Parameter	V_{CC} = 1.8 – 5.5V		V_{CC} = 2.7–5.5V		V_{CC} = 4.5–5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$1/t_{CLCL}$	Clock Frequency	0	4	0	8	0	12	MHz
t_{CLCL}	Clock Period	250		125		83		ns
t_{CHCX}	High Time	100		40		20		ns
t_{CLCX}	Low Time	100		40		20		ns
t_{CLCH}	Rise Time		2.0		1.6		0.5	µs
t_{CHCL}	Fall Time		2.0		1.6		0.5	µs
Δt_{CLCL}	Period change from one clock cycle to next		2		2		2	%

2.5 System and Reset Characteristics

2.5.1 Power-On Reset

Table 5. Characteristics of Enhanced Power-On Reset. T_A = -40 to +125°C

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Units
V_{POR}	Release threshold of power-on reset [2]	1.1	1.4	1.7	V
V_{POA}	Activation threshold of power-on reset [3]	0.6	1.3	1.7	V
SR_{ON}	Power-On Slope Rate	0.01			V/ms

Note: 1. Values are guidelines, only
2. Threshold where device is released from reset when voltage is rising
3. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling)

2.6 Temperature Sensor

Table 6. Accuracy of Temperature Sensor at Factory Calibration

Symbol	Parameter	Condition	Min	Typ	Max	Units
A_{TS}	Accuracy	V_{CC} = 4.0, T_A = 25°C – 125°C		10		°C

Note: 1. Firmware calculates temperature based on factory calibration value.
2. Min and max values are not guaranteed. Contact your local Atmel sales office if higher accuracy is required.

2.7 ADC Characteristics

Table 7. ADC Characteristics. T = -40°C to +125°C. V_{CC} = 1.8 – 5.5V

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution				10	Bits
	Absolute accuracy (Including INL, DNL, and Quantization, Gain and Offset Errors)	$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz		2		LSB
		$V_{REF} = V_{CC}$ = 4V, ADC clock = 1 MHz		3		LSB
		$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz Noise Reduction Mode		1.5		LSB
		$V_{REF} = V_{CC}$ = 4V, ADC clock = 1 MHz Noise Reduction Mode		2.5		LSB
	Integral Non-Linearity (INL) (Accuracy after Offset and Gain Calibration)	$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz		1		LSB
	Differential Non-linearity (DNL)	$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz		0.5		LSB
	Gain Error	$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz		2.5		LSB
	Offset Error	$V_{REF} = V_{CC}$ = 4V, ADC clock = 200 kHz		1.5		LSB
	Conversion Time	Free Running Conversion	13		260	µs
	Clock Frequency		50		1000	kHz
V_{IN}	Input Voltage		GND		V_{REF}	V
	Input Bandwidth			38.5		kHz
R_{AIN}	Analog Input Resistance			100		MΩ
	ADC Conversion Output		0		1023	LSB

2.8 Analog Comparator Characteristics

Table 8. Analog Comparator Characteristics, T = -40°C to +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{AIO}	Input Offset Voltage	V_{CC} = 5V, VIN = V_{CC} / 2		< 10	40	mV
I_{LAC}	Input Leakage Current	V_{CC} = 5V, VIN = V_{CC} / 2	-50		50	nA
t_{APD}	Analog Propagation Delay (from saturation to slight overdrive)	V_{CC} = 2.7V		750		ns
		V_{CC} = 4.0V		500		
	Analog Propagation Delay (large step change)	V_{CC} = 2.7V		100		
		V_{CC} = 4.0V		75		
t_{DPD}	Digital Propagation Delay	V_{CC} = 1.8V – 5.5		1	2	CLK

2.9 Serial Programming Characteristics

Table 9. Serial Programming Characteristics, T = -40°C to +125°C, V_{CC} = 1.8 – 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		4	MHz
t_{CLCL}	Oscillator Period	250			ns
$1/t_{CLCL}$	Oscillator Freq. (V_{CC} = 4.5V - 5.5V)	0		16	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.5V - 5.5V)	62.5			ns
t_{SHSL}	SCK Pulse Width High	2 t_{CLCL} [1]			ns
t_{SLSH}	SCK Pulse Width Low	2 t_{CLCL} [1]			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns

Note: 1. 2 t_{CLCL} for f_{ck} < 12MHz, 3 t_{CLCL} for f_{ck} >= 12 MHz

3. Typical Characteristics

3.1 Current Consumption in Active Mode

Figure 2. Active Supply Current vs. Frequency (1 - 16 MHz)

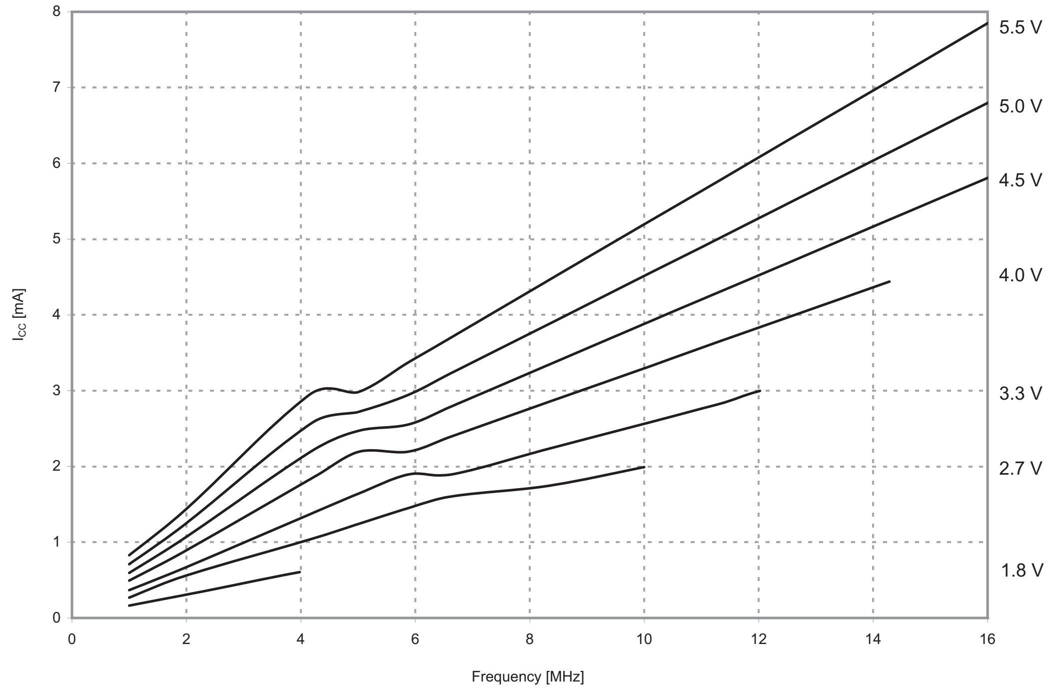


Figure 3. Active Supply Current vs. V_{CC} (Internal Oscillator, 8 MHz)

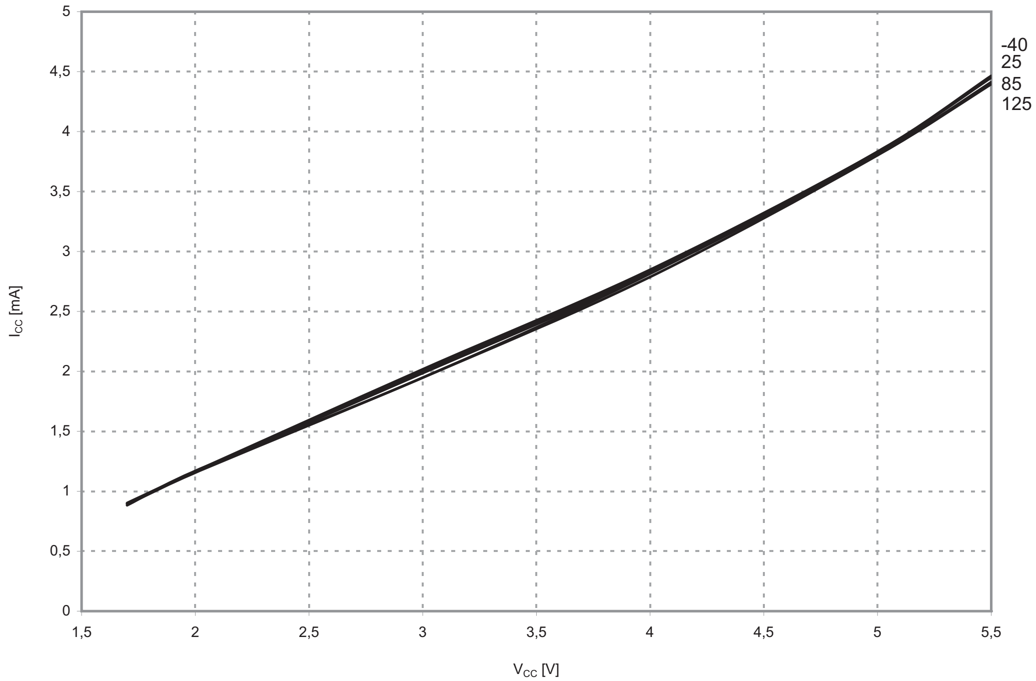


Figure 4. **Active Supply Current vs. V_{CC} (Internal Oscillator, 1 MHz)**

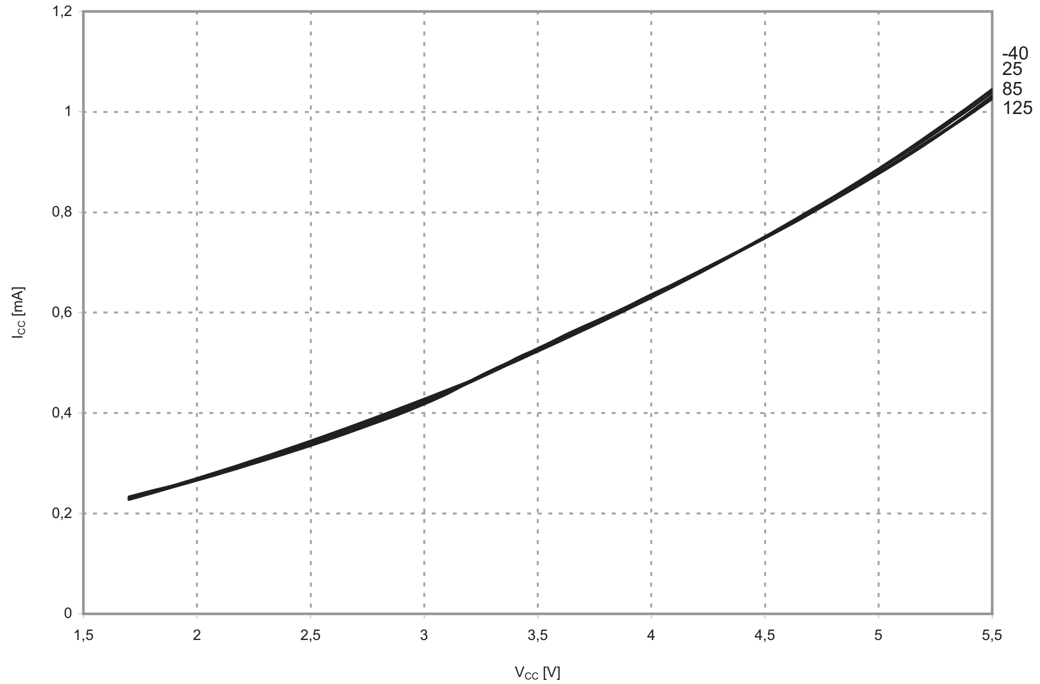
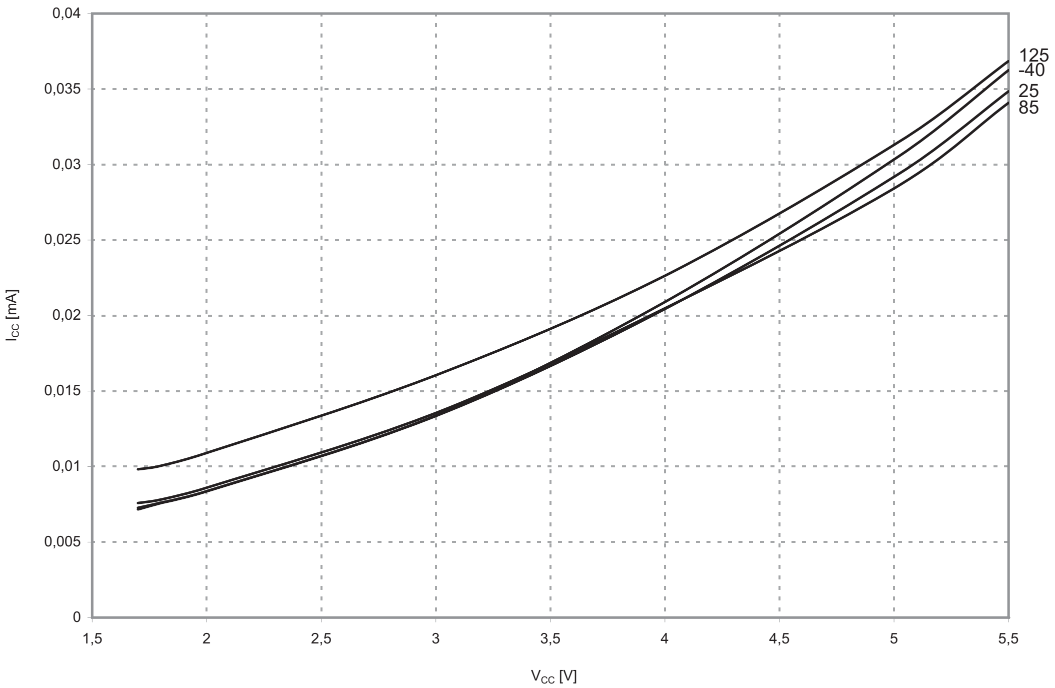


Figure 5. **Active Supply Current vs. V_{CC} (Internal Oscillator, 32kHz)**



3.2 Current Consumption in Idle Mode

Figure 6. Idle Supply Current vs. Frequency (1 - 16 MHz)

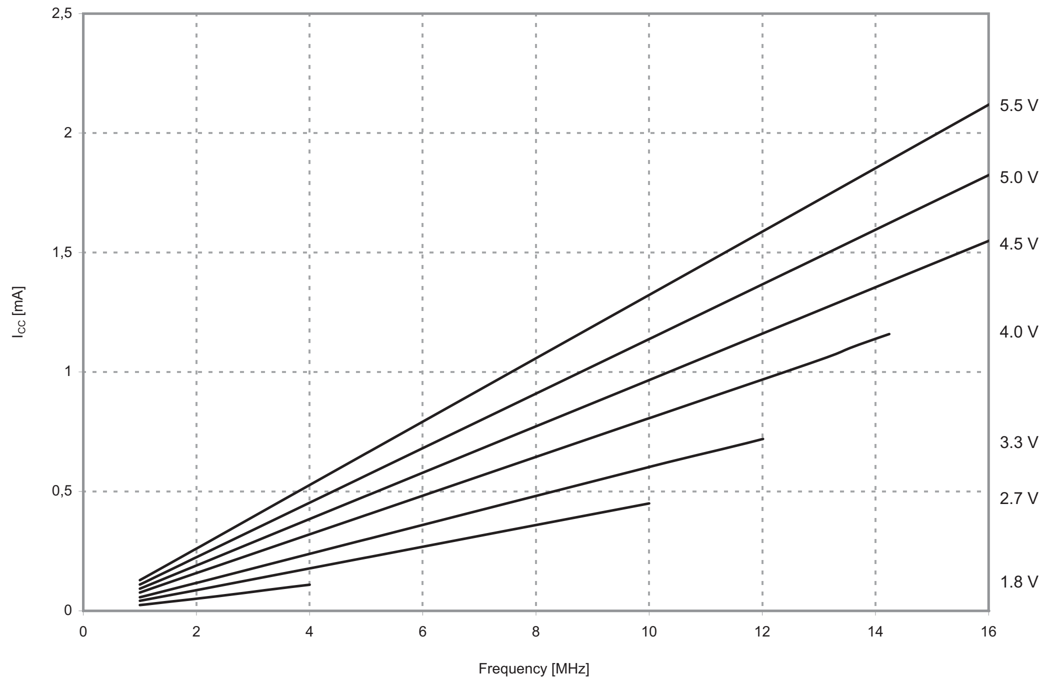


Figure 7. Idle Supply Current vs. V_{CC} (Internal Oscillator, 8 MHz)

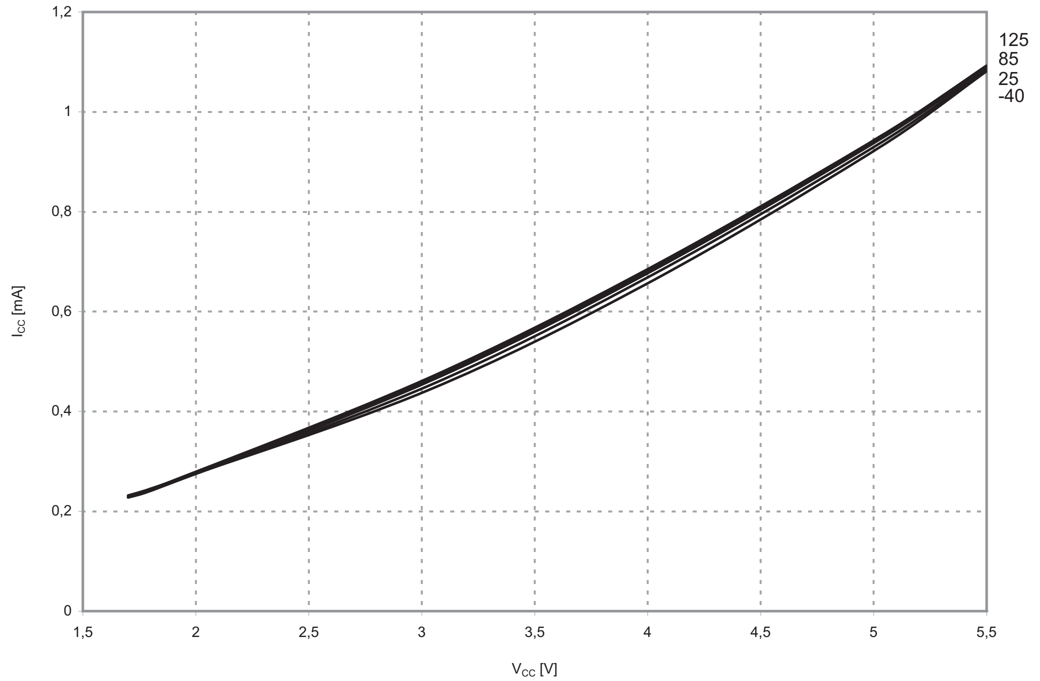


Figure 8. Idle Supply Current vs. V_{CC} (Internal Oscillator, 1 MHz)

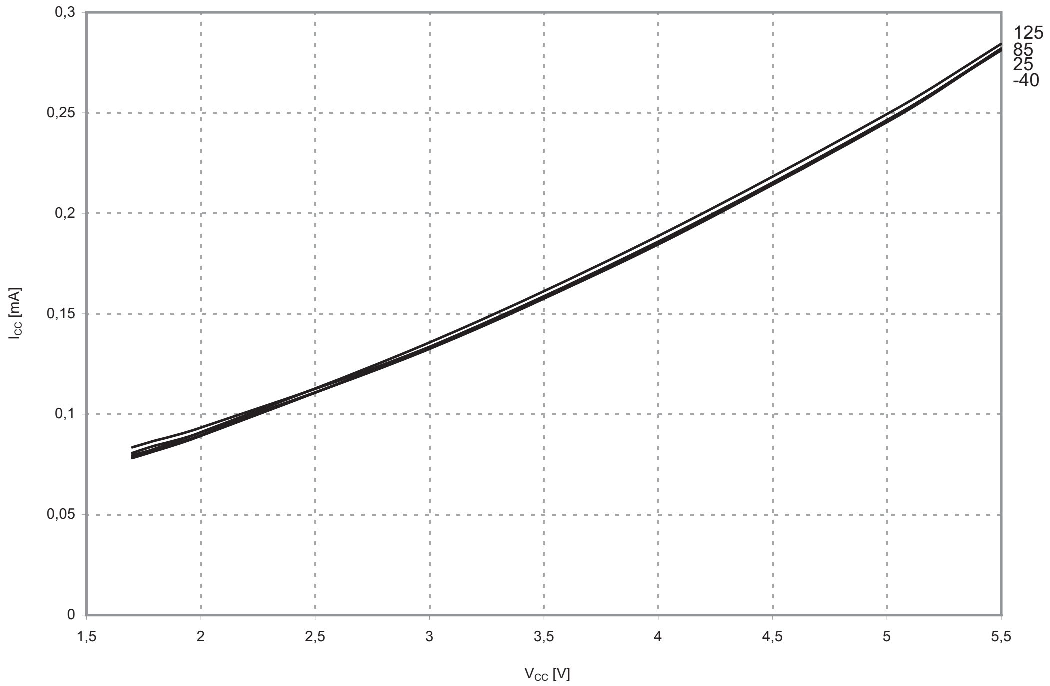
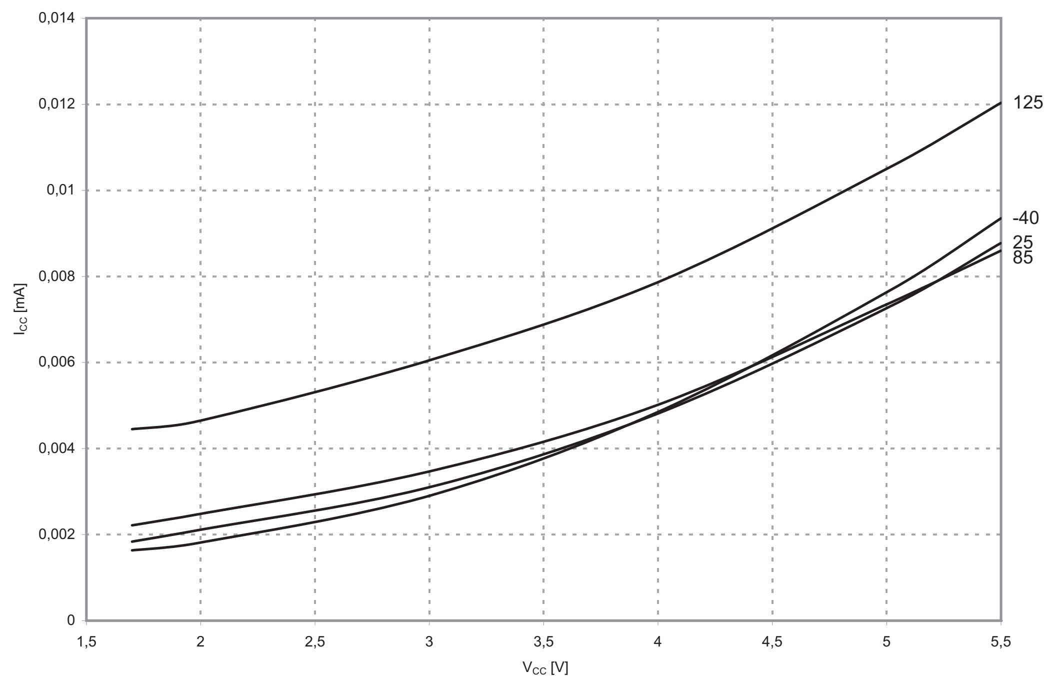


Figure 9. Idle Supply Current vs. V_{CC} (Internal Oscillator, 32kHz)



3.3 Current Consumption in Power-down Mode

Figure 10. Power-down Supply Current vs. V_{CC} (Watchdog Timer Disabled)

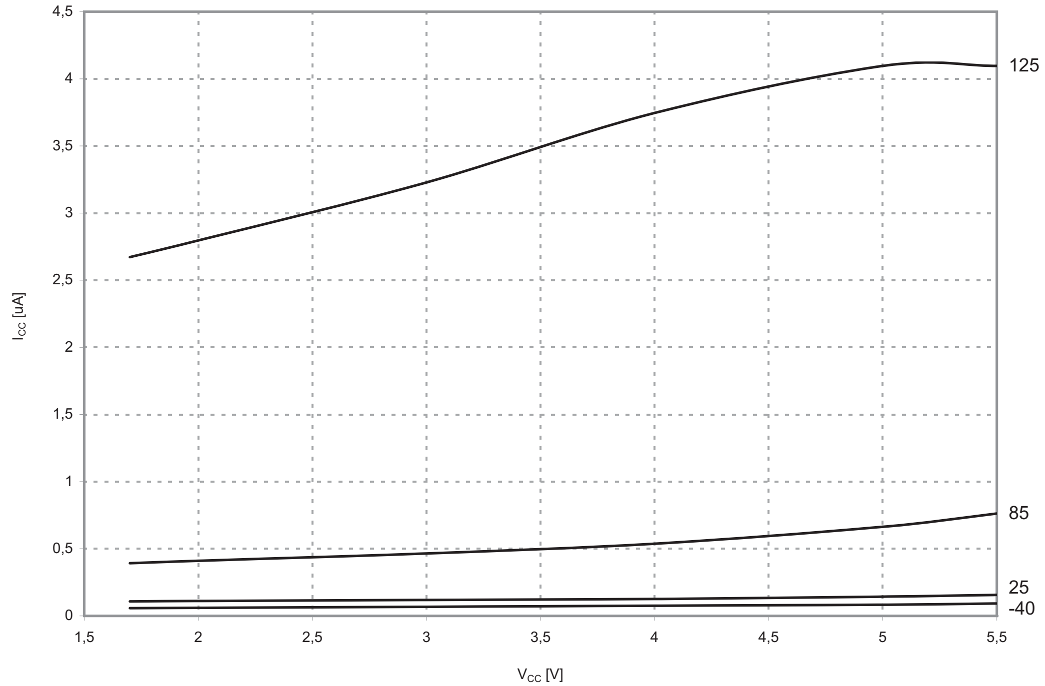
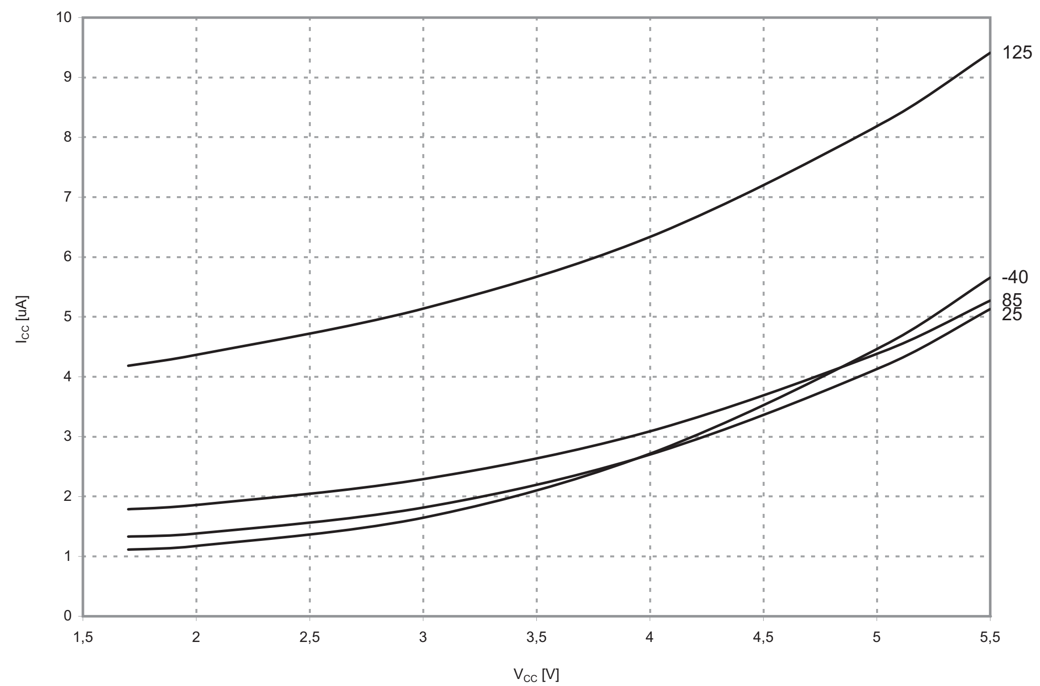


Figure 11. Power-down Supply Current vs. V_{CC} (Watchdog Timer Enabled)



3.4 Current Consumption in Reset

Figure 12. Reset Current vs. Frequency (1 – 16MHz, Excluding Pull-Up Current)

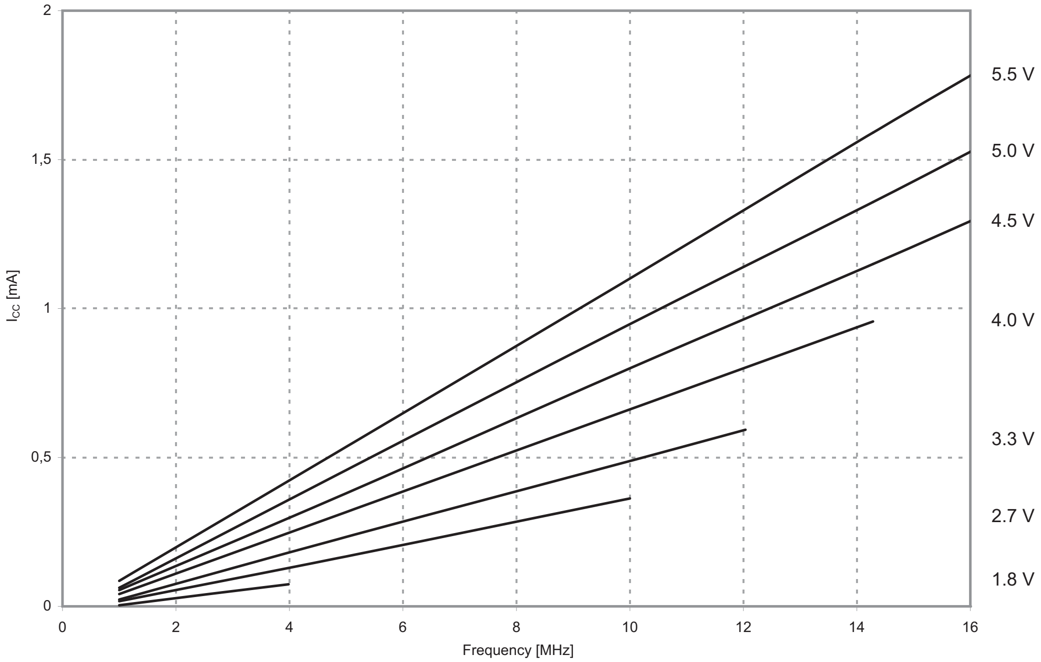
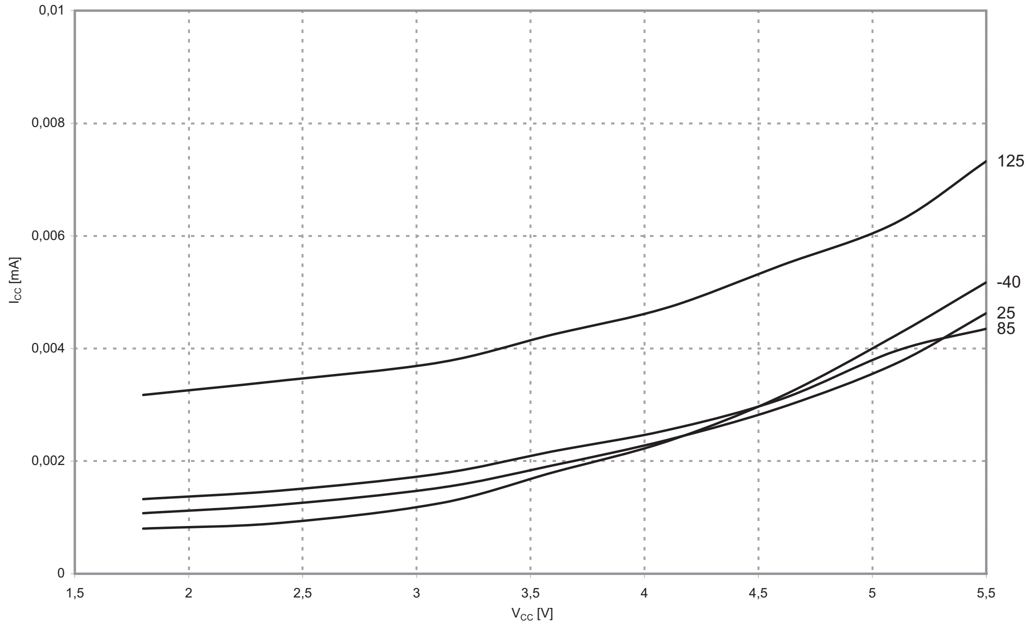


Figure 13. Reset Current vs. V_{CC} (No Clock, excluding Reset Pull-Up Current)



3.5 Current Consumption of Peripheral Units

Figure 14. Watchdog Timer Current vs. V_{CC}

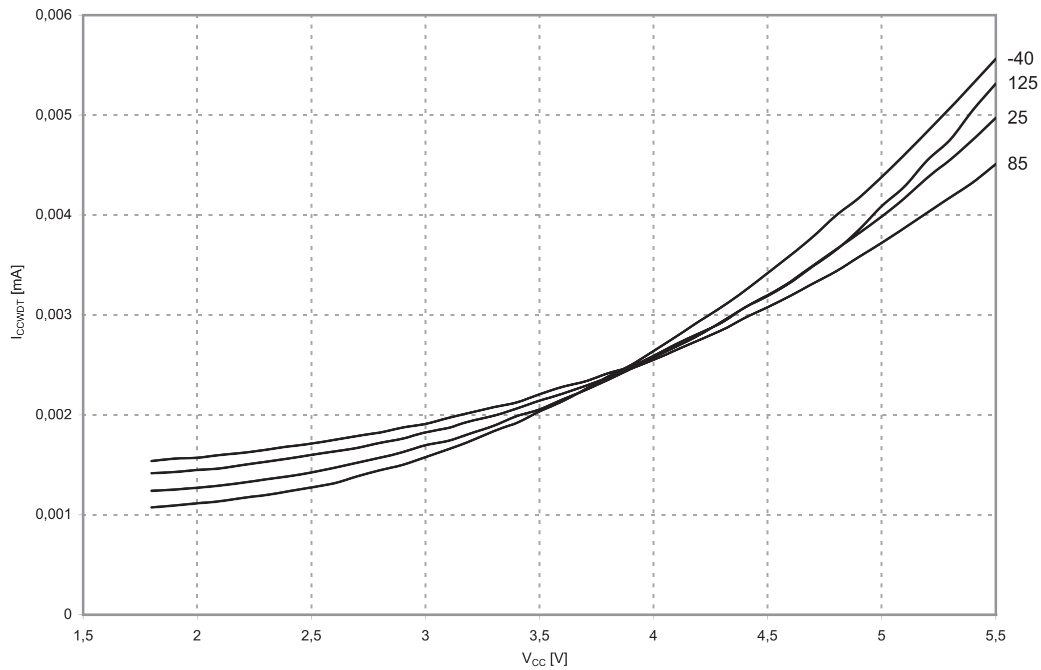


Figure 15. Brownout Detector Current vs. V_{CC}

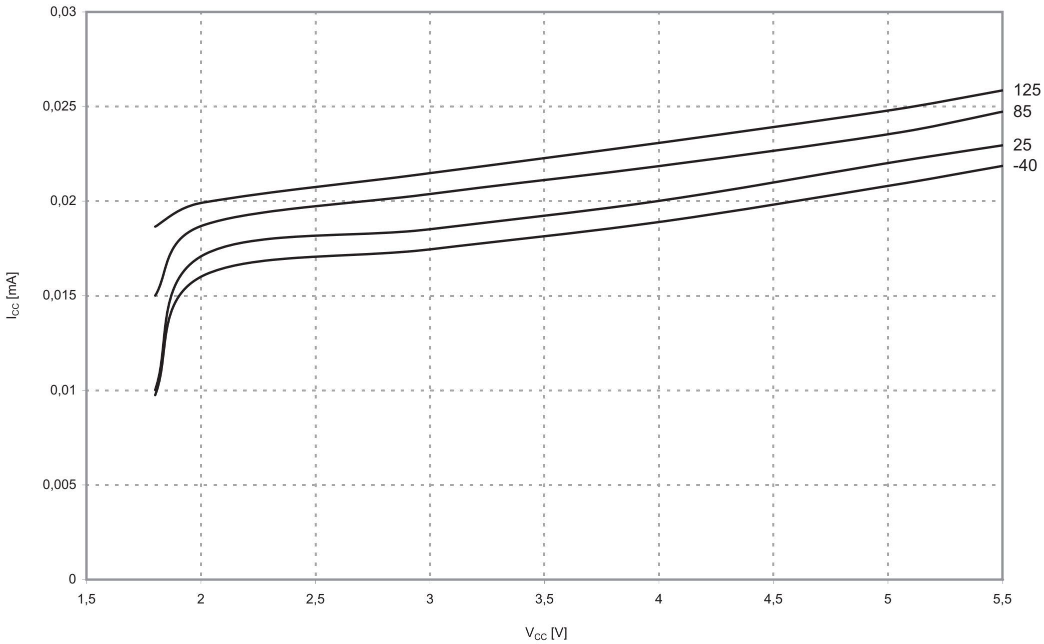
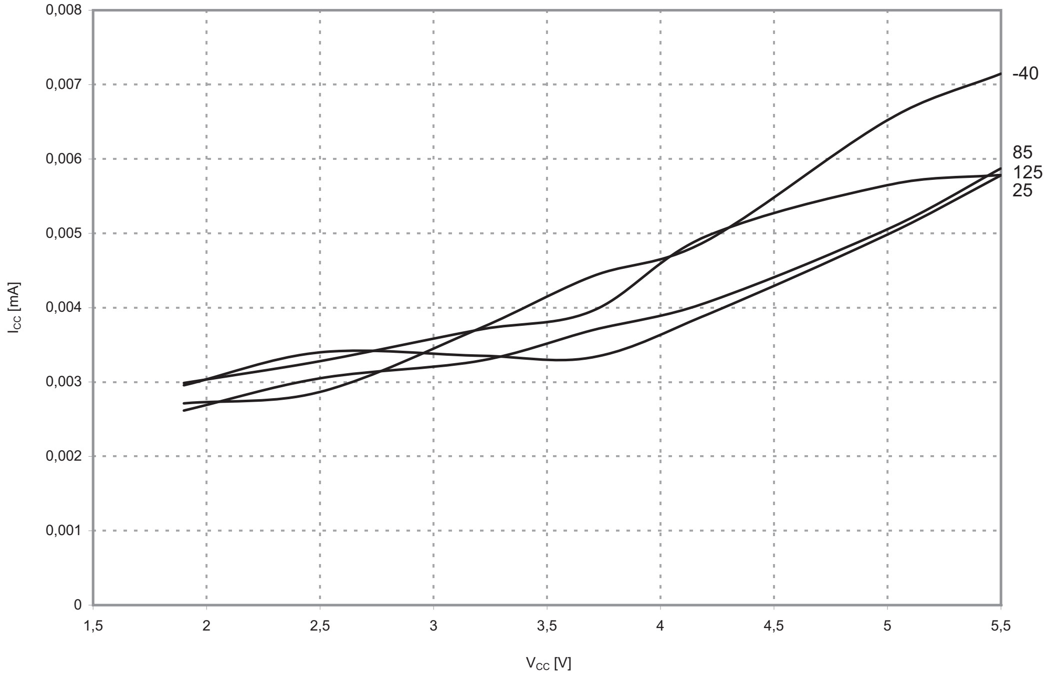


Figure 16. Sampled Brownout Detector Current vs. V_{CC}



3.6 Pull-up Resistors

3.6.1 I/O Pins

Figure 17. I/O pin Pull-up Resistor Current vs. Input Voltage (V_{CC} = 1.8V)

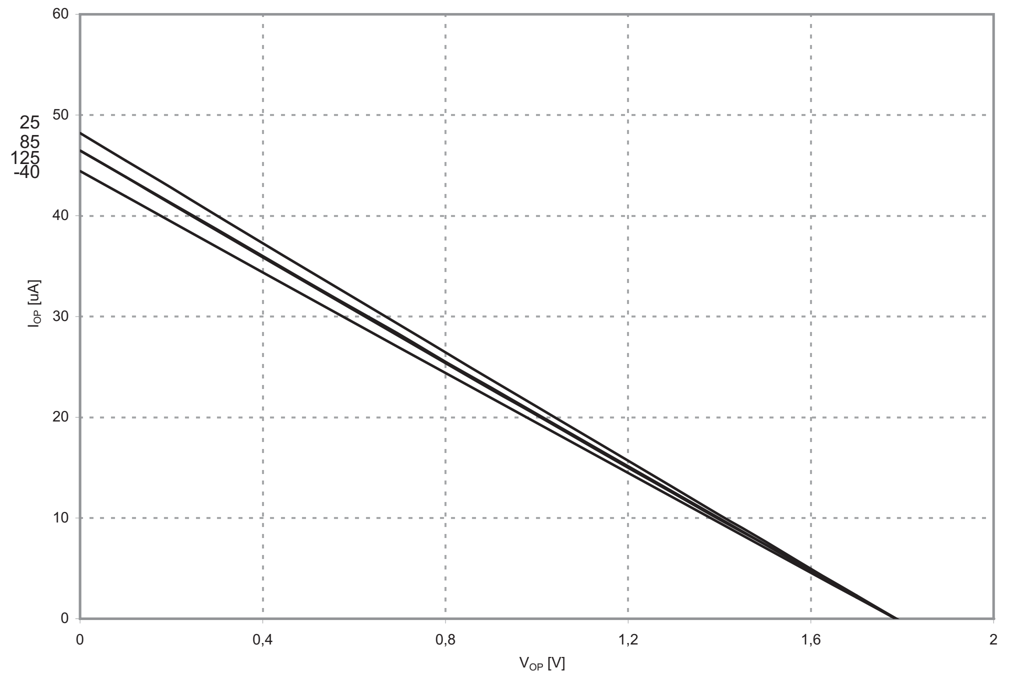


Figure 18. I/O Pin Pull-up Resistor Current vs. input Voltage (V_{CC} = 2.7V)

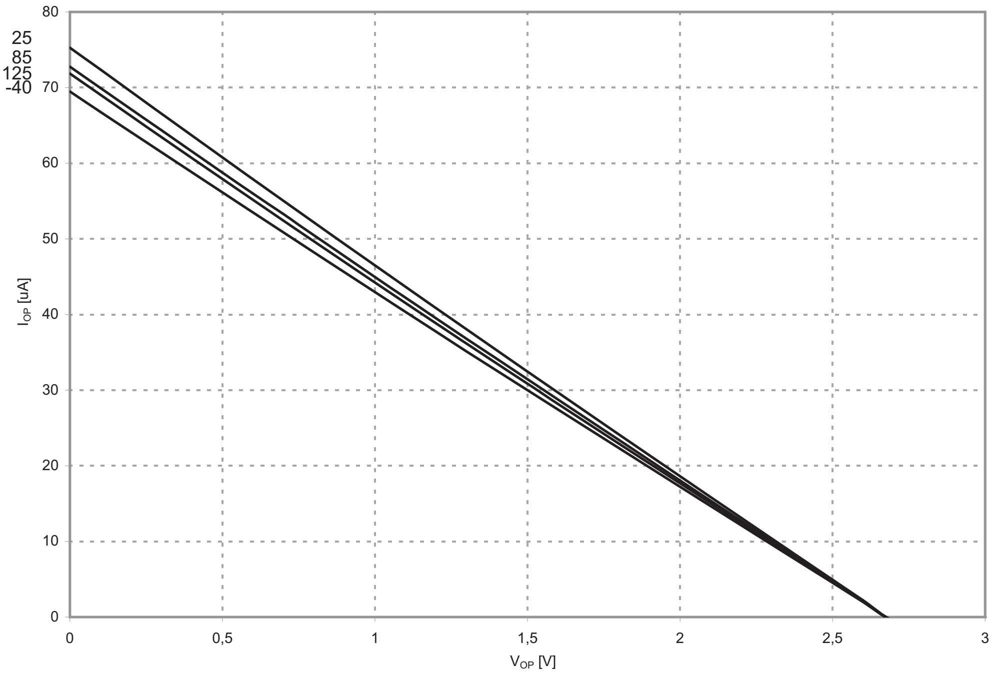
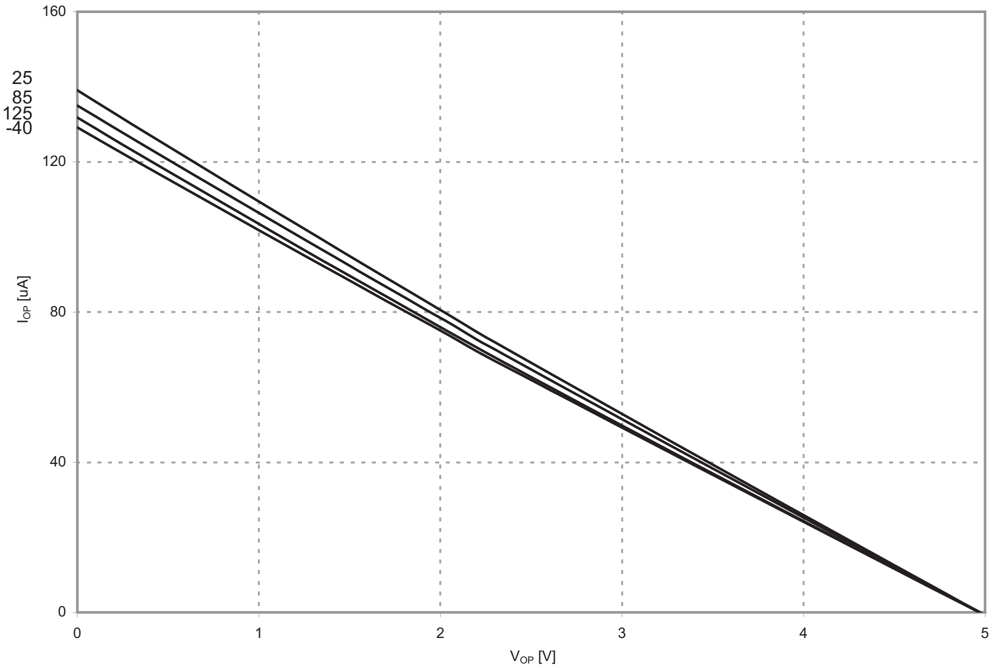


Figure 19. I/O pin Pull-up Resistor Current vs. Input Voltage (V_{CC} = 5V)



3.6.2 Reset Pin

Figure 20. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 1.8V)

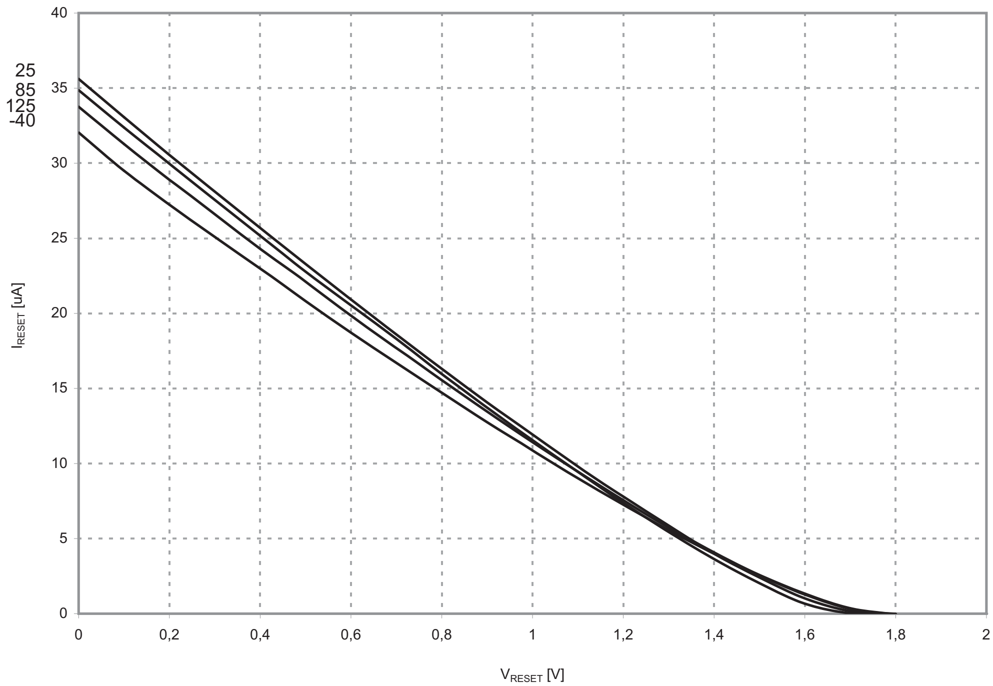


Figure 21. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 2.7V)

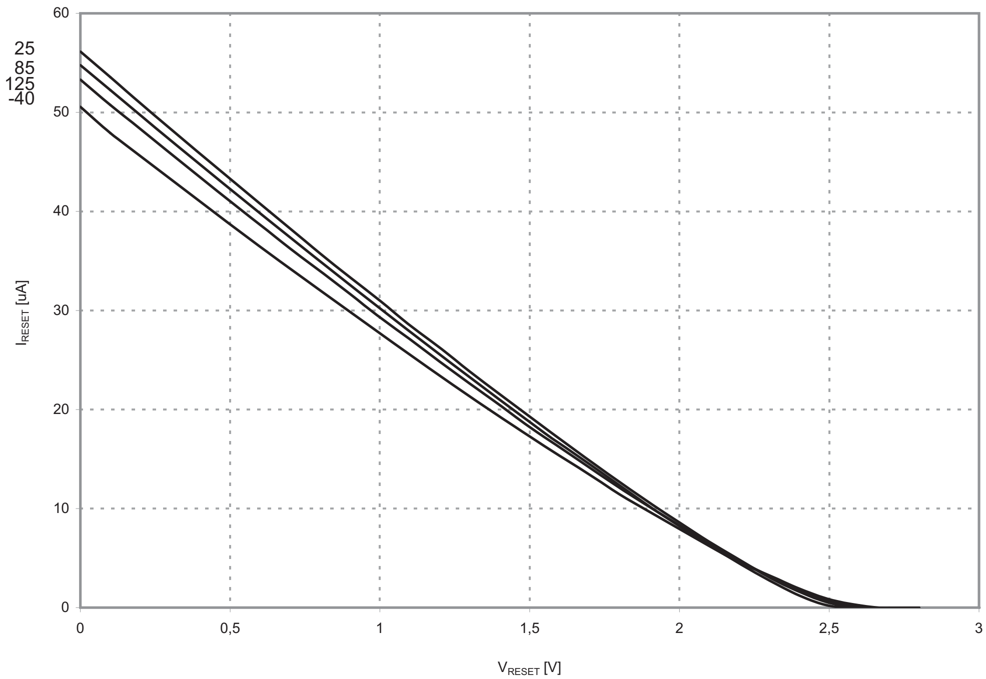
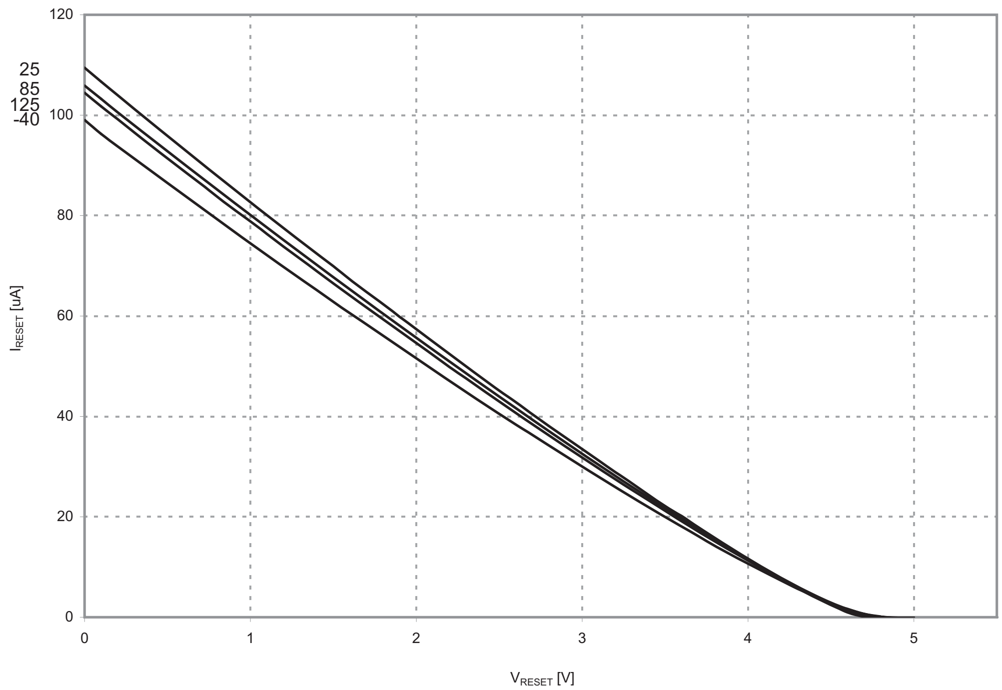


Figure 22. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 5V)



3.7 Input Thresholds

3.7.1 I/O Pins

Figure 23. V_{IH}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '1')

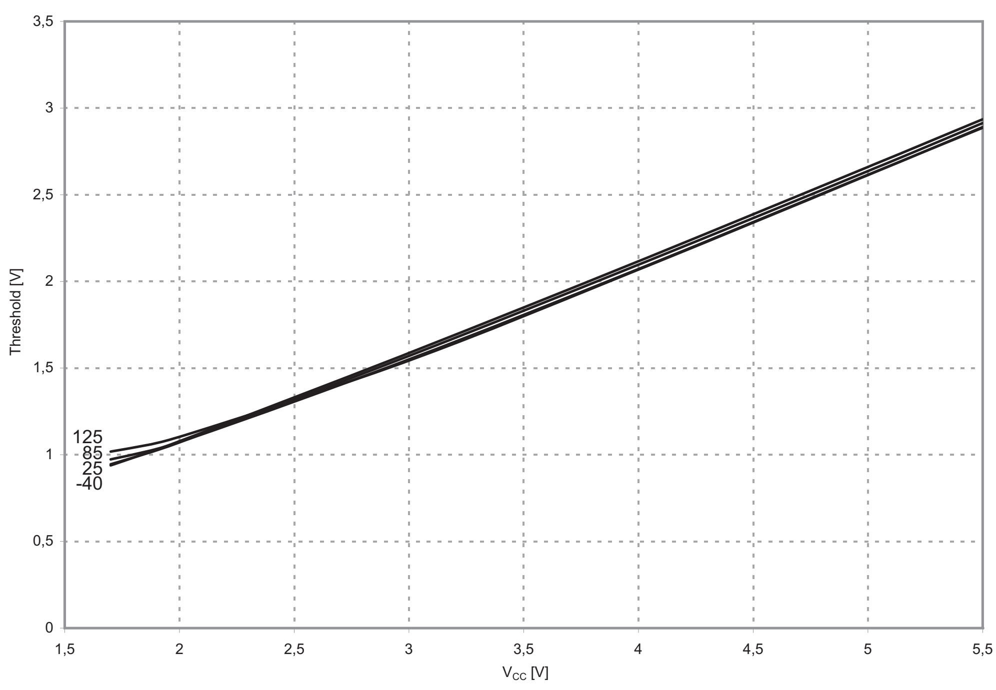


Figure 24. V_{IL}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '0')

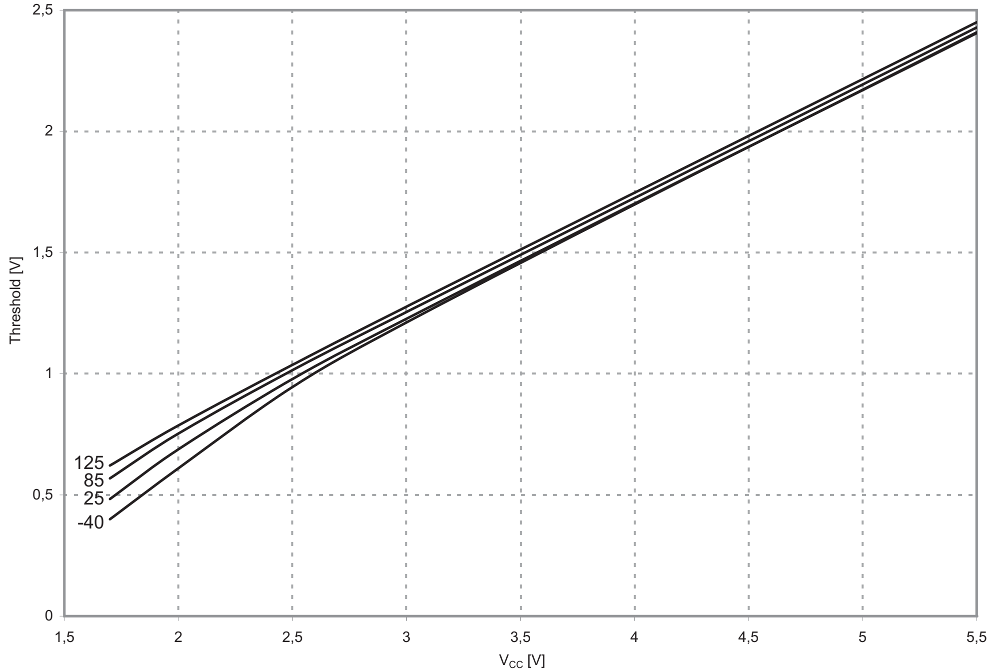
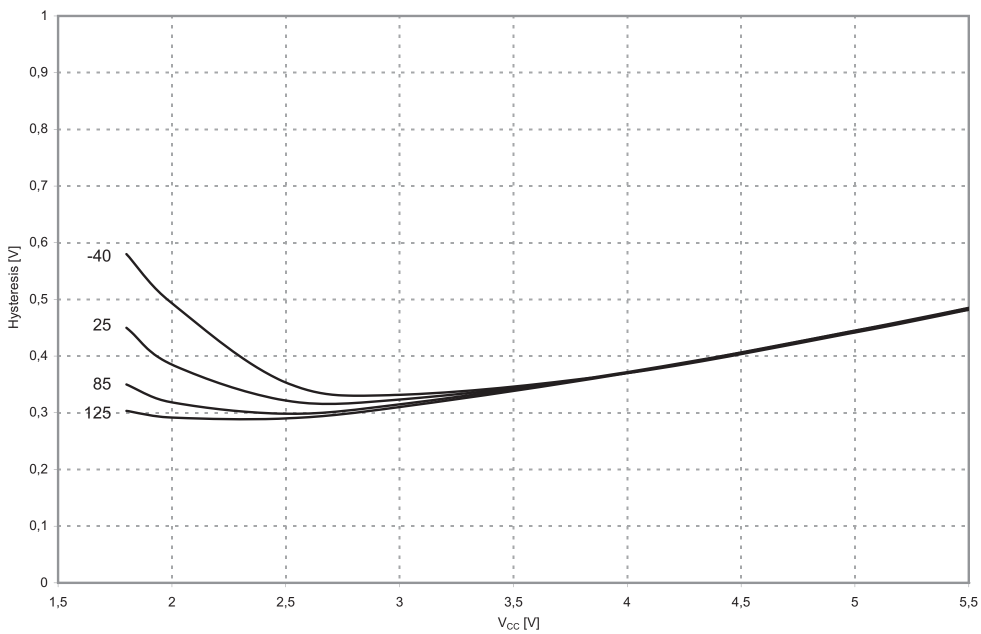


Figure 25. V_{IH}-V_{IL}: Input Hysteresis vs. V_{CC} (I/O Pin)



3.7.2 TWI Pins

Figure 26. V_{IH}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '1')

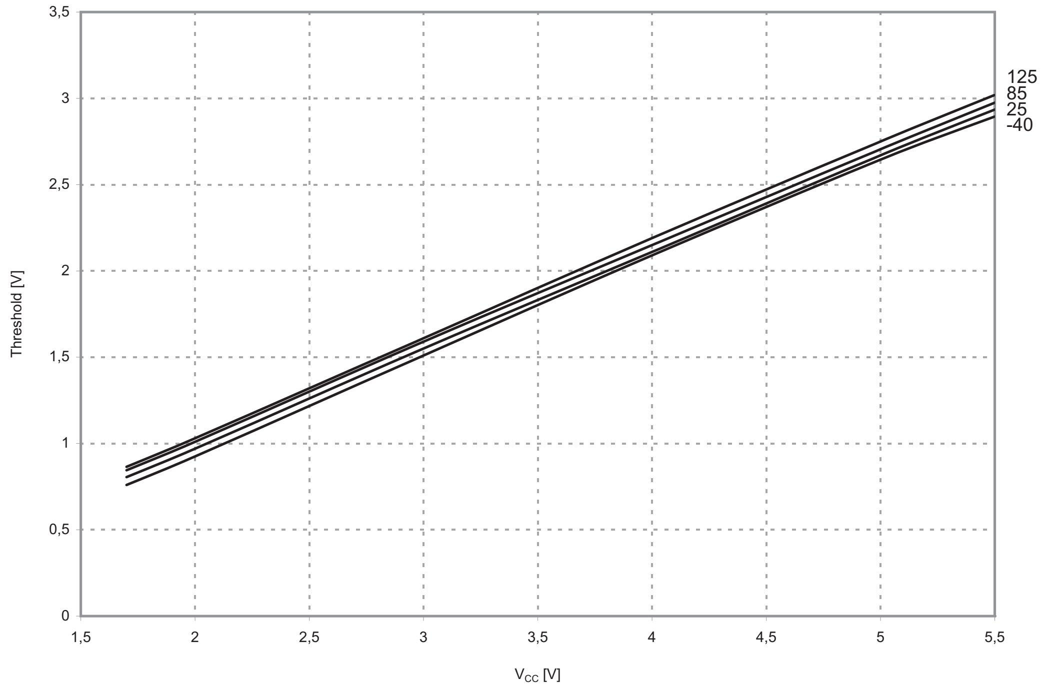


Figure 27. V_{IL}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '0')

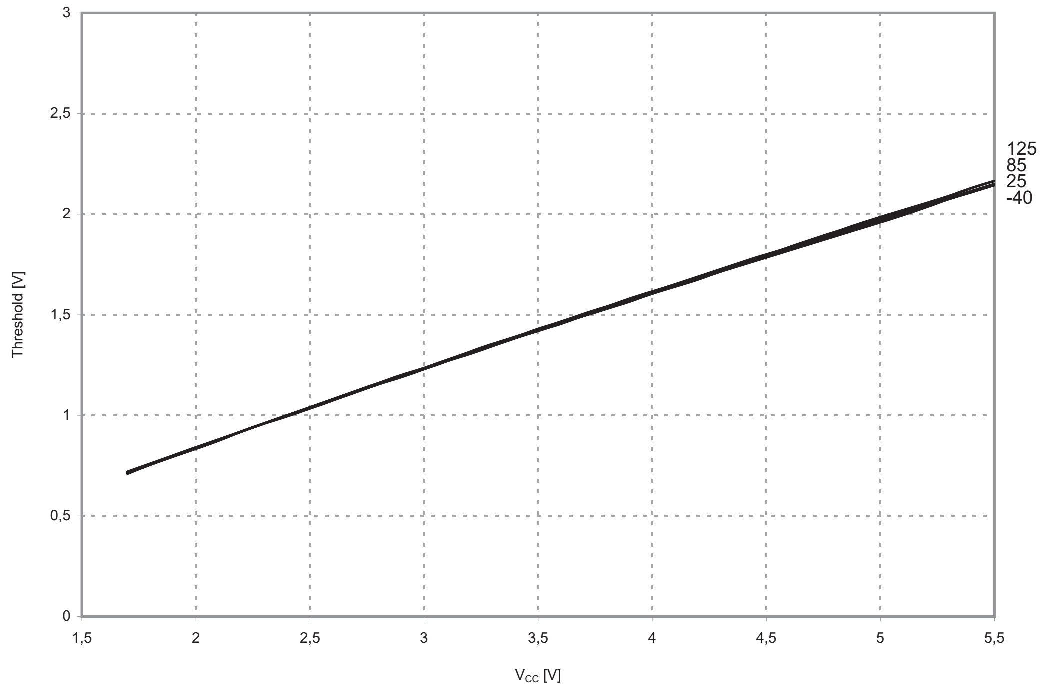
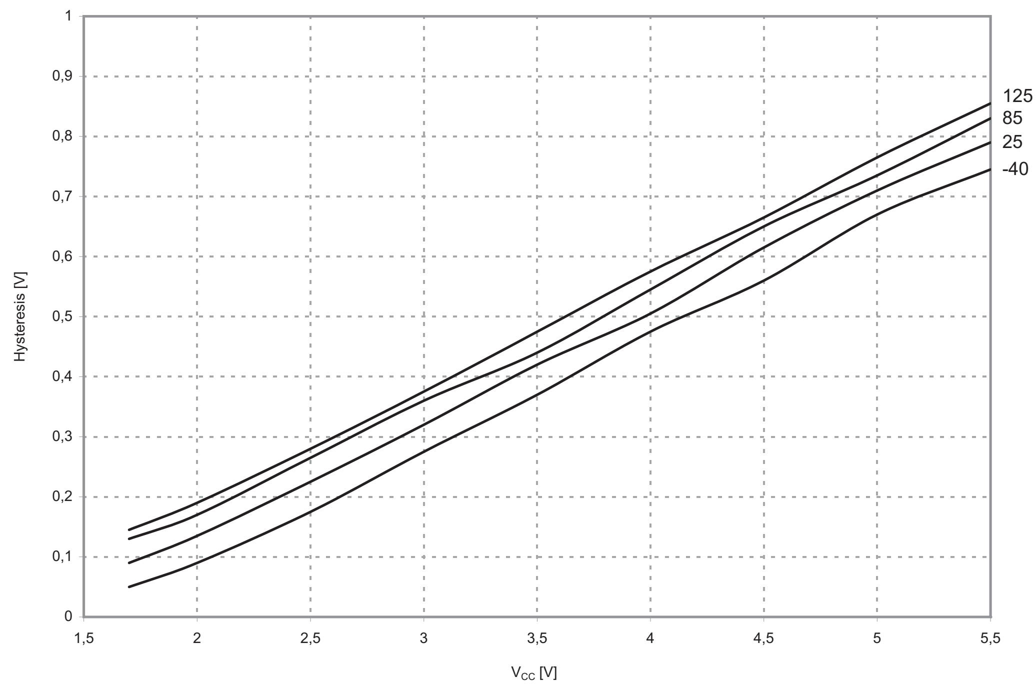


Figure 28. V_{IH}-V_{IL}: Input Hysteresis vs. V_{CC} (I/O Pin)



3.7.3 Reset Pin as I/O

Figure 29. V_{IH}: Input Threshold Voltage vs. V_{CC} (Reset Pin as I/O, Read as '1')

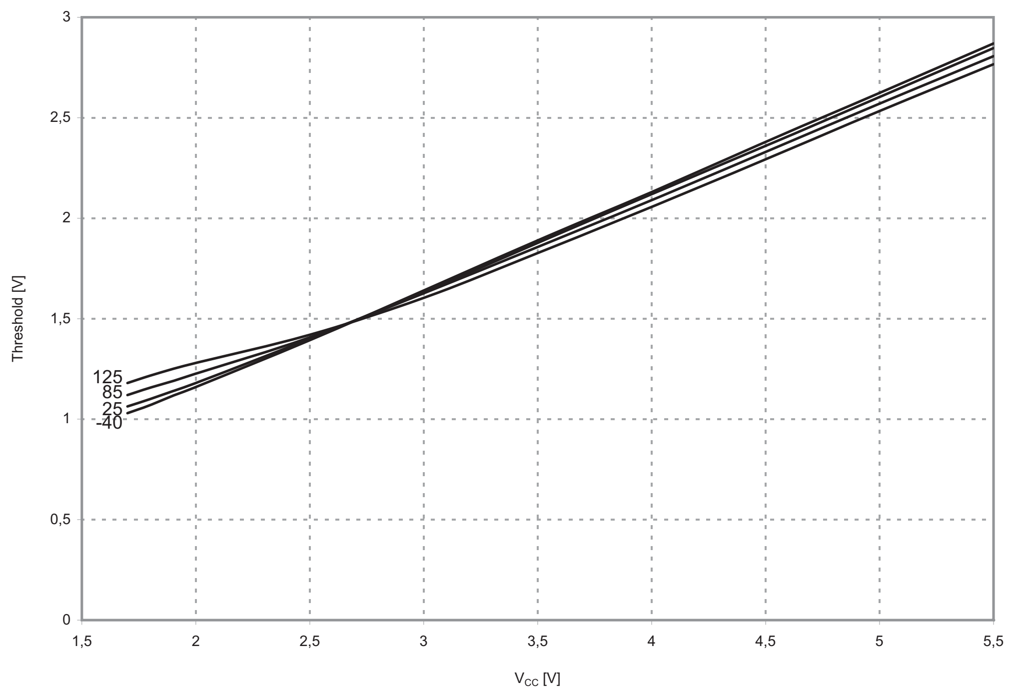


Figure 30. V_{IL}: Input Threshold Voltage vs. V_{CC} (Reset Pin as I/O, Read as ‘0’)

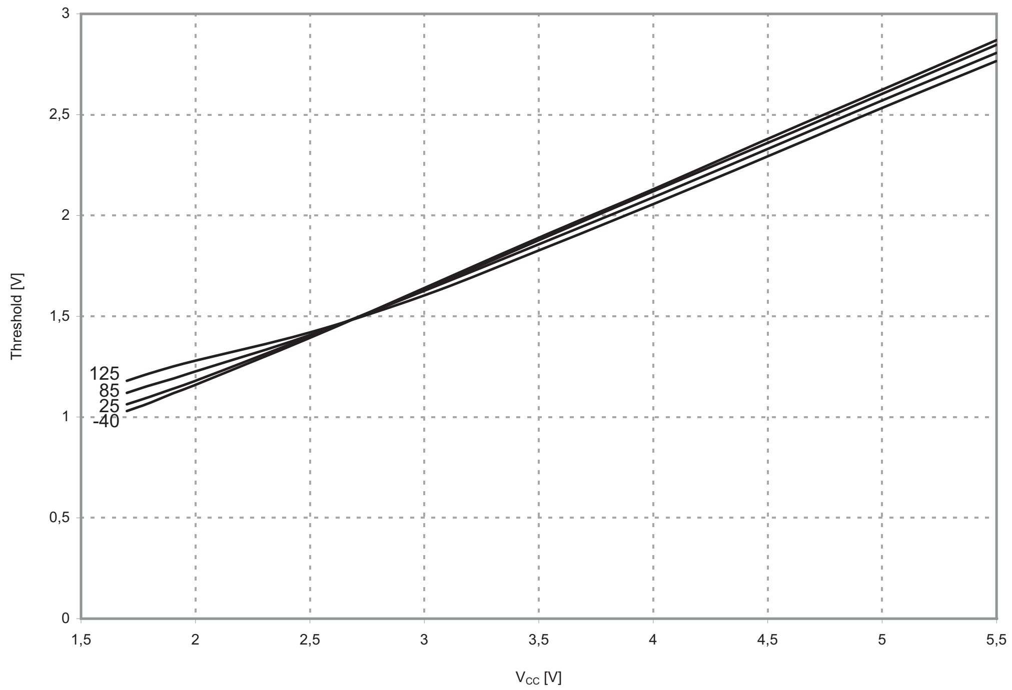
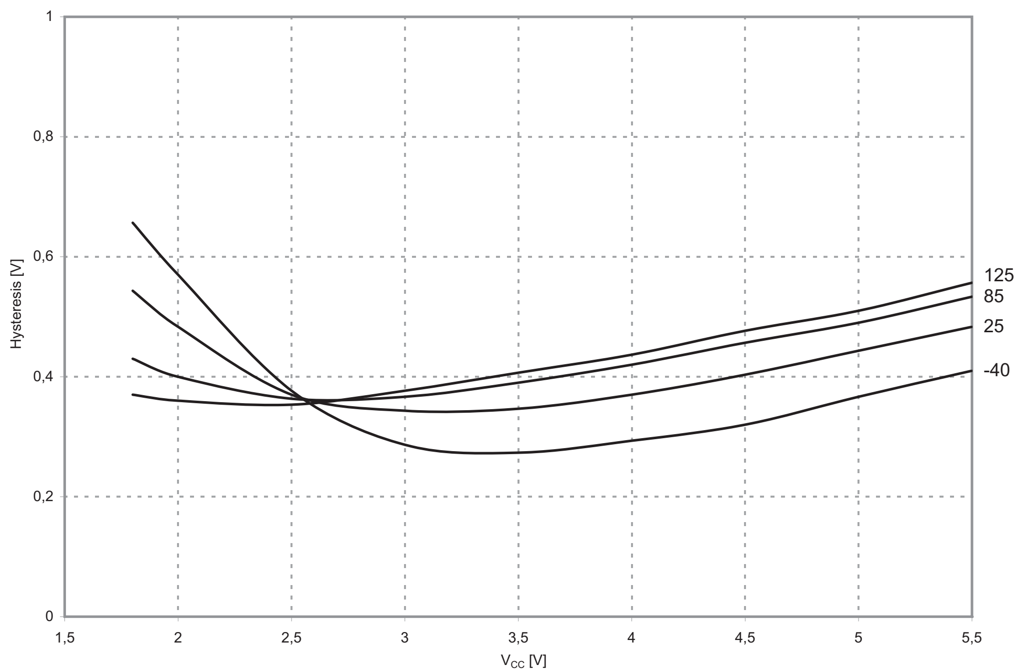


Figure 31. V_{IH}-V_{IL}: Input Hysteresis vs. V_{CC} (Reset Pin as I/O)



3.7.4 Reset Pin

Figure 32. V_{IH}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as '1')

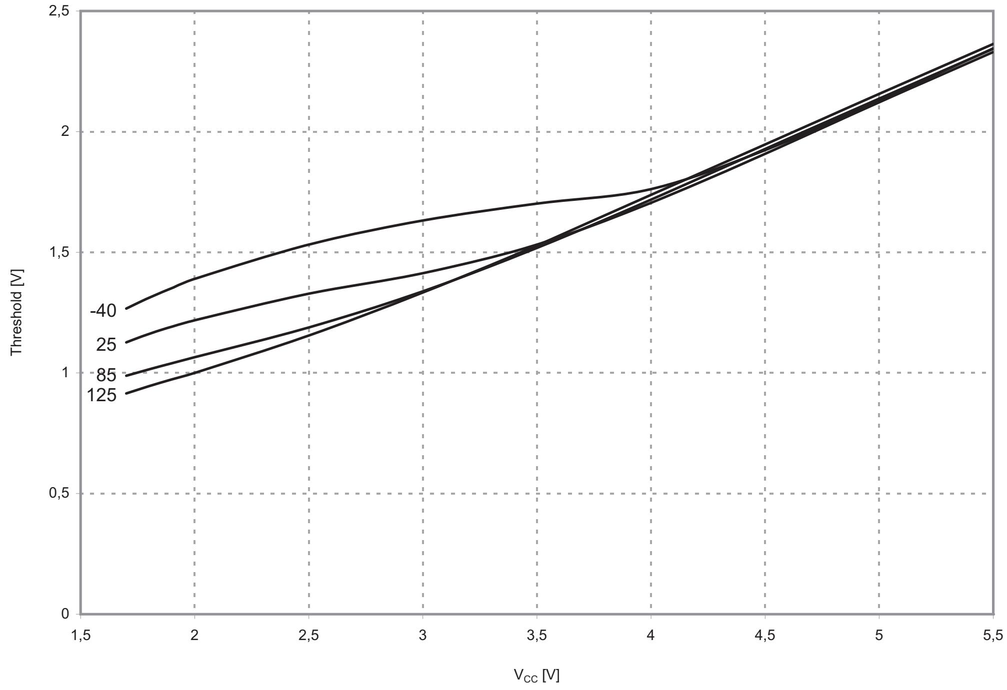


Figure 33. V_{IL}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as '0')

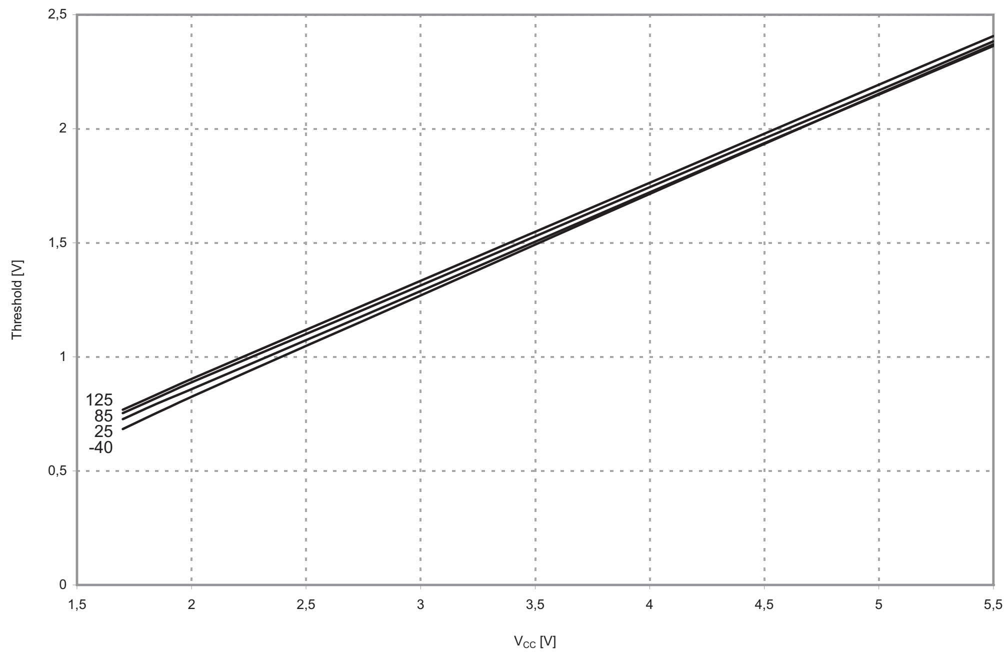
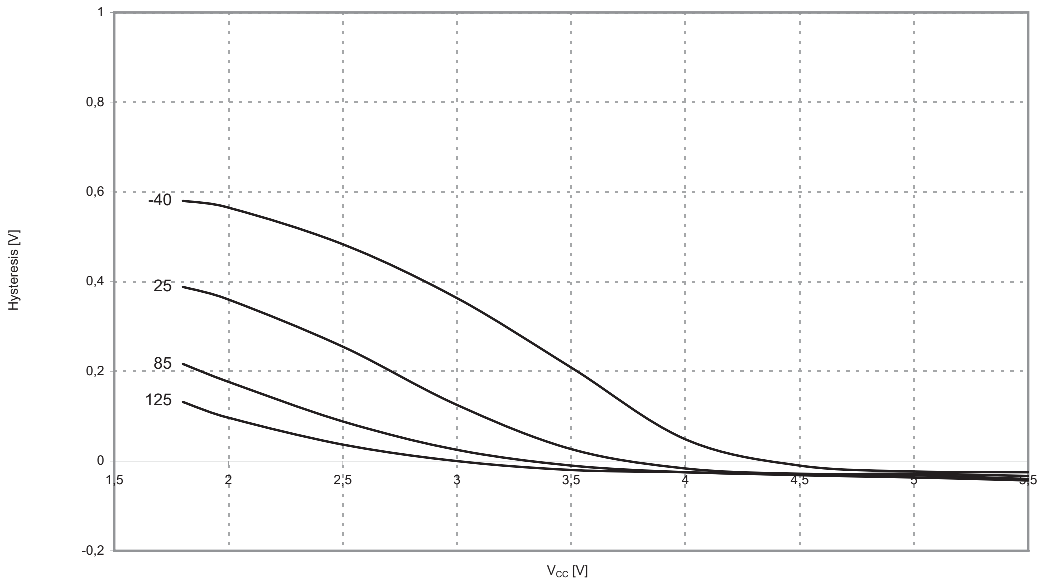


Figure 34. V_{IH}-V_{IL}: Input Hysteresis vs. V_{CC} (Reset Pin)



3.8 Current Source Strength

3.8.1 I/O Pins

Figure 35. V_{OH}: Output Voltage vs. Source Current (I/O Pin, V_{CC} = 1.8V)

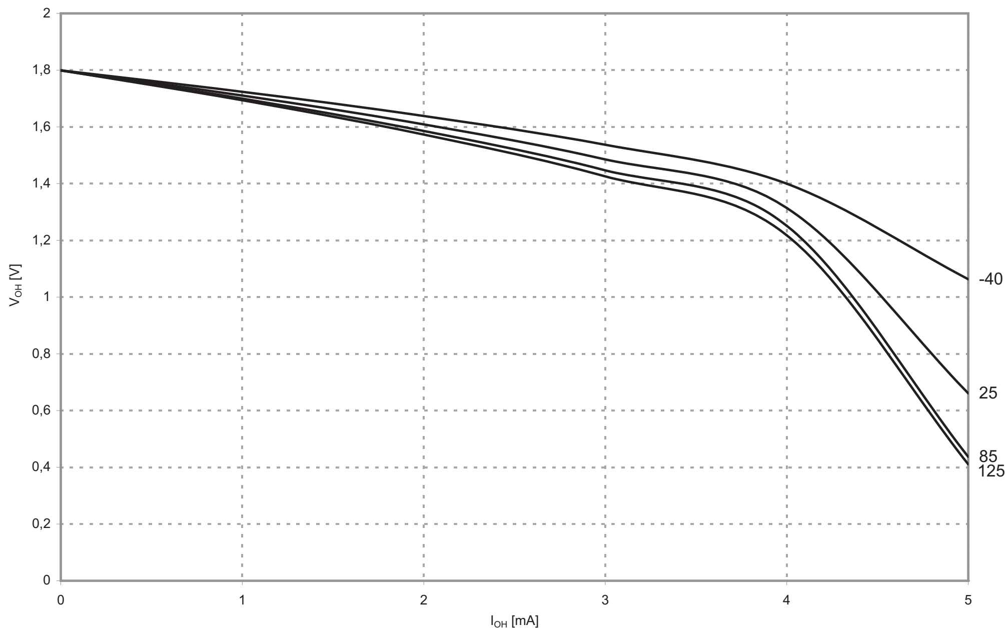


Figure 36. V_{OH}: Output Voltage vs. Source Current (I/O Pin, V_{CC} = 3V)

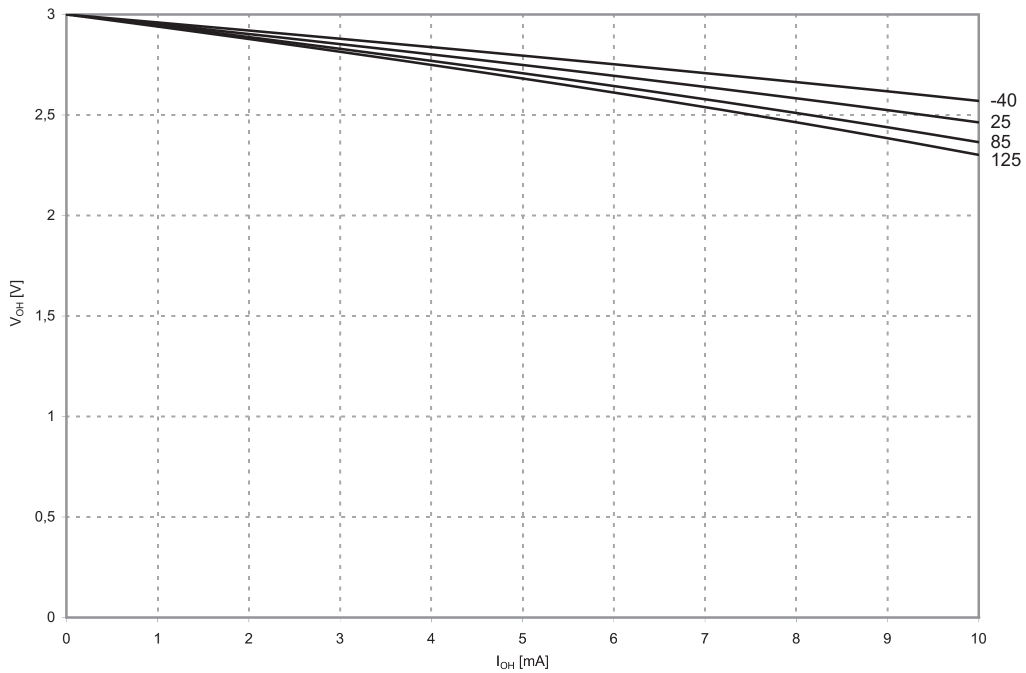
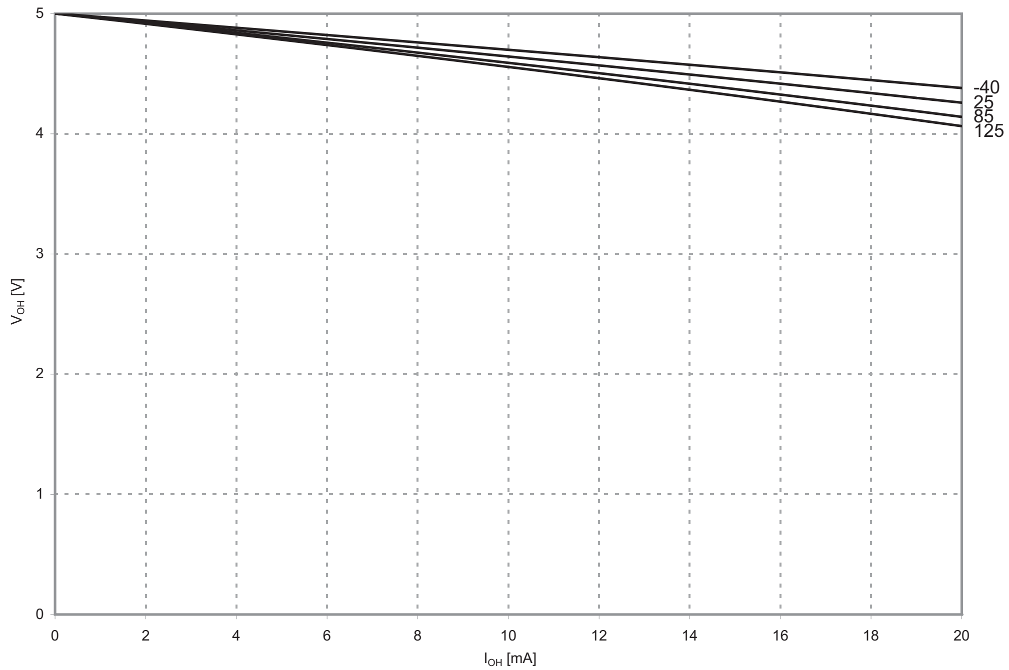


Figure 37. V_{OH}: Output Voltage vs. Source Current (I/O Pin, V_{CC} = 5V)



3.8.2 Reset Pin as I/O

Figure 38. V_{OH}: Output Voltage vs. Source Current (Reset Pin as I/O, V_{CC} = 1.8V

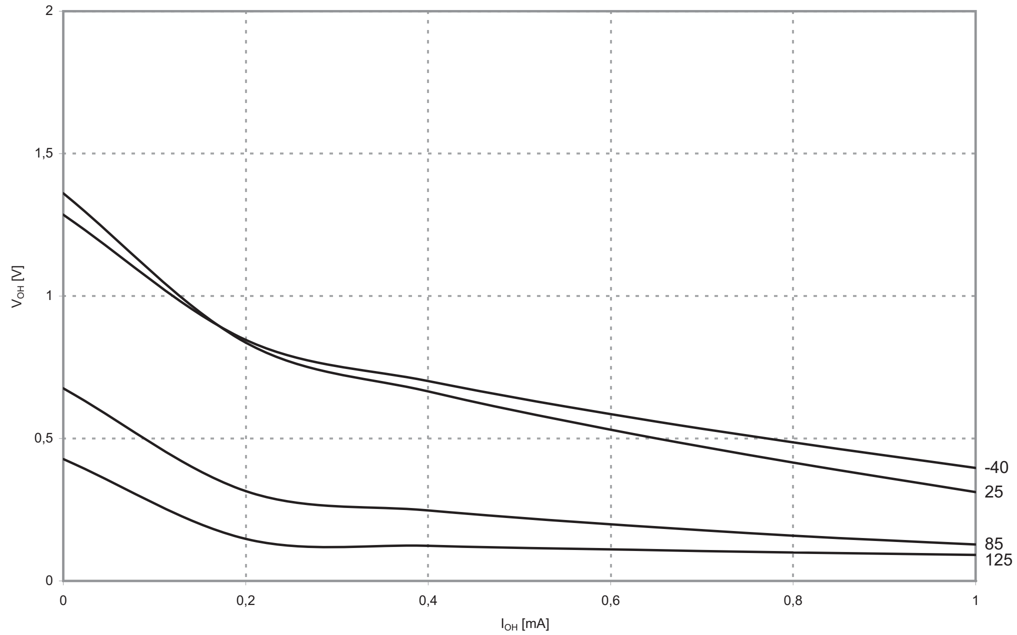


Figure 39. V_{OH}: Output Voltage vs. Source Current (Reset Pin as I/O, V_{CC} = 3V

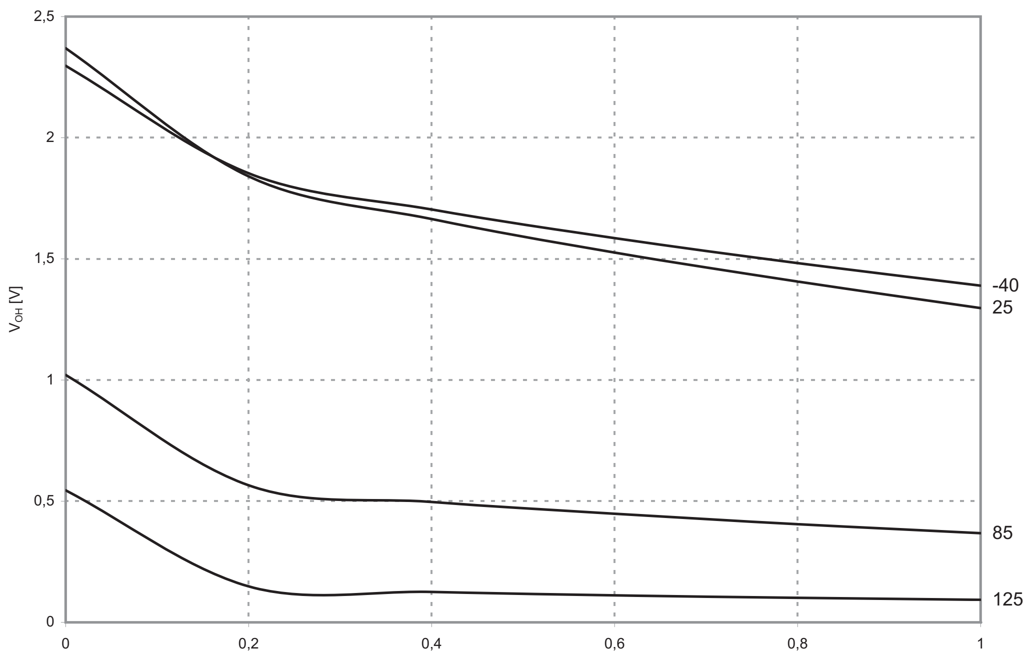
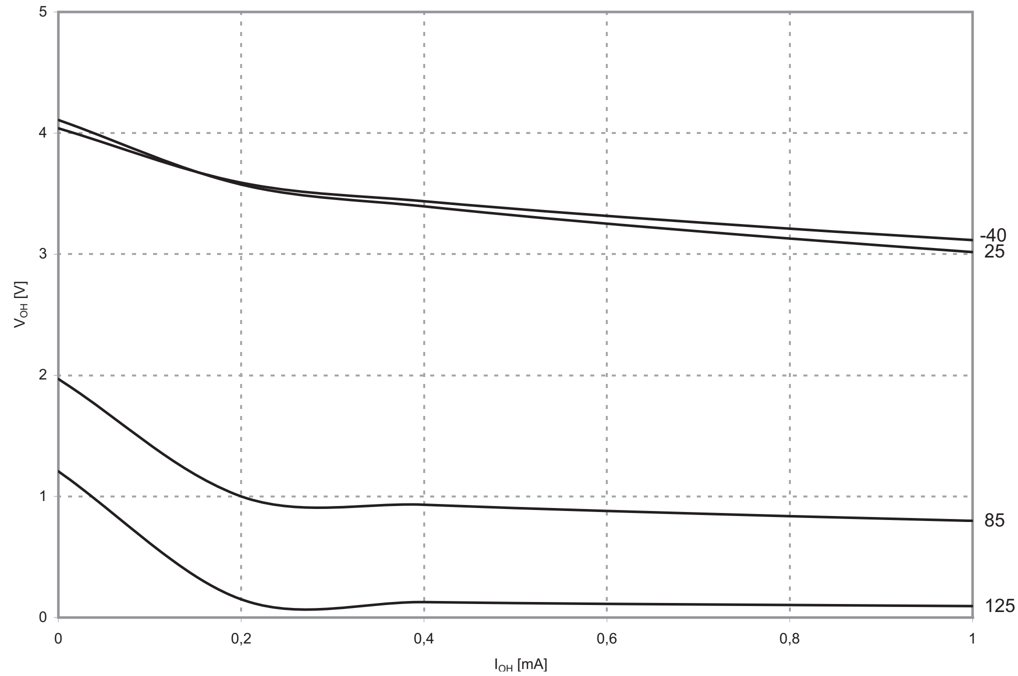


Figure 40. V_{OH}: Output Voltage vs. Source Current (Reset Pin as I/O, V_{CC} = 5V



3.9 Current Sink Capability

3.9.1 I/O Pins with Standard Sink Capability

Figure 41. V_{OL}: Output Voltage vs. Sink Current (Standard I/O Pin, V_{CC} = 1.8V)

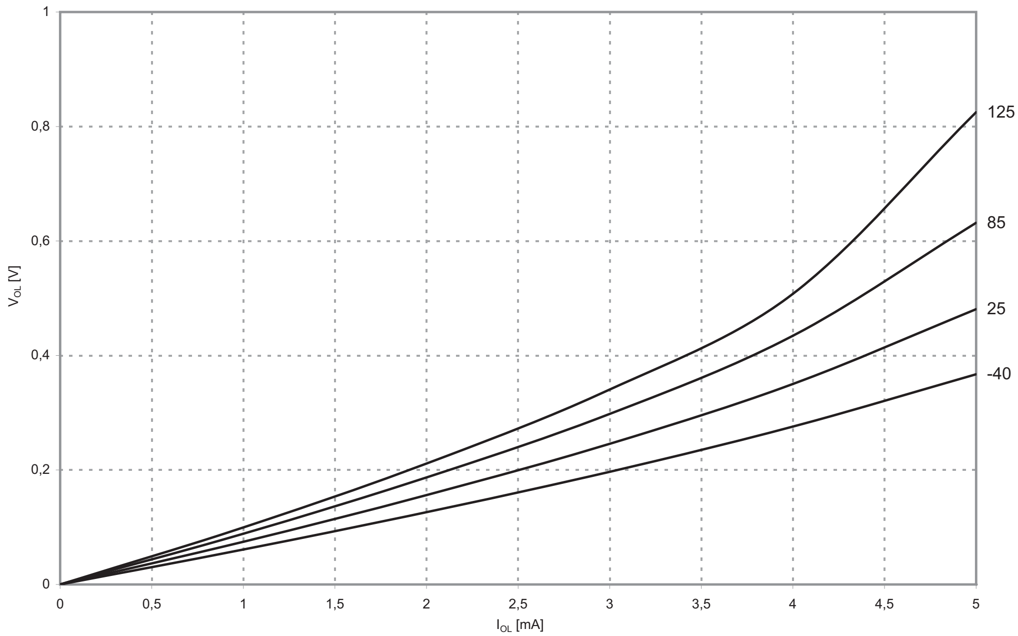


Figure 42. V_{OL}: Output Voltage vs. Sink Current (Standard I/O Pin, V_{CC} = 3V)

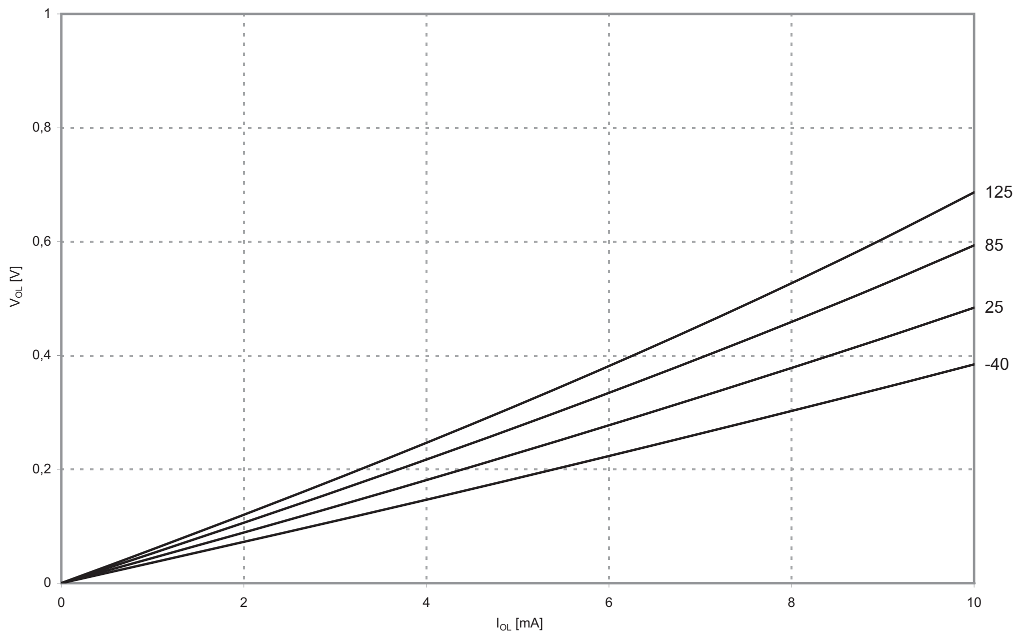
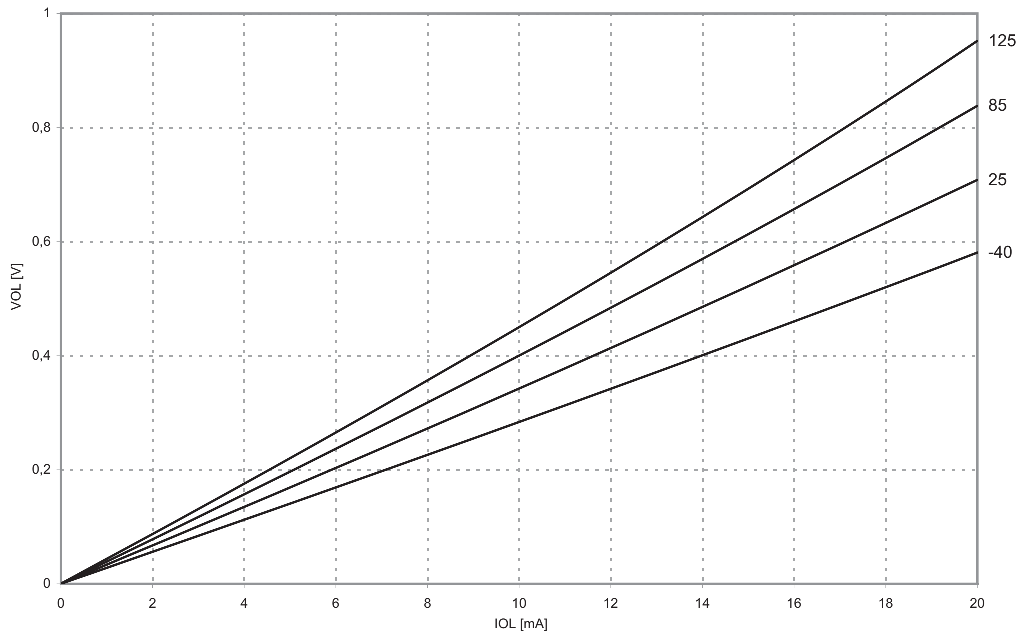


Figure 43. V_{OL}: Output Voltage vs. Sink Current (Standard I/O Pin, V_{CC} = 5V)



3.9.2 I/O Pins with High Sink Capability

Figure 44. V_{OL}: Output Voltage vs. Sink Current (High Sink I/O Pin, V_{CC} = 1.8V)

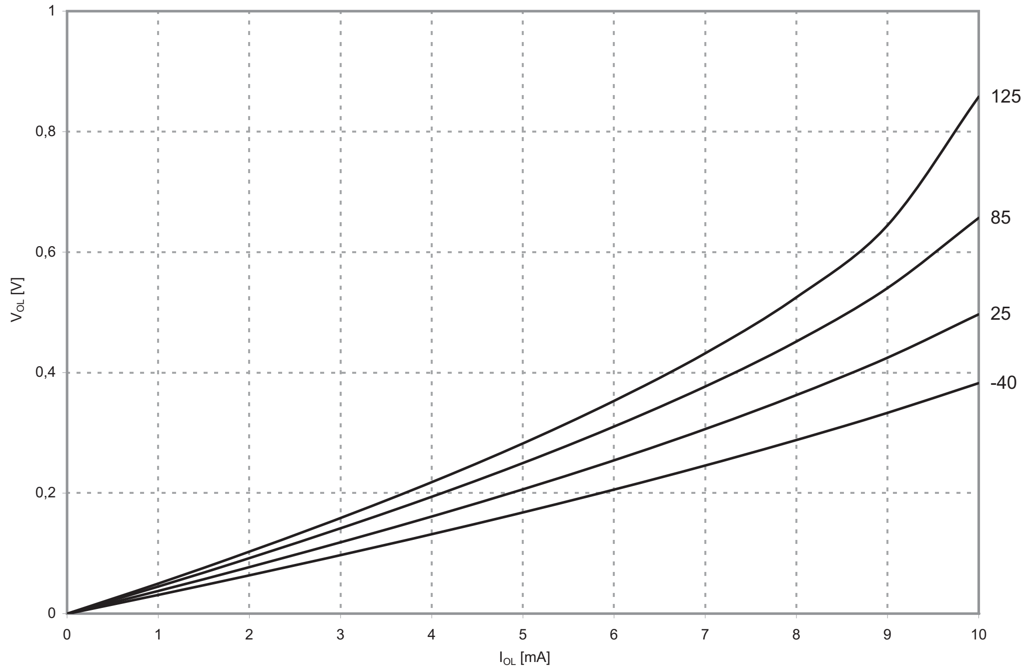


Figure 45. V_{OL}: Output Voltage vs. Sink Current (High Sink I/O Pin, V_{CC} = 3V)

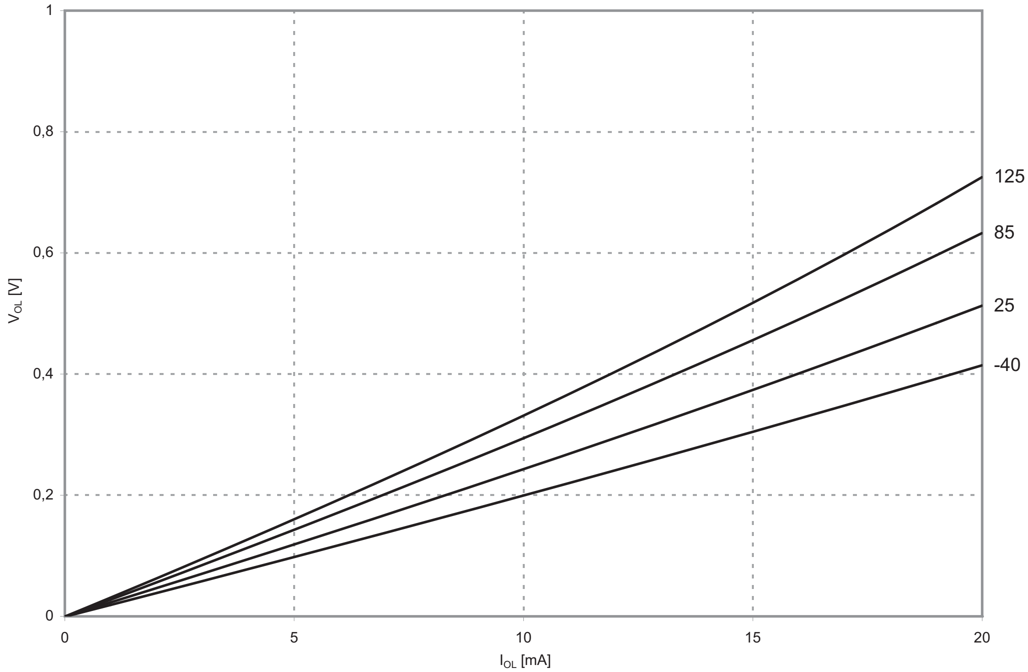
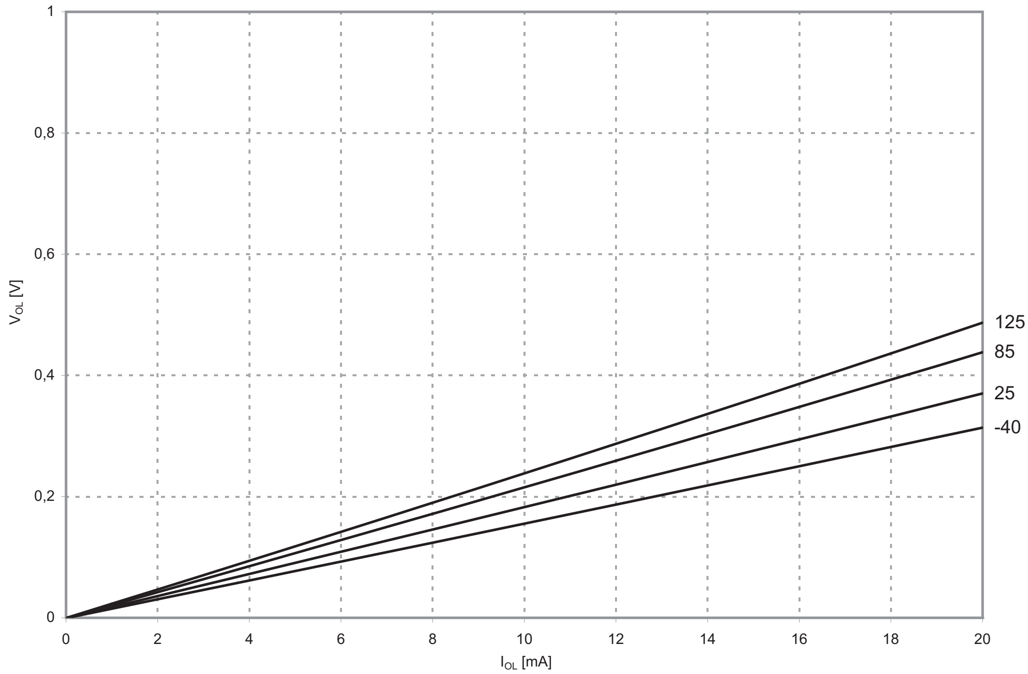


Figure 46. V_{OL}: Output Voltage vs. Sink Current (High Sink I/O Pin, V_{CC} = 5V)



3.9.3 I/O Pins with Extra High Sink Capability

Figure 47. V_{OL}: Output Voltage vs. Sink Current (Extra High Sink I/O Pin, V_{CC} = 1.8V)

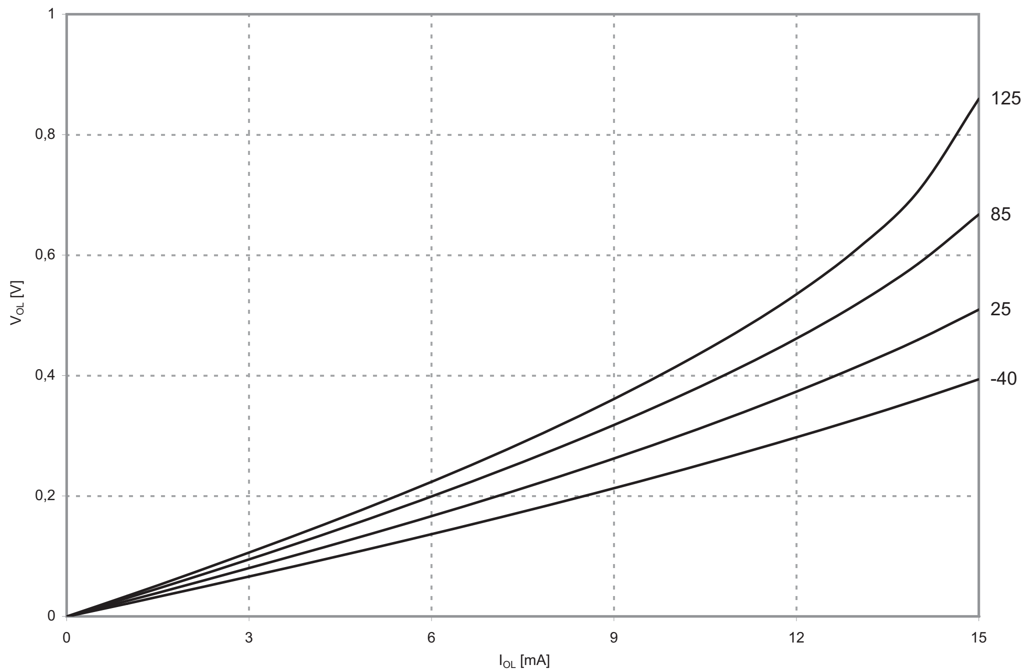


Figure 48. V_{OL}: Output Voltage vs. Sink Current (Extra High Sink I/O Pin, V_{CC} = 3V)

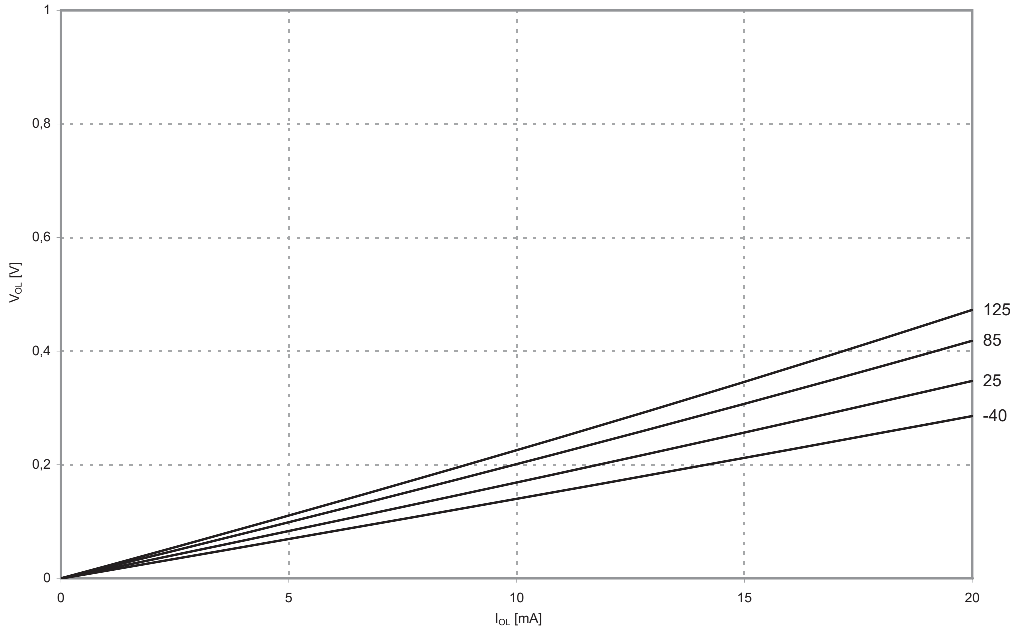
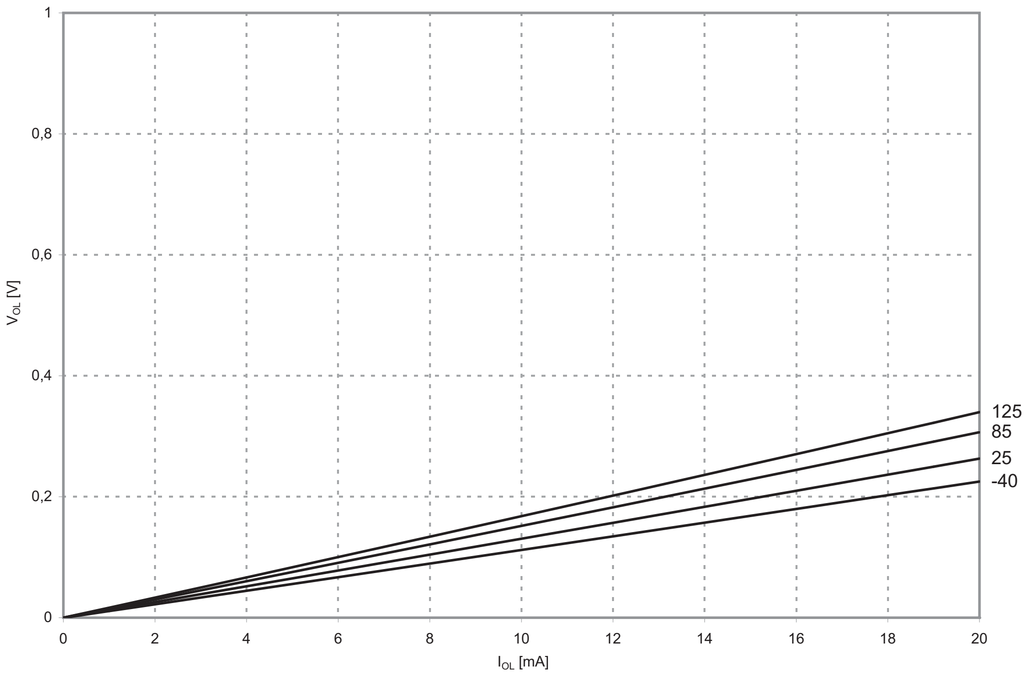


Figure 49. V_{OL}: Output Voltage vs. Sink Current (Extra High Sink I/O Pin, V_{CC} = 5V)



3.9.4 Reset Pin as I/O

Figure 50. V_{OL}: Output Voltage vs. Sink Current (Reset Pin as I/O, V_{CC} = 1.8V)

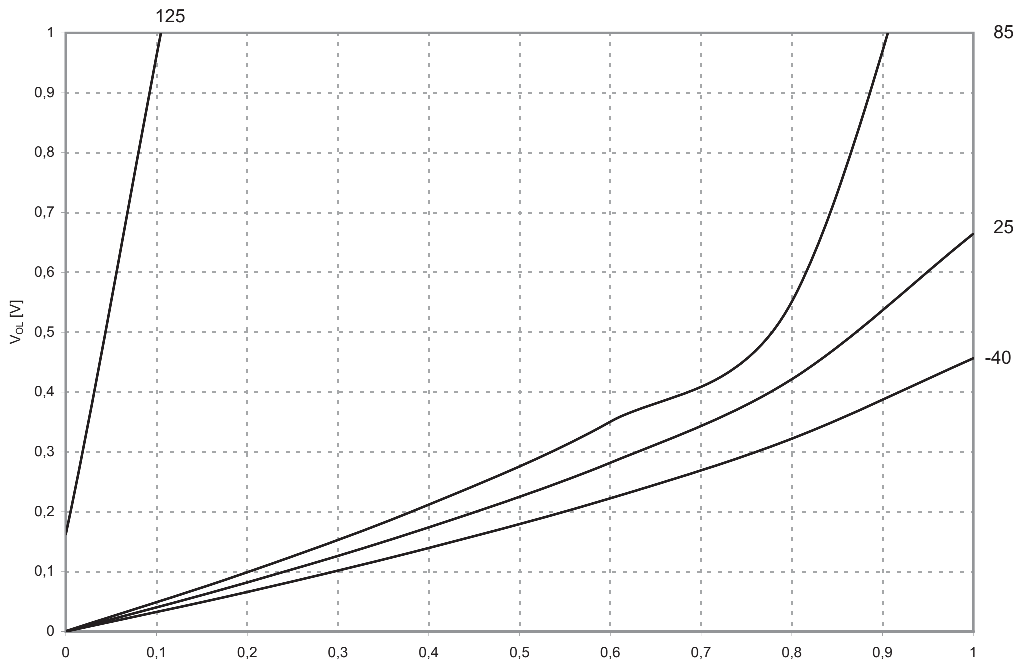


Figure 51. V_{OL}: Output Voltage vs. Sink Current (Reset Pin as I/O, V_{CC} = 3V)

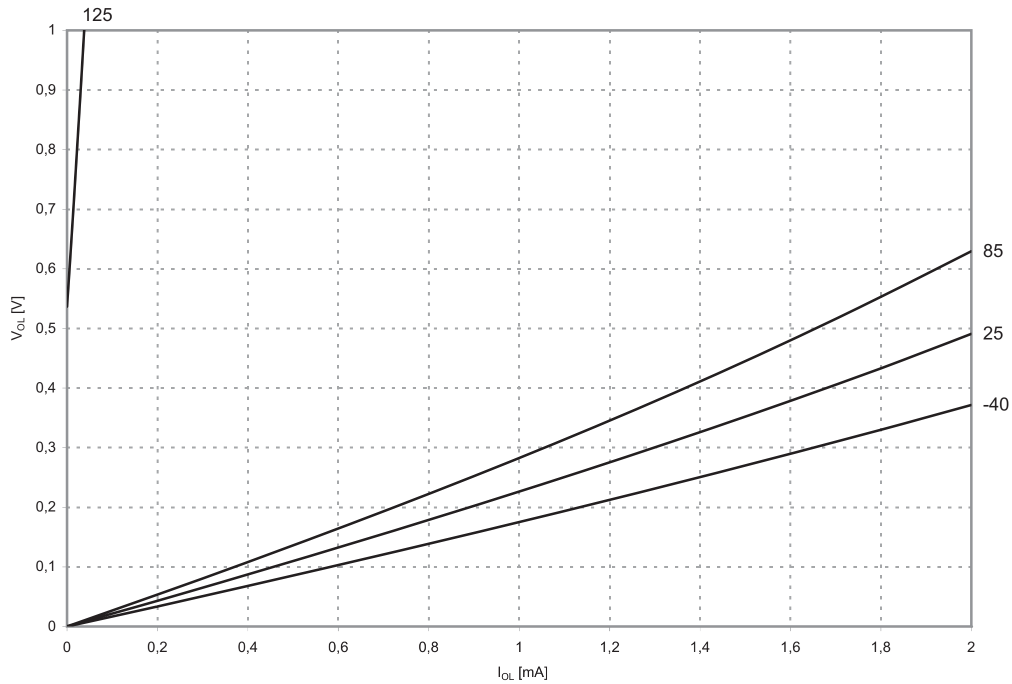
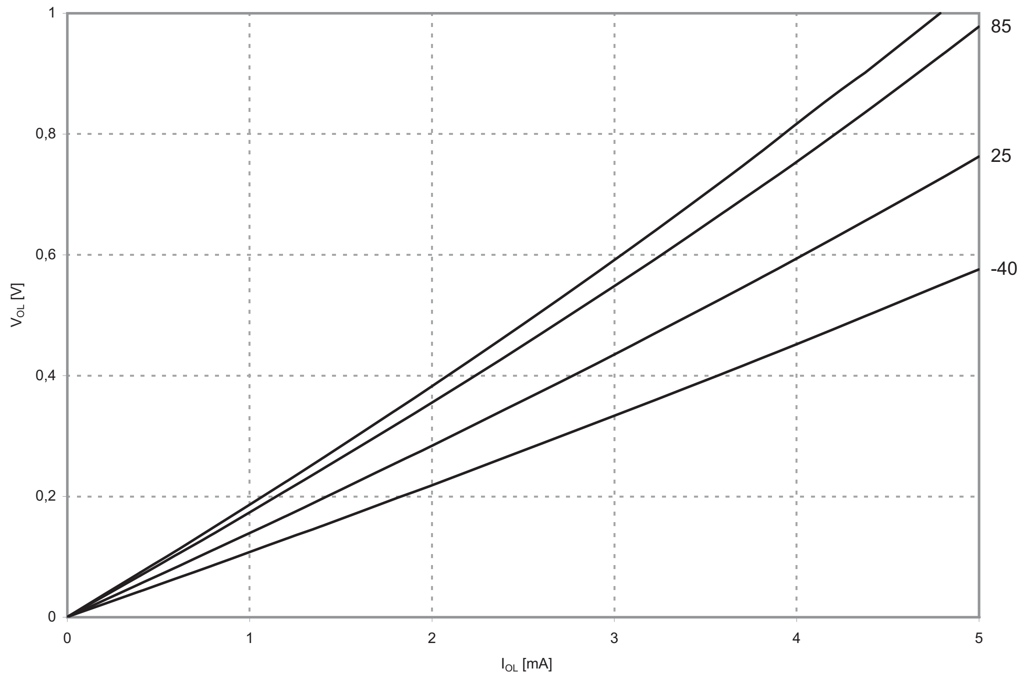


Figure 52. V_{OL}: Output Voltage vs. Sink Current (Reset Pin as I/O, V_{CC} = 5V)



3.10 BOD

Figure 53. BOD Threshold vs Temperature (BODLEVEL = 4.3V)

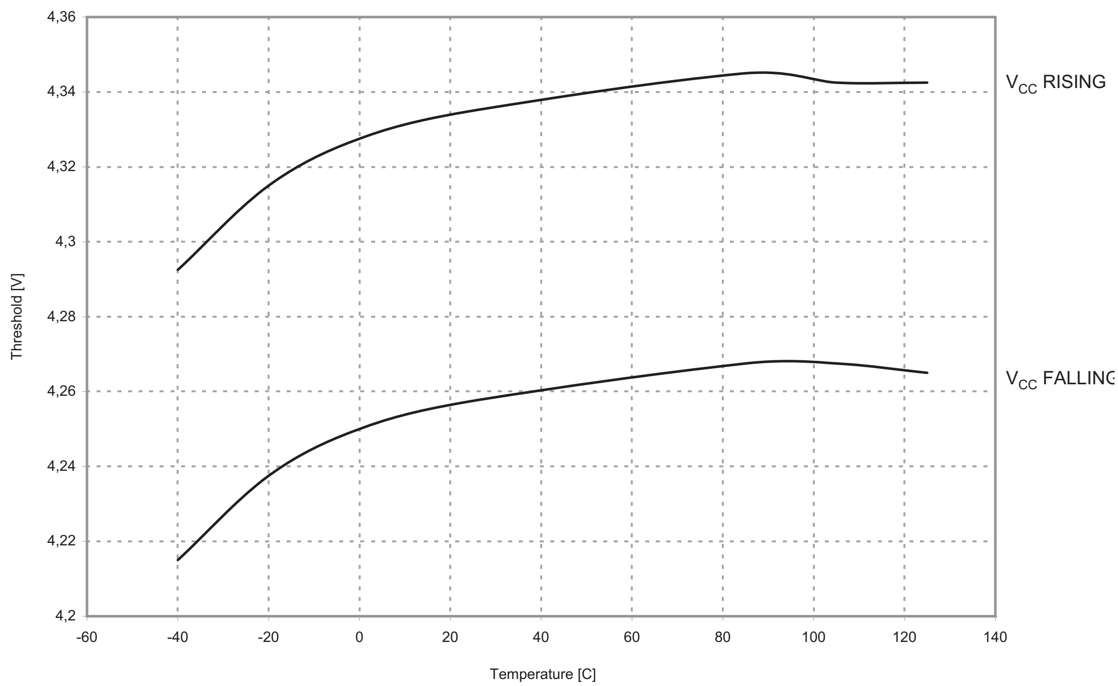


Figure 54. BOD Threshold vs Temperature (BODLEVEL = 2.7V)

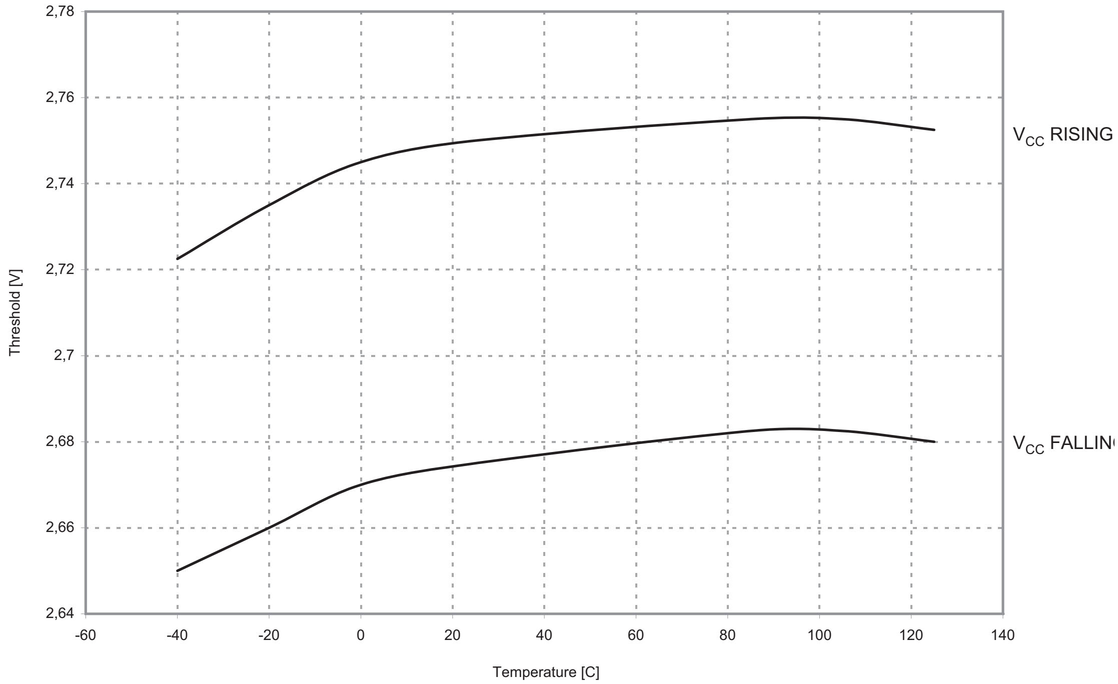


Figure 55. BOD Threshold vs Temperature (BODLEVEL = 1.8V)

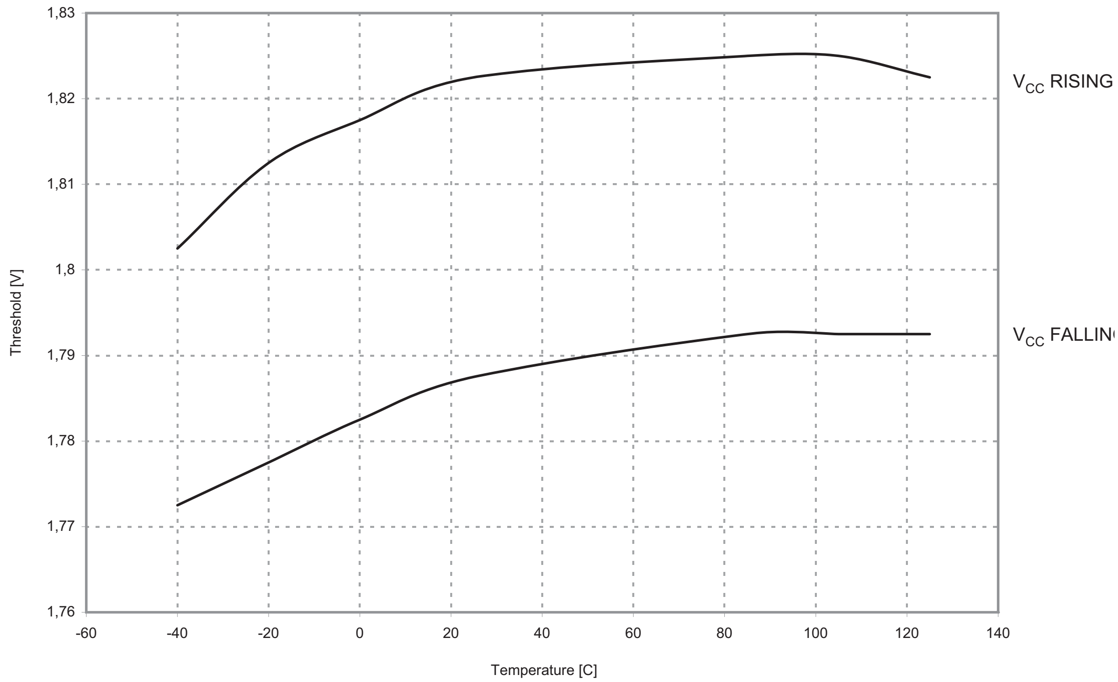


Figure 56. Sampled BOD Threshold vs Temperature (BODLEVEL = 4.3V)

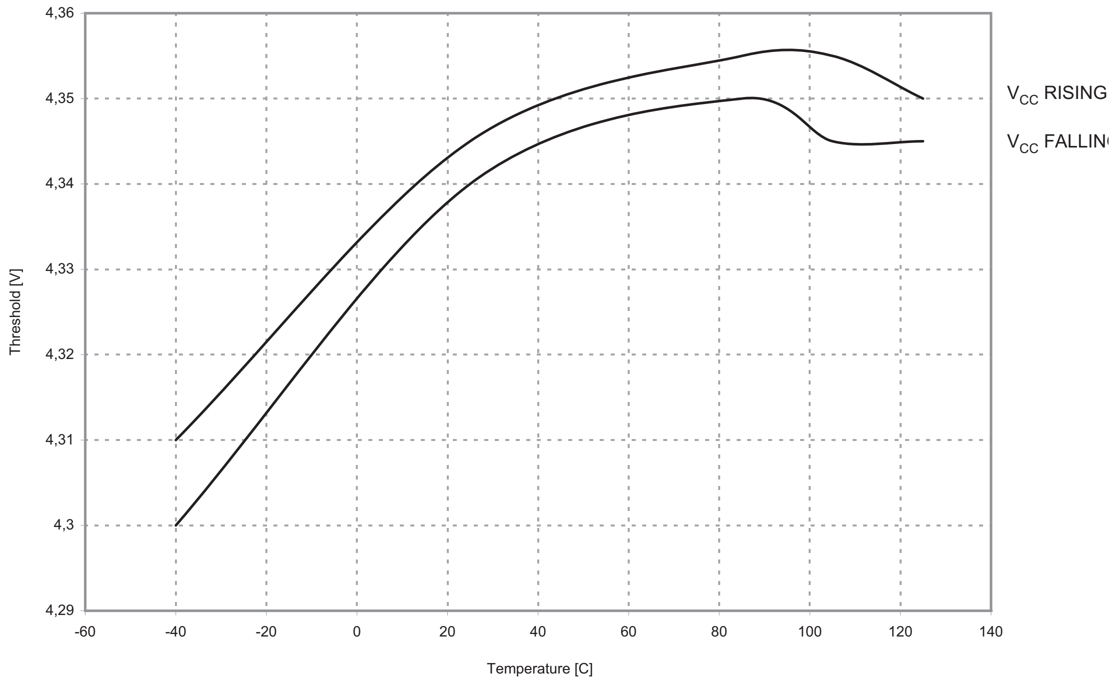


Figure 57. Sampled BOD Threshold vs Temperature (BODLEVEL = 2.7V)

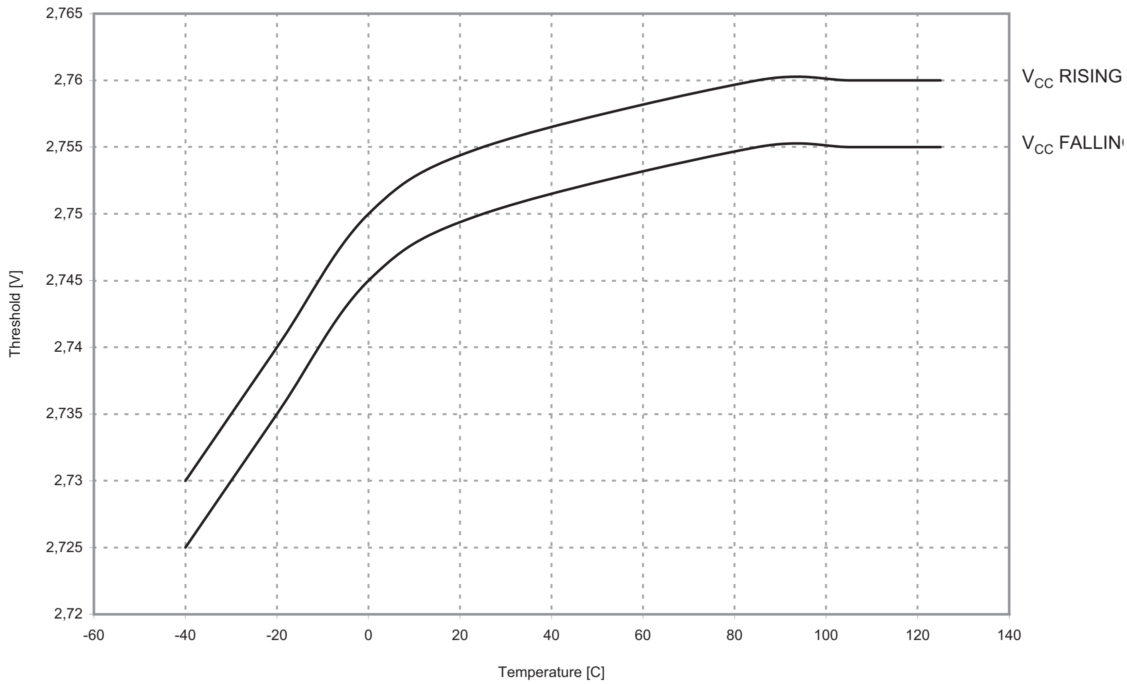
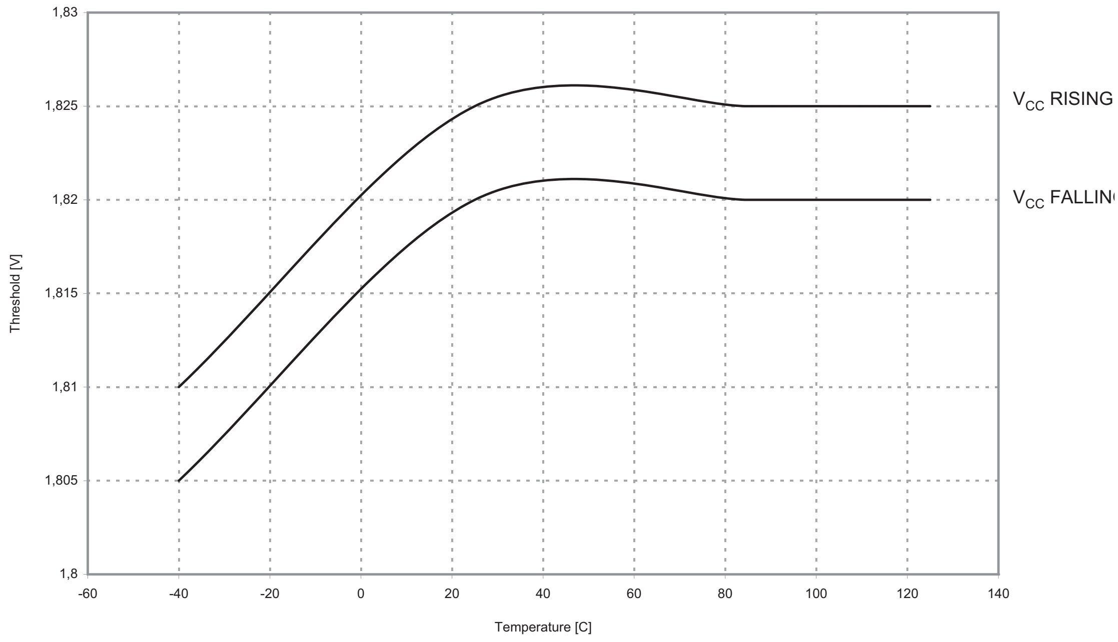


Figure 58. Sampled BOD Threshold vs Temperature (BODLEVEL = 1.8V)



3.11 Bandgap Voltage

Figure 59. Bandgap Voltage vs. Supply Voltage

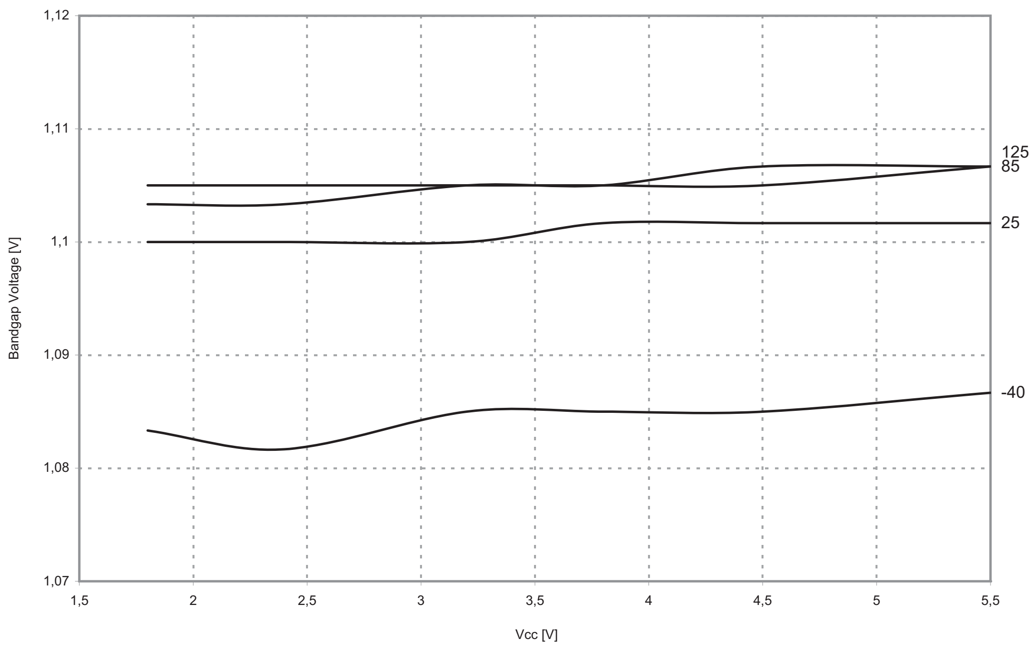
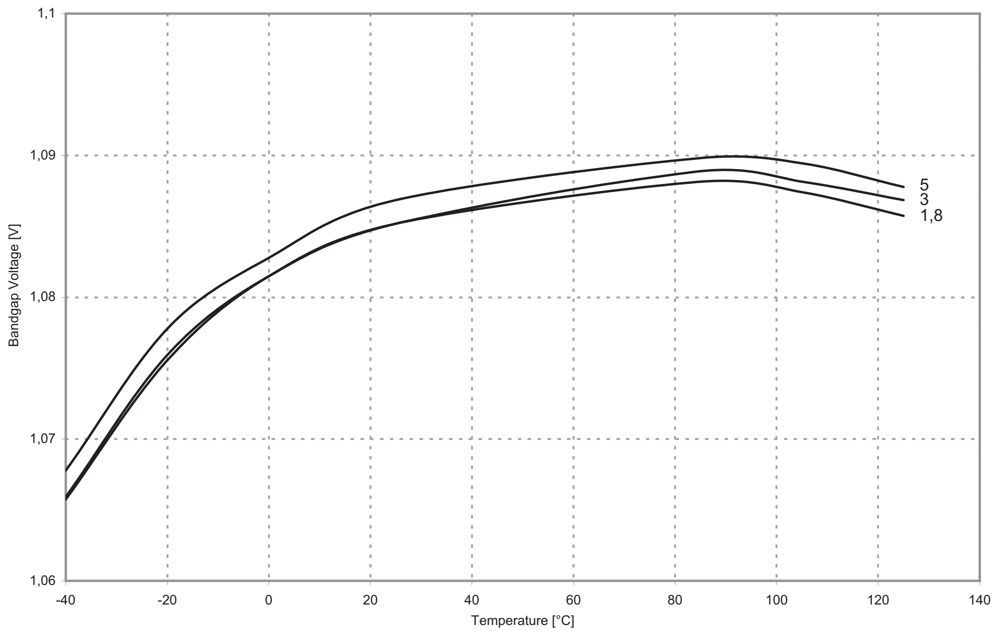


Figure 60. Bandgap Voltage vs. Temperature (V_{CC} = 1.8 / 3 / 5V)



3.12 Reset

Figure 61. POR Trigger Levels

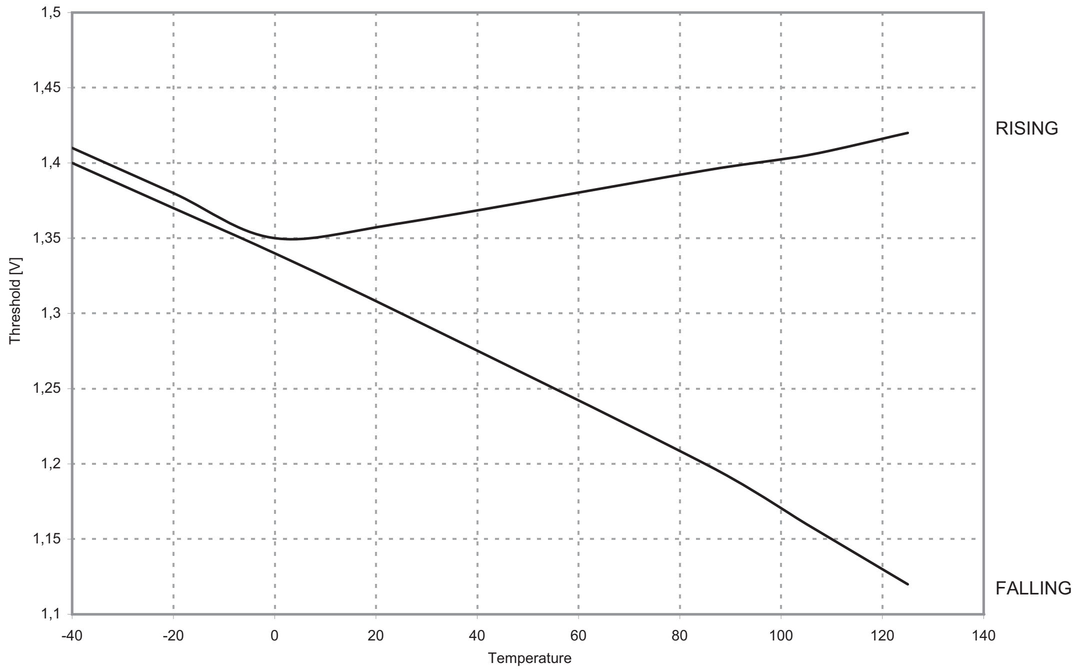
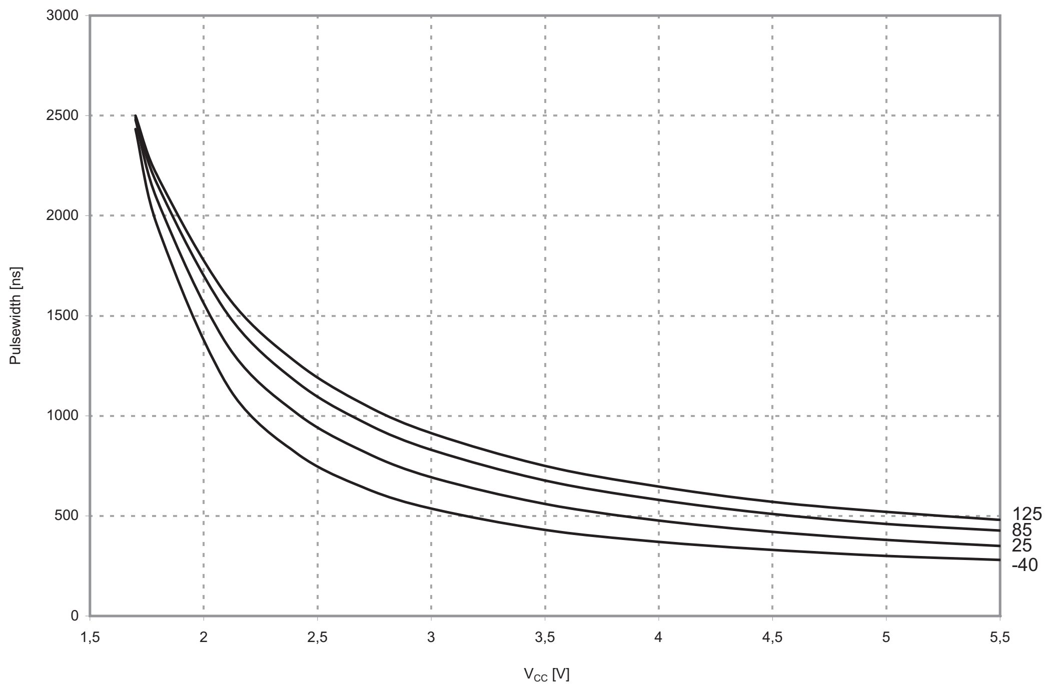


Figure 62. Minimum Reset Pulse Width vs. V_{CC}



3.13 Analog Comparator Offset

Figure 63. Analog Comparator Offset vs. V_{IN} (V_{CC} = 5V)

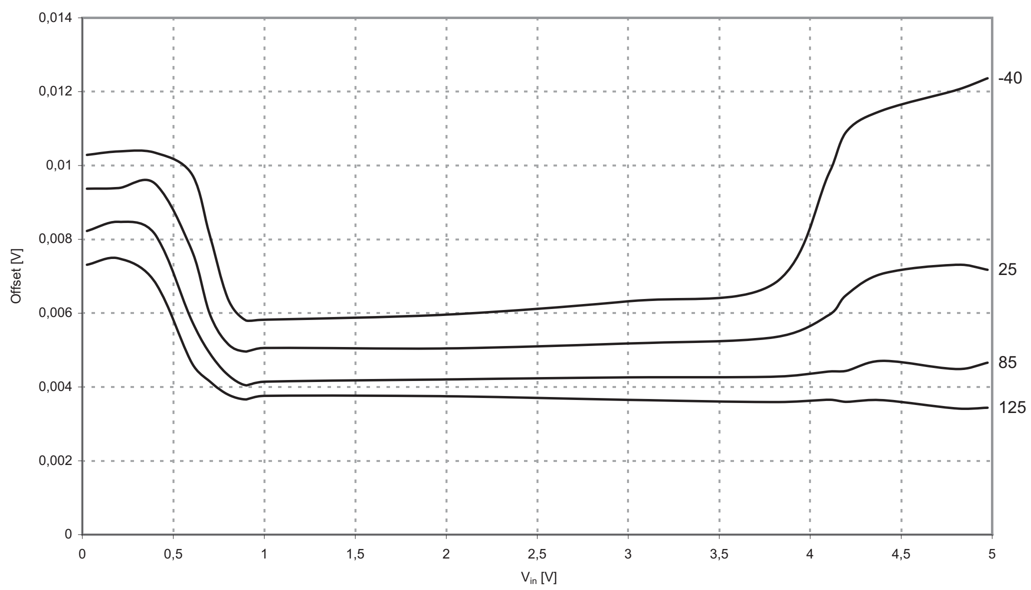


Figure 64. Analog Comparator Offset vs. V_{CC} (V_{IN} = 1.1V)

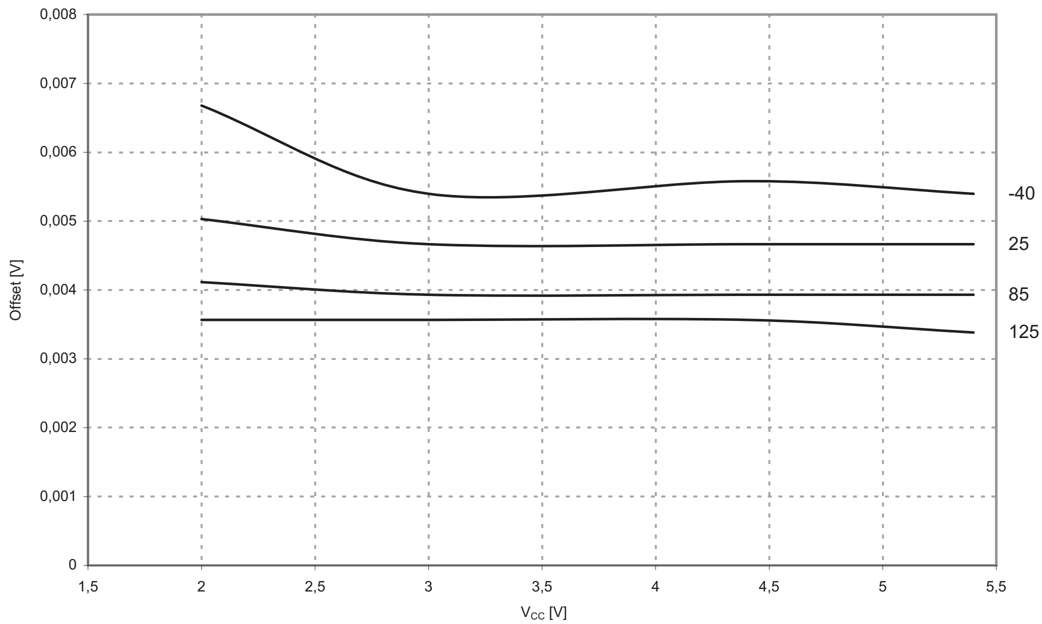
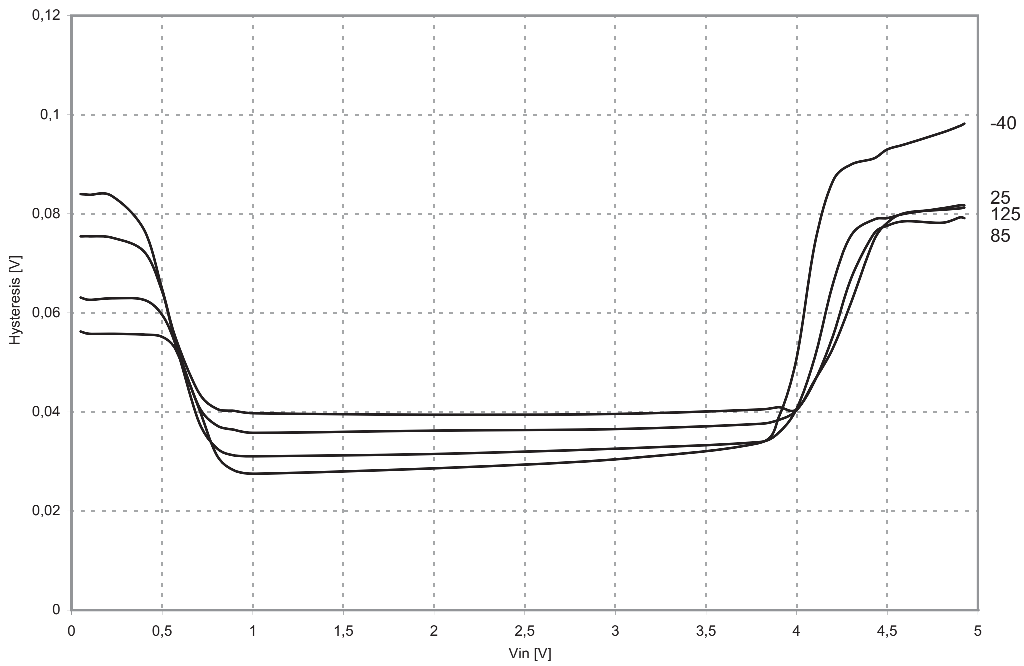


Figure 65. Analog Comparator Hysteresis vs. V_{IN} (V_{CC} = 5.0V)



3.14 Internal Oscillator Speed

3.14.1 8MHz Oscillator with CKDIV8 Enabled

Figure 66. Calibrated Oscillator Frequency vs. V_{CC} (One-point Calibration)

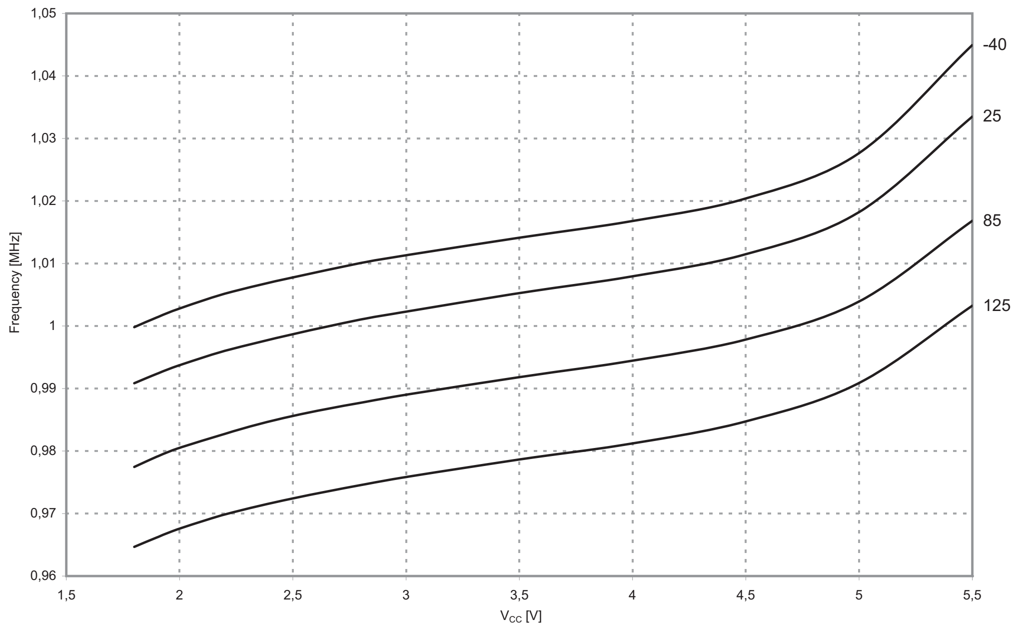


Figure 67. Calibrated Oscillator Frequency vs. V_{CC} (Two-point Calibration)

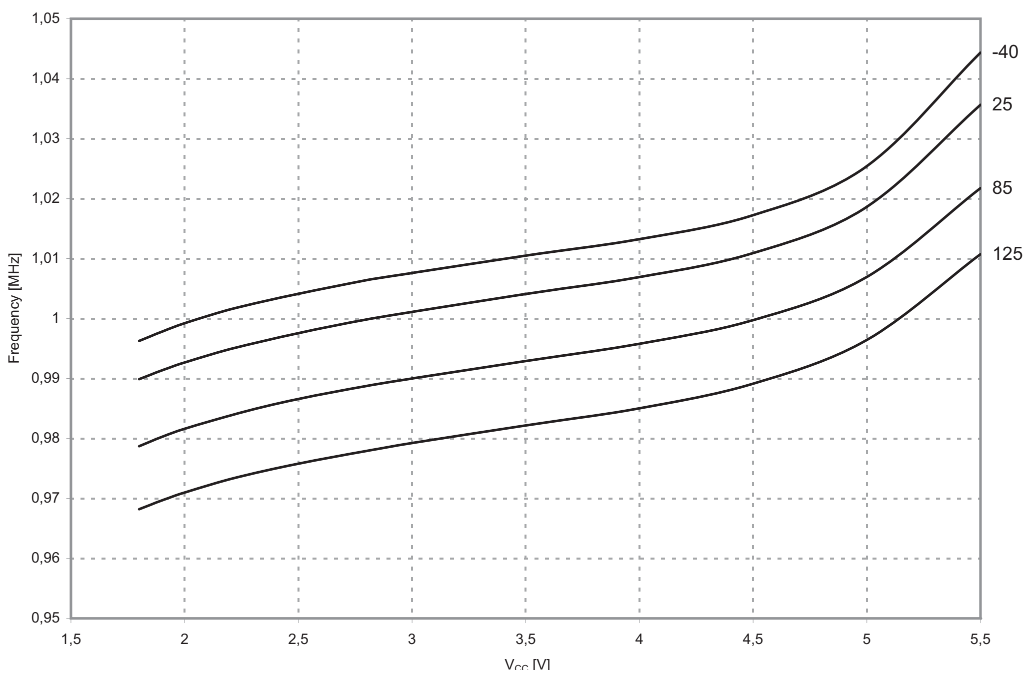


Figure 68. Calibrated Oscillator Frequency vs. Temperature (One-point Calibration)

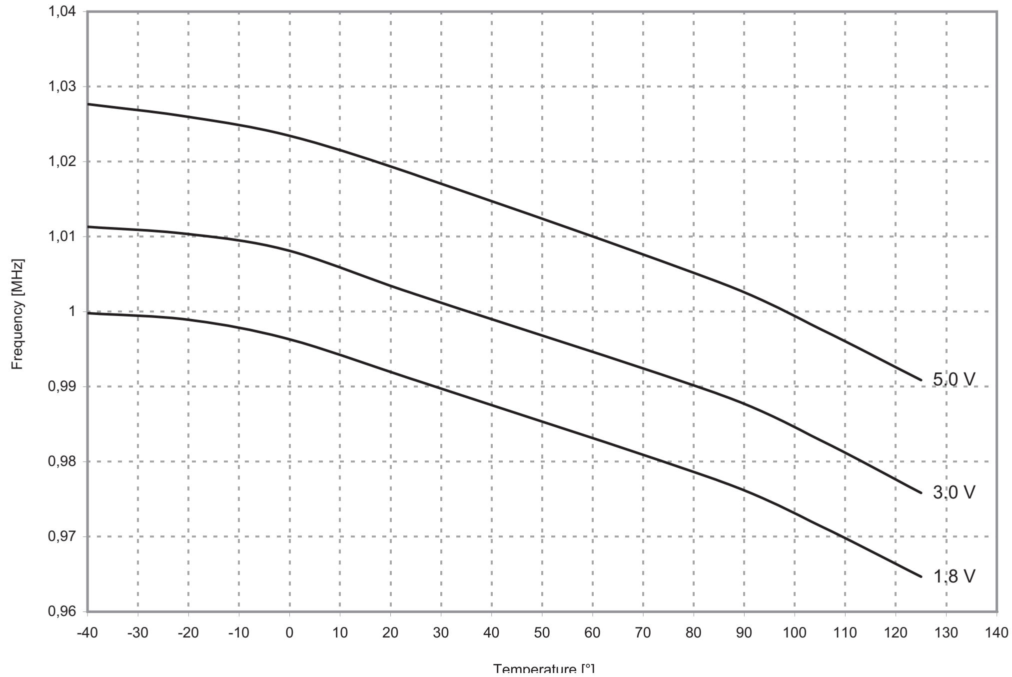


Figure 69. Calibrated Oscillator Frequency vs. Temperature (Two-point Calibration)

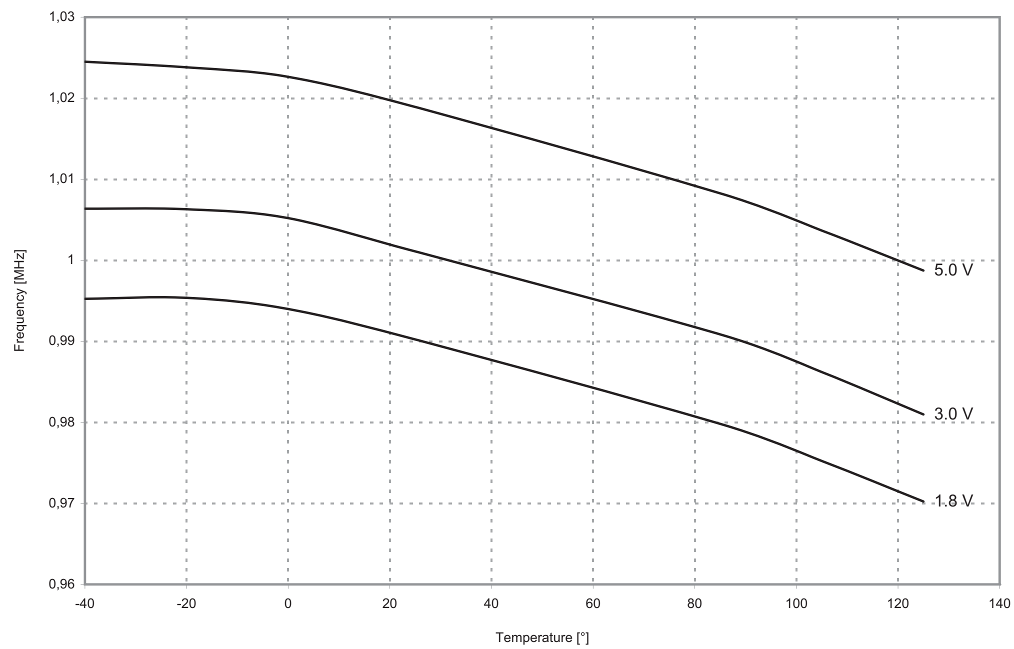
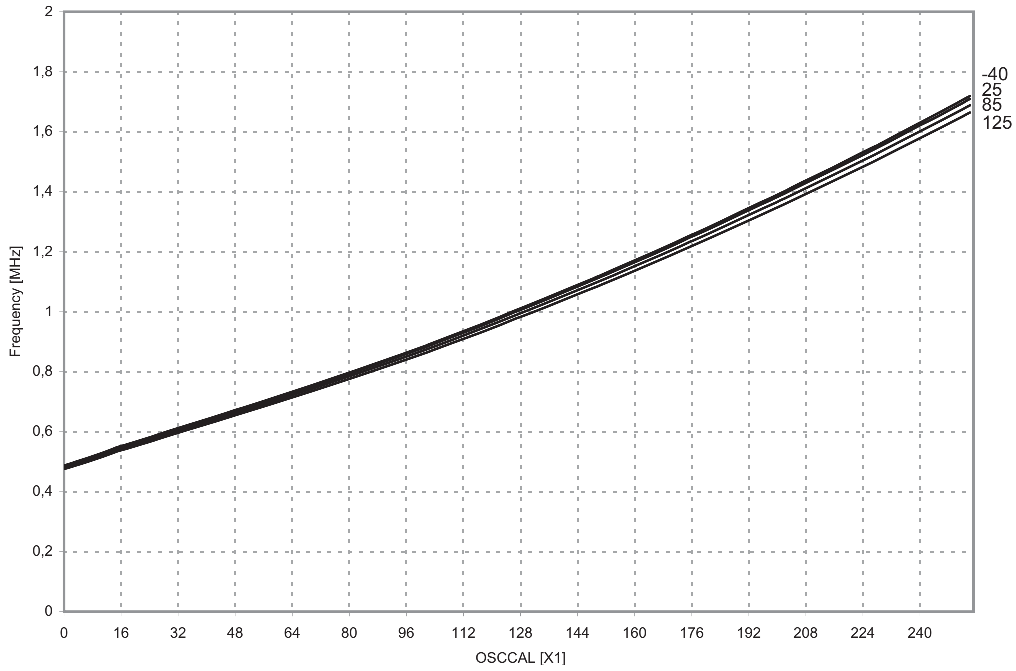


Figure 70. Calibrated Oscillator Frequency vs. OSCCAL0 Value



3.14.2 32kHz ULP Oscillator

Figure 71. ULP Oscillator Frequency vs. V_{CC}

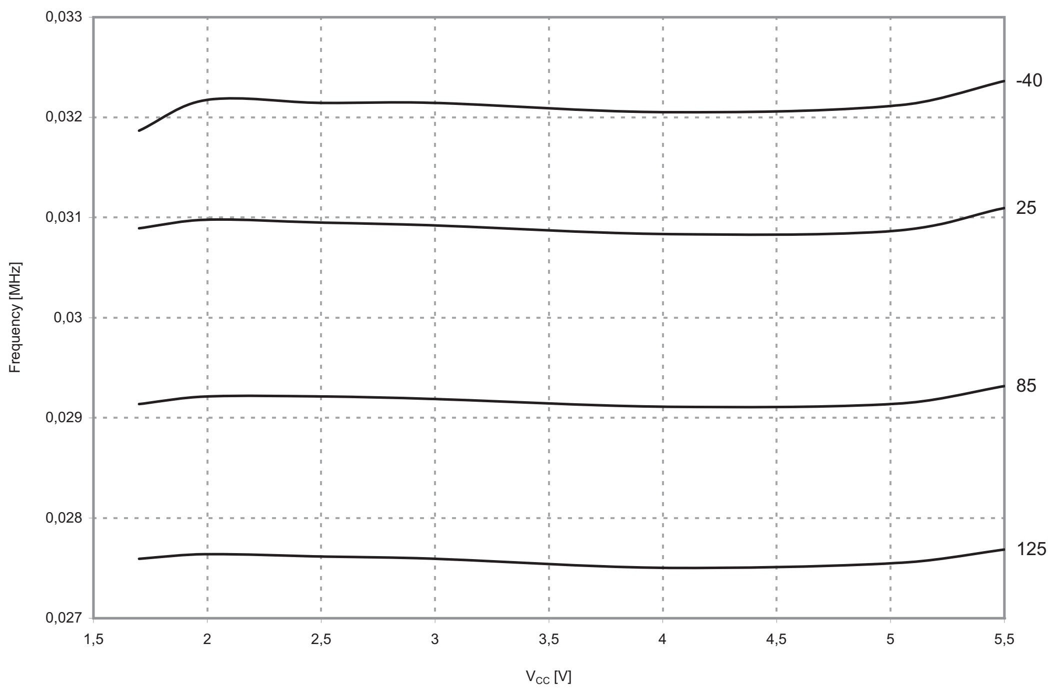


Figure 72. ULP Oscillator Frequency vs. Temperature

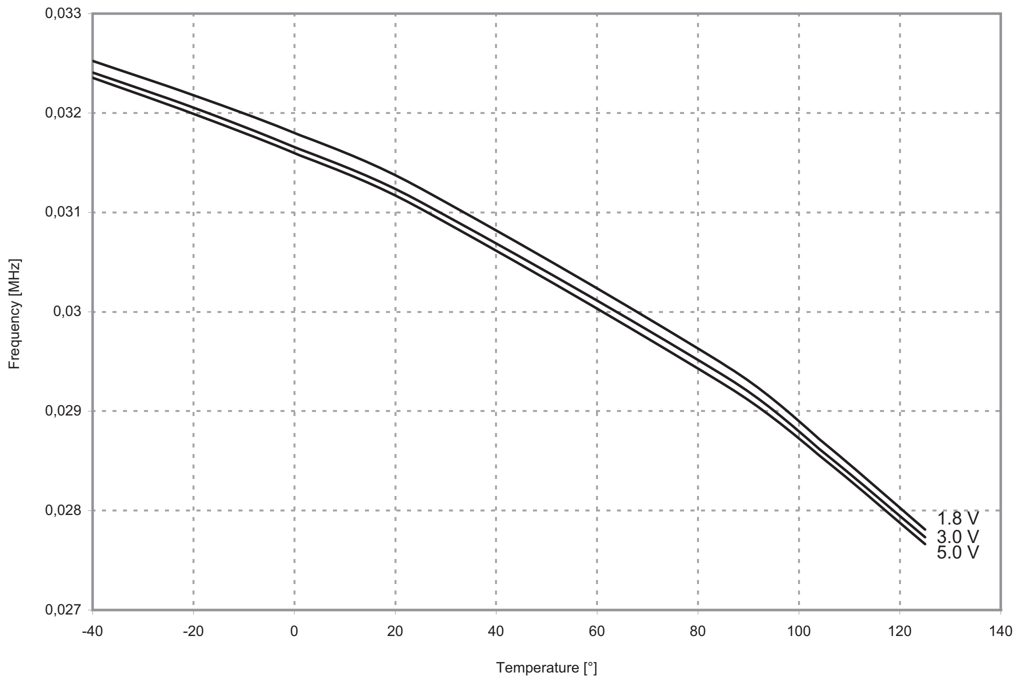
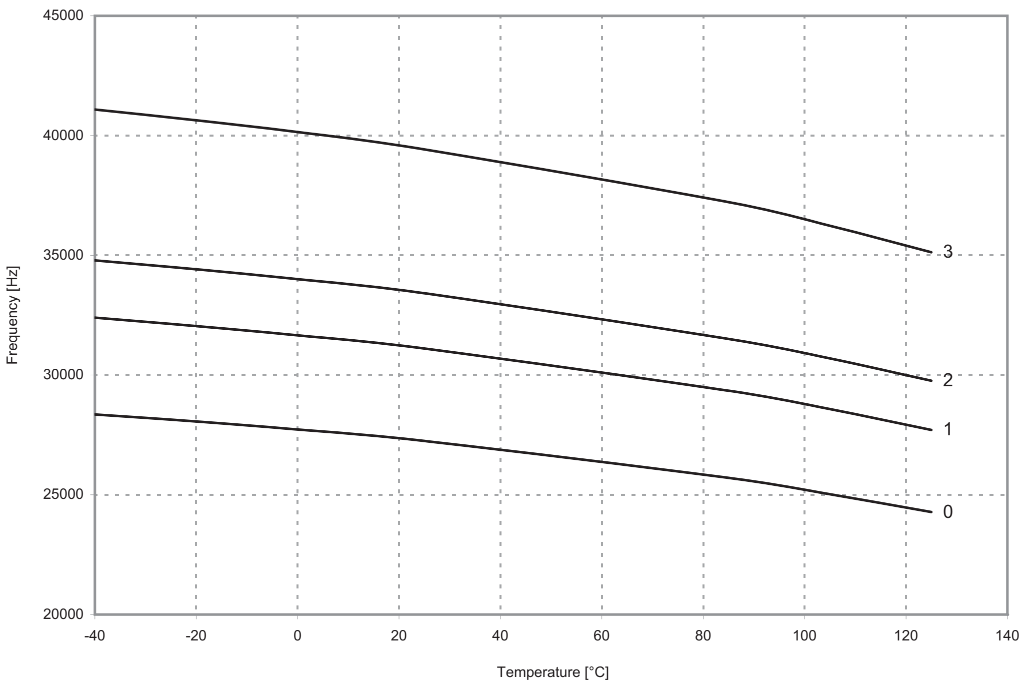


Figure 73. ULP Oscillator Frequency vs. OSCCAL1 Value



4. Ordering Information

4.1 ATtiny828

Speed (MHz) [1]	Supply Voltage (V) [1]	Temperature Range	Package [2]	Accuracy [3]	Ordering Code [4]
16 MHz	1.8 – 5.5V	Industrial [5] (-40°C to +125°C)	32A	±10%	ATtiny828-AF
				±2%	ATtiny828R-AF
				±10%	ATtiny828-AFR
				±2%	ATtiny828R-AFR
			32M1-A	±10%	ATtiny828-MF
				±2%	ATtiny828R-MF
				±10%	ATtiny828-MFR
				±2%	ATtiny828R-MFR

Notes: 1. For speed vs. supply voltage, see section "Speed" on page 5.

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Indicates accuracy of internal oscillator. See "Accuracy of Calibrated Internal Oscillator" on page 5.
4. Code indicators:
   - F: matte tin
   - R: tape & reel
5. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm, Quad Flat No-Lead (QFN)

5. Revision History

Revision	Comments
8371A: Appendix B – 02/2013	Initial document release.

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