
3-wire Automotive Temperature Serial EEPROM
2K (256 x 8 or 128 x 16) and 4K (512 x 8 or 256 x 16)

DATASHEET

Features

- Medium-voltage and Standard-voltage Operation
 - $V_{CC} = 2.5V$ to $5.5V$
- Automotive Temperature Range $-40^{\circ}C$ to $125^{\circ}C$
- User-selectable Internal Organization
 - 2K: 256 x 8 or 128 x 16
 - 4K: 512 x 8 or 256 x 16
- 3-wire Serial Interface
- Sequential Read Operation
- 2MHz Clock Rate
- Self-timed Write Cycle (5ms max)
- High Reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 100 Years
- Lead-free/Halogen-free Devices Available
- 8-lead JEDEC SOIC and 8-lead TSSOP Packages

Description

The Atmel® AT93C56B/66B provides 2,048/4,096 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM is organized as 128/256 words of 16 bits each when the ORG pin is connected to V_{CC} and 256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many automotive applications where low-power and low-voltage operations are essential. AT93C56B/66B is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages.

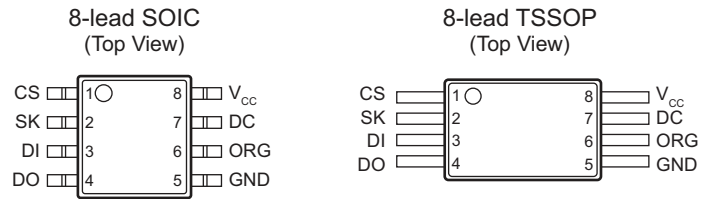
AT93C56B/66B is enabled through the Chip Select (CS) pin and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

AT93C56B/66B operates from 2.5V to 5.5V.

1. Pin Configuration and Pinouts

Figure 1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V _{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect



Note: Drawings are not to scale.

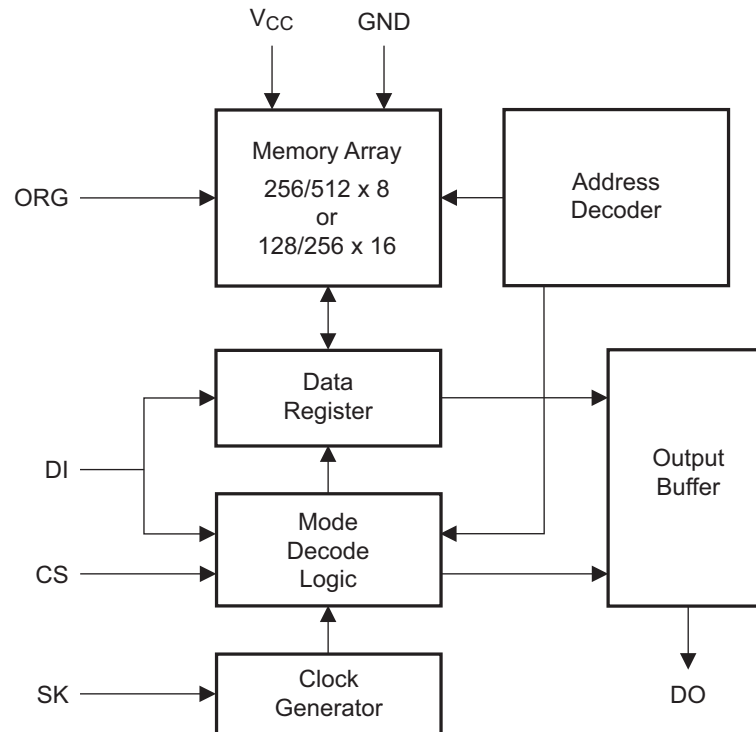
2. Absolute Maximum Ratings*

Operating Temperature -55°C to +125°C
Storage Temperature -65°C to +150°C
Voltage on any pin with respect to ground -1.0V to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

3. Block Diagram

Figure 3-1. Block Diagram



Note: When the ORG pin is connected to V_{CC} , the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal $1\text{m}\Omega$ pullup, then the “x 16” organization is selected.

4. Electrical Characteristics

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			2.5		5.5	V
V_{CC2}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 2.5\text{V}$	CS = 0V		3.0	10.0	μA
I_{SB2}	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V		10.0	15.0	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	3.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	3.0	μA
$V_{IL1}^{(1)}$	Input Low Voltage	$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6		0.8	V
$V_{IH1}^{(1)}$	Input High Voltage				2.0		$V_{CC} + 1$
V_{OL1}	Output Low Voltage	$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{m}$			0.4	V
V_{OH1}	Output High Voltage		$I_{OH} = -0.4\text{mA}$	2.4			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1$ TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		0		2	MHz
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		0		1	
t_{SKH}	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			ns
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			
t_{SKL}	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			ns
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			
t_{CS}	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			ns
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250			
t_{CSS}	CS Setup Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			
t_{DIS}	DI Setup Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
t_{PD1}	Output Delay to "1"	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			500	
t_{PD0}	Output Delay to "0"	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			500	
t_{SV}	CS to Status Valid	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			100	ns
			$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			150	
t_{WP}	Write Cycle Time		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			5	ms
Endurance ⁽¹⁾	5.0V, 25°C			1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

5. Instruction Set

Table 5-1. Instruction Set for the AT93C56B/66B

Instruction	SB	Opcode	Address		Data		Comments
			x 8	x 16	x 8	x 16	
Read	1	10	A8 – A0	A7 – A0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write enable must precede all programming modes.
Erase	1	11	A8 – A0	A7 – A0			Erase memory location An – A0.
Write	1	01	A8 – A0	A7 – A0	D7 – D0	D15 – D0	Writes memory location An – A0.
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	D7 – D0	D15 – D0	Writes all memory locations. Valid only at $V_{CC} = 5.0V \pm 10\%$ and Disable Register cleared.
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Disables all programming instructions.

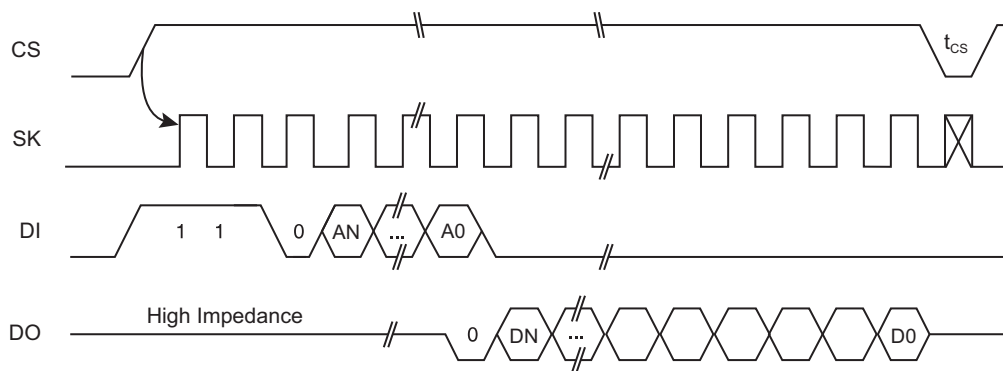
Note: The X in the address field represent *don't care* values and must be clocked.

6. Functional Description

AT93C56B/66B is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A *valid instruction starts with a rising edge of CS* and consists of a start bit (Logic 1) followed by the appropriate opcode and the desired memory address location.

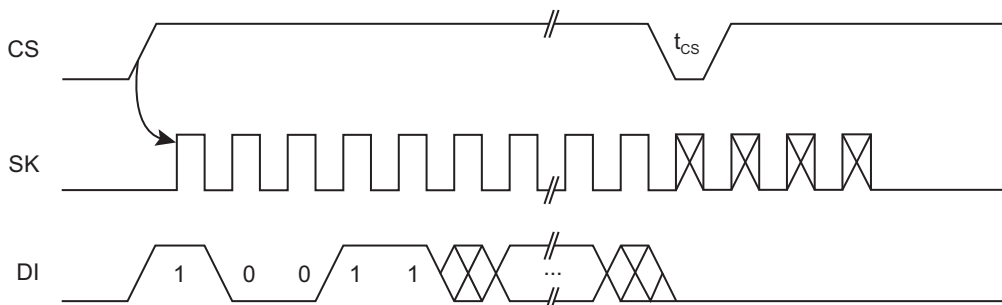
Read: The Read instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (Logic 0) precedes the 8- or 16-bit data output string. AT93C56B/66B supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic 0) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

Figure 6-1. Read Timing



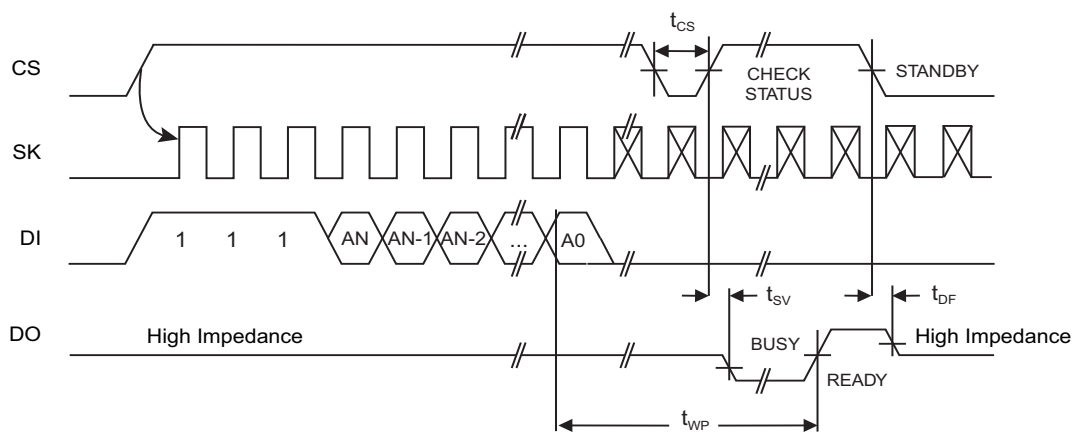
Erase/Write Enable (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

Figure 6-2. EWEN Timing



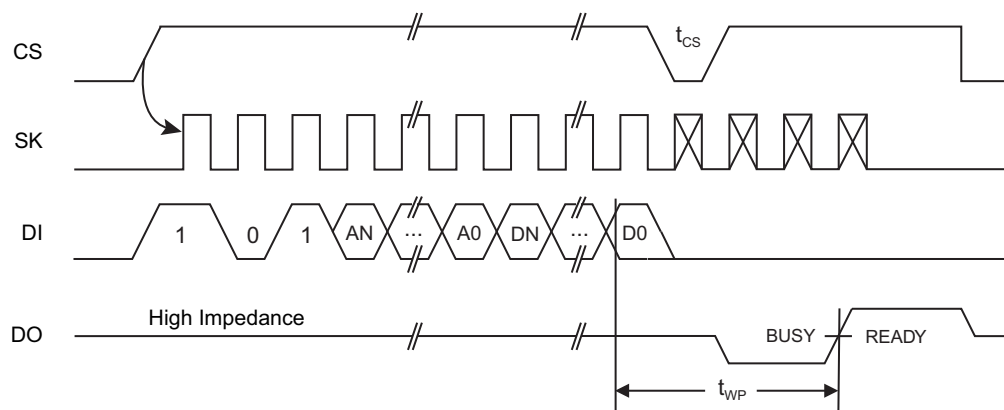
Erase: The Erase instruction programs all bits in the specified memory location to the Logical 1 state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

Figure 6-3. Erase Timing



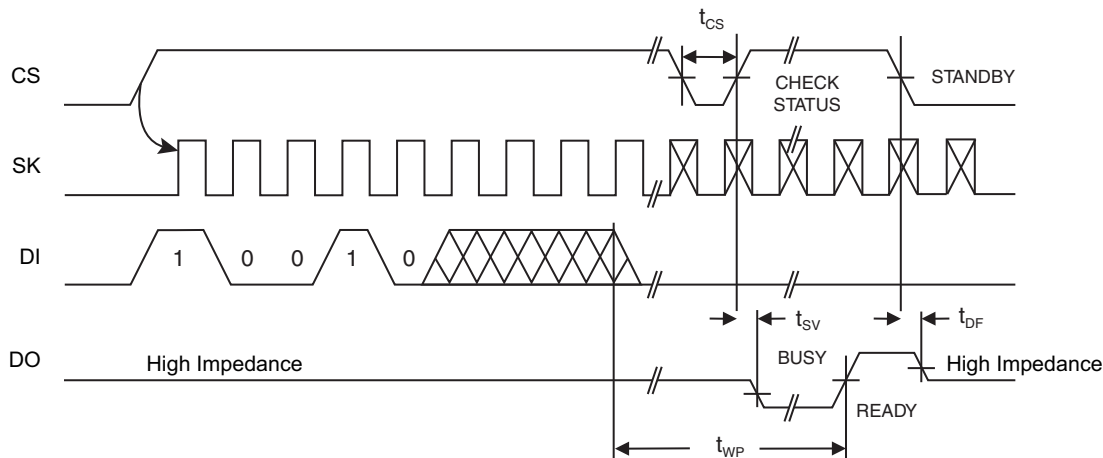
Write: The Write instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP} .

Figure 6-4. Write Timing



Erase All (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

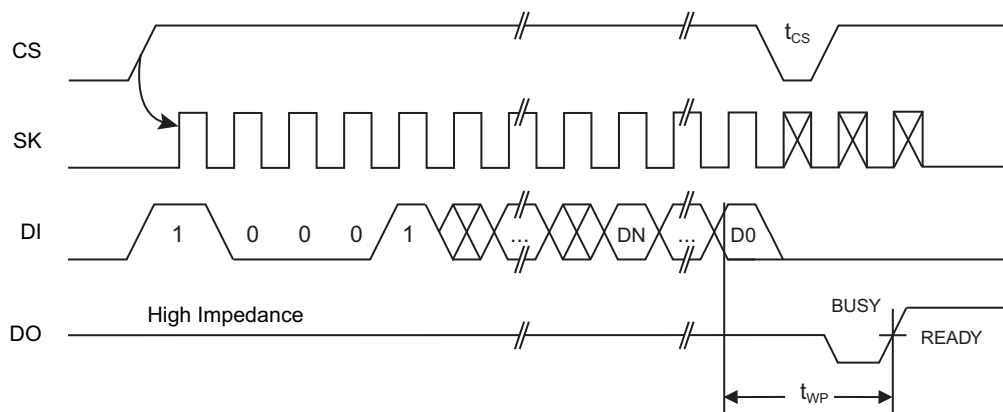
Figure 6-5. ERAL Timing



Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.

Write All (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

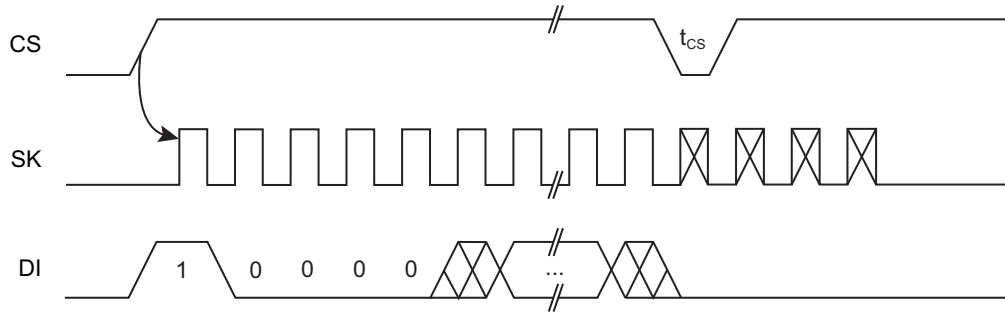
Figure 6-6. WRAL Timing



Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$

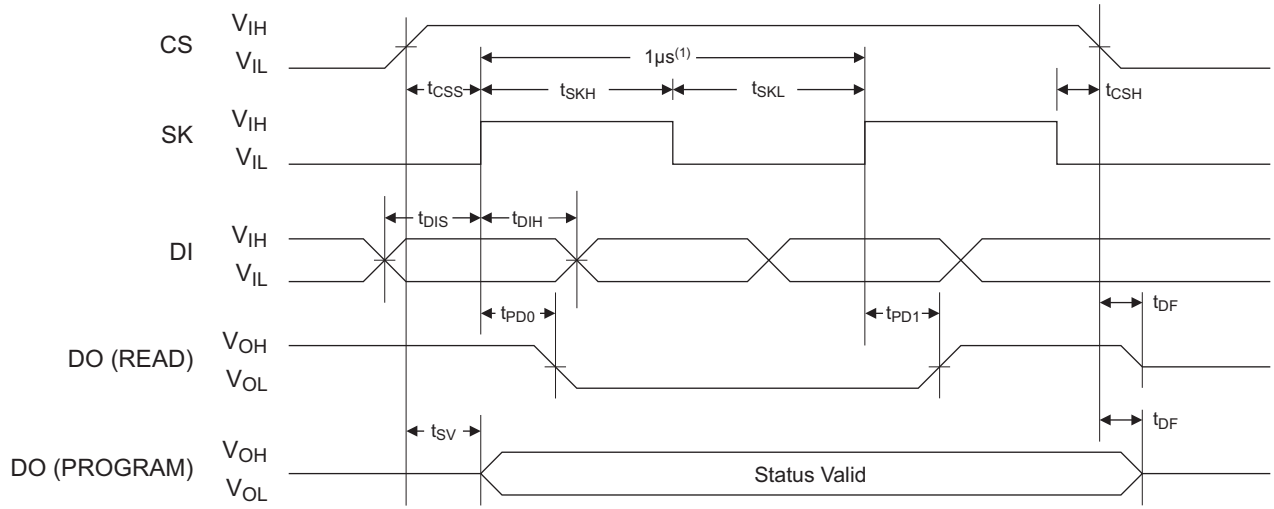
Erase/Write Disable (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Figure 6-7. EWDS Timing



7. Timing Diagrams

Figure 7-1. Synchronous Data Timing



Note: This is the minimum SK period.

Table 7-1. Organization Key for Timing Diagrams

I/O	AT93C56B (2K)		AT93C66B (4K)	
	x 8	x 16	x 8	x 16
AN	A8 ⁽¹⁾	A7 ⁽²⁾	A8	A7
DN	D7	D15	D7	D15

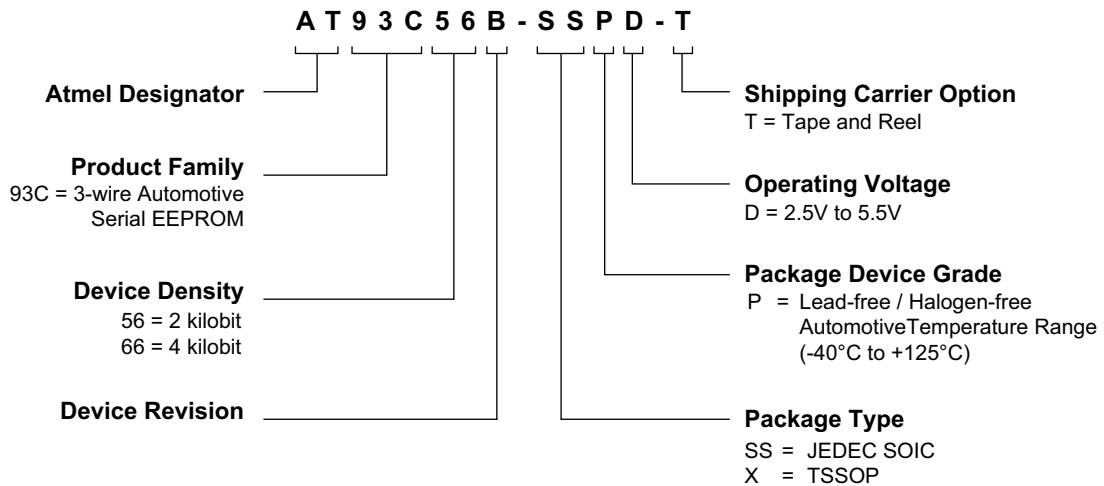
Notes: 1. A_8 is a *don't care* value, but the extra clock is required.
2. A_7 is a *don't care* value, but the extra clock is required.

7.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum device operating voltage. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100 μs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

8. Ordering Information

8.1 Ordering Code Detail



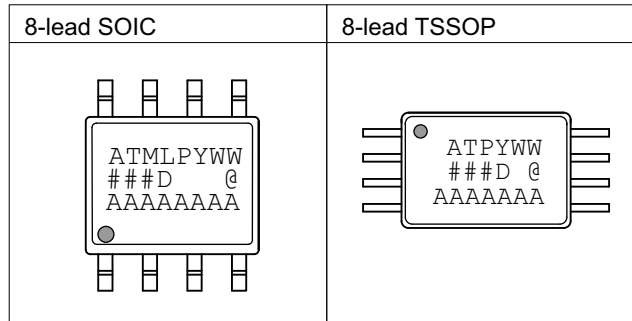
8.2 Atmel Ordering Code Information

Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT93C56B-SSPD-T	Lead-free Halogen-free	8S1	Tape and Reel	4,000 per Reel	Automotive Temperature (-40°C to 125°C)
AT93C56B-XPD-T		8X		5,000 per Reel	
AT93C66B-SSPD-T	Lead-free Halogen-free	8S1	Tape and Reel	4,000 per Reel	Automotive Temperature (-40°C to 125°C)
AT93C66B-XPD-T		8X		5,000 per Reel	

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

9. Product Markings

AT93C56B and AT93C66B: Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

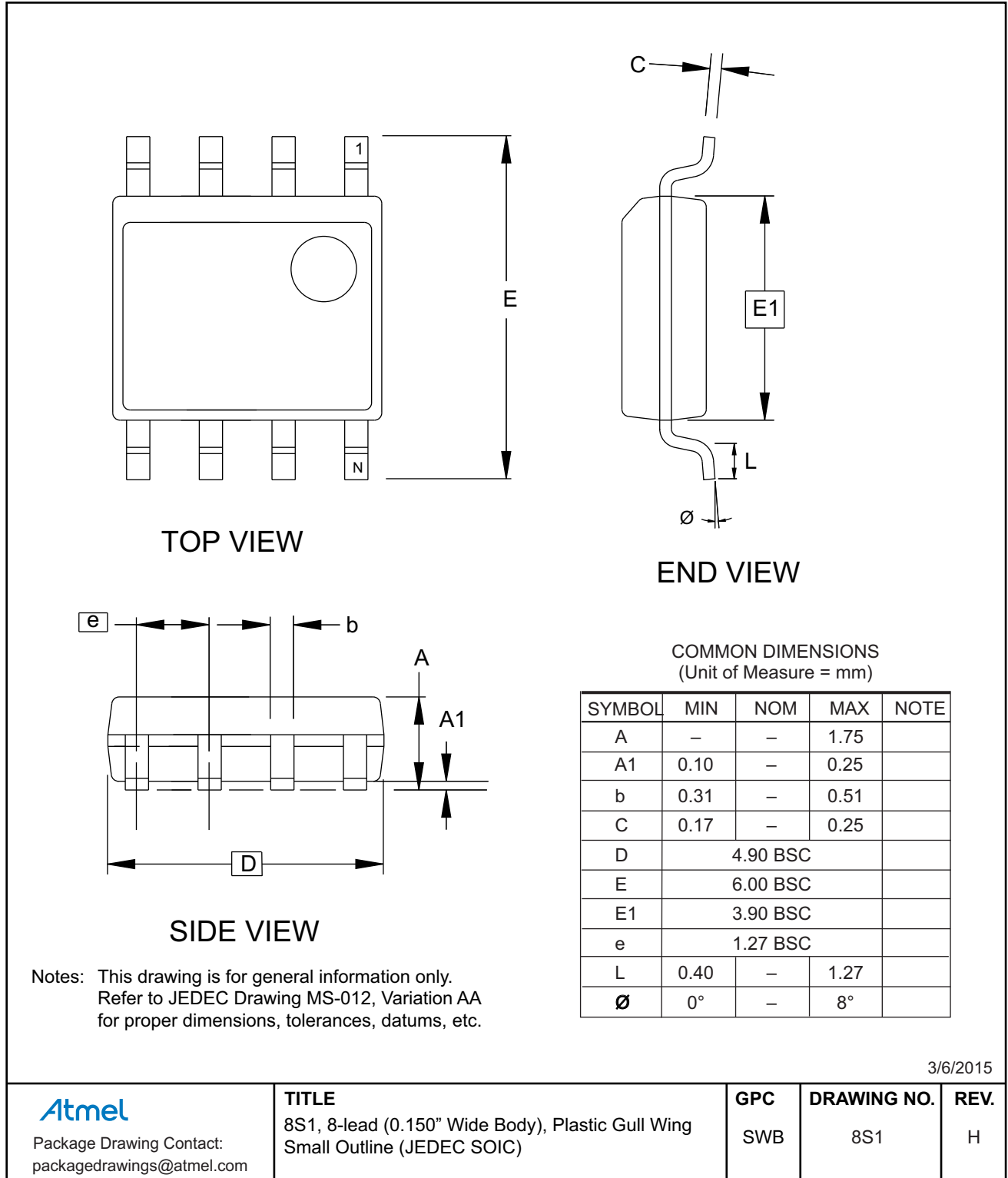
Catalog Number Truncation			
AT93C56B		Truncation Code ###: 56B	
AT93C66B		Truncation Code ###: 66B	
Date Codes			Voltagess
Y = Year	M = Month	WW = Work Week of Assembly	D: 2.5V min
2: 2012 6: 2016	A: January	02: Week 2	
3: 2013 7: 2017	B: February	04: Week 4	
4: 2014 8: 2018	
5: 2015 9: 2019	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	P: Automotive/NiPdAu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/15/12

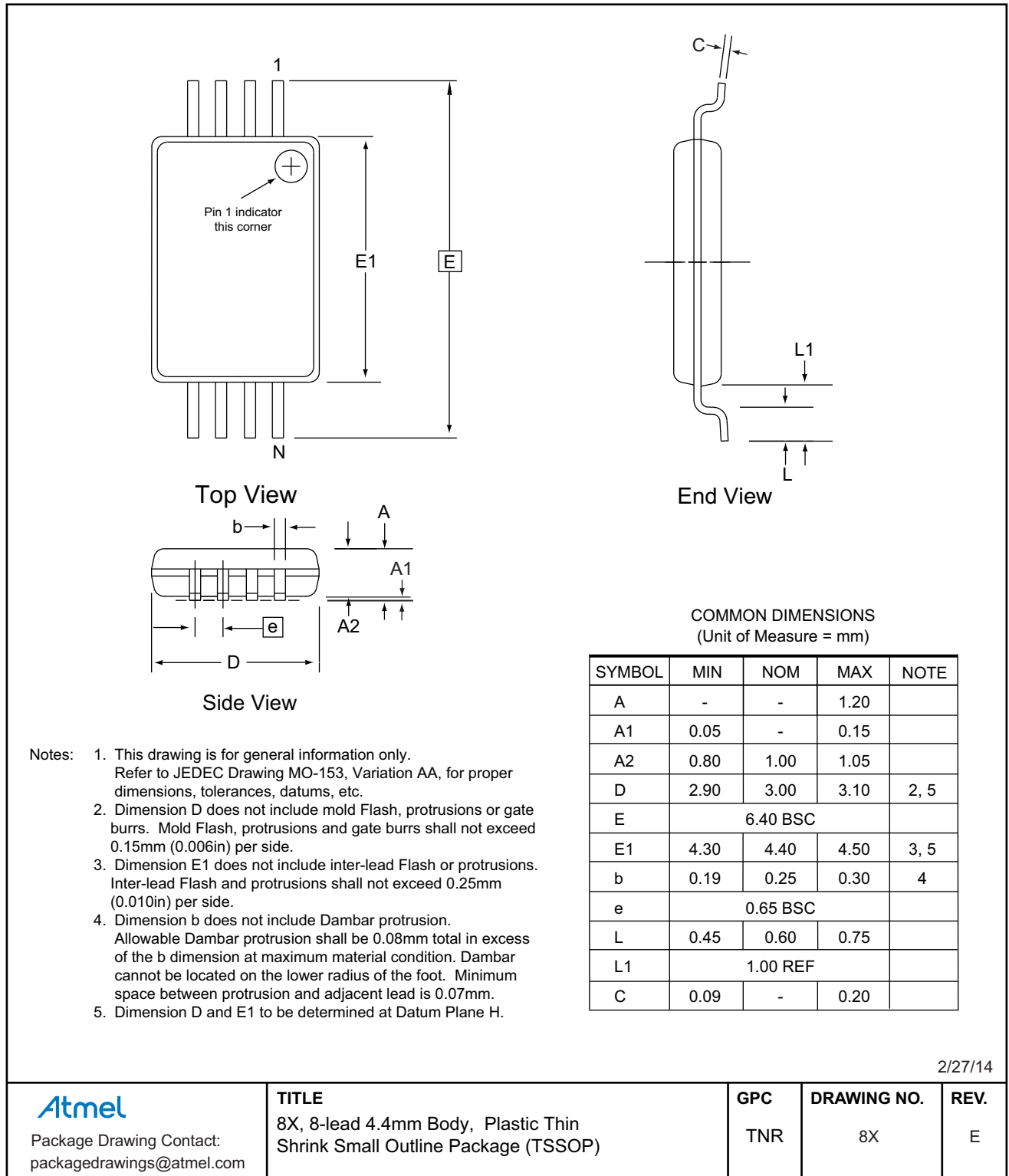
 Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	93C56-66BAM, AT93C56B and AT93C66B Automotive Package Marking Information	93C56-66BAM	C

10. Packaging Information

10.1 8S1 — 8-lead JEDEC SOIC



10.2 8X — 8-lead TSSOP



11. Revision History

Doc. Rev.	Date	Comments
8811C	02/2016	Updated 8S1 and 8X package drawings and ordering information. Added the ordering code detail. Removed bulk(tube) options. Document reorganization.
8811B	08/2012	Removed preliminary status. Updated Atmel logos and disclaimer/copy page.
8811A	06/2012	Initial document release

