## Features

- Utilizes the ARM7TDMI™ ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 8K Bytes Internal RAM
- Fully-programmable External Bus Interface (EBI)
  - 128 M Bytes of Maximum External Address Space
  - Up to 8 Chip Selects
  - Software Programmable 8-/16-bit External Databus
- 8-channel Peripheral Data Controller
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - Five External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 54 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - Six External Clock Inputs, Two Multi-purpose I/O Pins per Channel
- 2 USARTs
  - Two Dedicated Peripheral Data Controller (PDC) Channels per USART
  - Support for up to 9-bit Data Transfers
- 2 Master/Slave SPI Interfaces
  - Two Dedicated Peripheral Data Controller (PDC) Channels per SPI
  - 8-bit to 16-bit Programmable Data Length
  - Four External Slave Chip Selects per SPI
- 3 System Timers
  - Period Interval Timer (PIT), Real-time Timer (RTT) and Watchdog Timer (WDT)
- Power Management Controller (PMC)
  - Individual Deactivation of CPU and Peripherals
- Clock Generator with 32.768 kHz Low-power Oscillator and PLL
  - Support for 38.4 kHz Crystals
  - Software Programmable System Clock (up to 33 MHz)
- IEEE 1149.1 JTAG Boundary-scan on All Active Pins
- Fully Static Operation: 0 Hz to 33 MHz Internal Frequency Range at $V_{DDCORE}$ = 3.0 V, 85°C
- 2.7V to 3.6V Core Operating Range
- 2.7V to 5.5V I/O Operating Range
- 2.7V to 3.6V Oscillator and PLL Operating Range
- -40°C to +85°C Temperature Range
- Available in a 144-lead TQFP or 144-ball BGA Package

## Description

The AT91M42800A is a member of the Atmel AT91 16-/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low-power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91M42800A has a direct connection to off-chip memory, including Flash, through the External Bus Interface.

The Power Management Controller allows the user to adjust the device activity according to system requirements, and, with the 32.768 kHz low-power oscillator, enables the AT91M42800A to reduce power requirements to an absolute minimum.

The AT91M42800A is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with an on-chip RAM and a wide range of peripheral functions, including timers, serial communication controllers and a versatile clock generator on a monolithic chip, the Atmel AT91M42800A provides a highly-flexible and cost-effective solution to many compute-intensive applications.

# AT91 ARM® Thumb® Microcontrollers

# AT91M42800A Electrical Characteristics

Rev. 1776B–ATARM–06/02

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature (Industrial) | -40°C to + 85°C |
| Storage Temperature | -60°C to + 150°C |
| Voltage on Input Pin with Respect to Ground | -0.3V to +5.5V |
| Maximum Operating Voltage ($V_{DDCORE}$ and $V_{DDPLL}$) | 3.6V |
| Maximum Operating Voltage ($V_{DDIO}$) | 5.5V |
| DC Output Current ($V_{DDIO}$) | 6 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

The following characteristics are applicable over the Operating Temperature range: $T_A$ = -40°C to +85°C, unless otherwise specified and are certified for a Junction Temperature up to $T_J$ = 100°C.

**Table 1.** DC Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{DDCORE}$ | DC Supply Core | | | 2.7 | | 3.6 | V |
| $V_{DDPLL}$ | DC Supply Oscillator and PLL | | | $V_{DDCORE}$ | | 3.6 | V |
| $V_{DDIO}$ | DC Supply Digital I/Os | | | $V_{DDCORE}$ | | $V_{DDCORE}$ + 2.0 or 5.5 | V |
| $V_{IL}$ | Input Low-level Voltage | | | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High-level Voltage | | | 2 | | $V_{DD}$ + 0.3(1) | V |
| $V_{OL}$ | Output Low-level Voltage | $I_{OL}$ = 8 mA(2) | | | | 0.4 | V |
| | | $I_{OL}$ = 0 mA(2) | | | | 0.2 | V |
| $V_{OH}$ | Output High-level Voltage | $I_{OH}$ = 8 mA(2) | | $V_{DD}$ - 0.4(1) | | | V |
| | | $I_{OH}$ = 0 mA(2) | | $V_{DD}$ - 0.2(1) | | | V |
| $I_{LEAK}$ | Input Leakage Current | | | | | 4 | µA |
| $I_{PULL}$ | Input Pull-up Current | $V_{DD}$ = 3.6V(1), $V_{IN}$ = 0 | | | | 280 | µA |
| $C_{IN}$ | Input Capacitance | 144-TQFP Package | | | | 8 | pF |
| $I_{SC}$ | Static Current | $V_{DD}$(1) = $V_{DDCORE}$ = 3.6V, MCK = 0 Hz | $T_A$ = 25°C | | | 20 | µA |
| | | All inputs driven TMS, TDI, TCK, NRST = 1 | $T_A$ = 85°C | | | 400 | |

Notes: 1. $V_{DD}$ is applicable to $V_{DDIO}$ and $V_{DDPLL}$.
2. $I_O$ = Output Current.

## Power Consumption

The values in the following tables are measured values in the operating conditions indicated (i.e., $V_{DDIO}$ = 3.3V, $V_{DDCORE}$ = 3.3V, $T_A$ = 25°C) on the AT91EB42 Evaluation Board. They represent the power consumption on the $V_{DDCORE}$ power supply, unless otherwise specified.

**Table 2.** Power Consumption

| Mode | Conditions | Consumption | Unit |
|---|---|---|---|
| Normal | Fetch in ARM mode out of internal SRAM<br>All peripheral clocks activated | 6.47 | mW/MHz |
| | Fetch in ARM mode out of internal SRAM<br>All peripheral clocks deactivated | 4.51 | |
| Idle | All peripheral clocks activated | 3.74 | |
| | All peripheral clocks deactivated | 1.67 | |

**Table 3.** Power Consumption per Peripheral

| Peripheral | | Consumption | Unit |
|---|---|---|---|
| PIO Controller | | 0.77 | mW/MHz |
| Timer/Counter Channel | | 0.12 | |
| Timer/Counter Block (3 Channels) | | 0.33 | |
| USART | | 0.36 | |
| SPI | | 0.42 | |
| PLLA(1) | $F_{OUT}$ = 3 MHz | 0.812 | mW |
| PLLA(1) | $F_{OUT}$ = 8 MHz | 1.33 | |
| PLLA(1) | $F_{OUT}$ = 16 MHz | 2.1 | |
| PLLA(1) | $F_{OUT}$ = 20 MHz | 2.2 | |
| PLLB(2) | $F_{OUT}$ = 20 MHz | 1.31 | |
| PLLB(2) | $F_{OUT}$ = 32.7 MHz | 1.81 | |

Notes:
1. Power consumption on the $V_{DDPLL}$ power supply. $F_{OSC}$ = 32.768 kHz and the loop filter values are R = 1.5 kΩ, $C_1$ = 100 nF, $C_2$ = 10 nF
2. Power consumption on the $V_{DDPLL}$ power supply. $F_{OSC}$ = 32.768 kHz and the loop filter values are R = 680Ω, $C_1$ = 1µF, $C_2$ = 100 nF

## Thermal and Reliability Considerations

### Thermal Data

In Table 4, the device lifetime is estimated with the MIL-217 standard in the “moderately controlled” environmental model (this model is described as corresponding to an installation in a permanent rack with adequate cooling air), depending on the device Junction Temperature. (For details see the section “Junction Temperature” on page 5.)

Note that the user must be extremely cautious with this MTBF calculation: as the MIL-217 model is pessimistic with respect to observed values due to the way the data/models are obtained (test under severe conditions). The life test results that have been measured are always better than the predicted ones.

**Table 4.** MTBF Versus Junction Temperature

| Junction Temperature ($T_J$) (C°) | Estimated Lifetime (MTBF) (Year) |
|---|---|
| 100 | 31 |
| 125 | 17 |
| 150 | 10 |
| 175 | 6 |

Table 5 summarizes the thermal resistance data related to the package of interest.

**Table 5.** Thermal Resistance Data

| Symbol | Parameter | Condition | Package | Typ | Unit |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | Still Air | TQFP144 | 37 | °C/W |
| | | | PBGA144 | 57 | |
| $\theta_{JC}$ | Junction-to-case thermal resistance | | TQFP144 | 10.9 | |
| | | | PBGA144 | 19.9 | |

### Reliability Data

The number of gates and the device die size are provided for the user to calculate reliability data with another standard and/or in another environmental model.

**Table 6.** Reliability Data

| Parameter | Data | Unit |
|---|---|---|
| Number of Logic Gates | 516 | K gates |
| Number of Memory Gates | 400 | K gates |
| Device Die Size | 22.9 | $mm^2$ |

## Junction Temperature

The average chip-junction temperature $T_J$ in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

Where:

- $\theta_{JA}$ = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 5 on page 4.
- $\theta_{JC}$ = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 5 on page 4.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- $P_D$ = device power consumption (W) estimated from data provided in the section “Power Consumption” on page 3.
- $T_A$ = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and thereby decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature $T_J$ in °C.

# Conditions

## Timing Results

The delays are given as typical values in the following conditions:

- $V_{DDIO} = V_{DDCORE} = 3.3V$
- Ambient Temperature = 25°C
- Load Capacitance = 0 pF
- The output level change detection is *0.5 x* $V_{DDIO}$
- The input level is *0.3 x* $V_{DDIO}$ for a low-level detection and is *0.7 x* $V_{DDIO}$ for a high level detection.

The minimum and maximum values given in the AC characteristics tables of this datasheet take into account the process variation and the design.

In order to obtain the timing for other conditions, the following equation should be used:

$$t = \delta_{T^\circ} \times ((\delta_{VDDCORE} \times t_{DATASHEET}) + (\delta_{VDDIO} \times \sum (C_{SIGNAL} \times \delta_{CSIGNAL})))$$

Where:

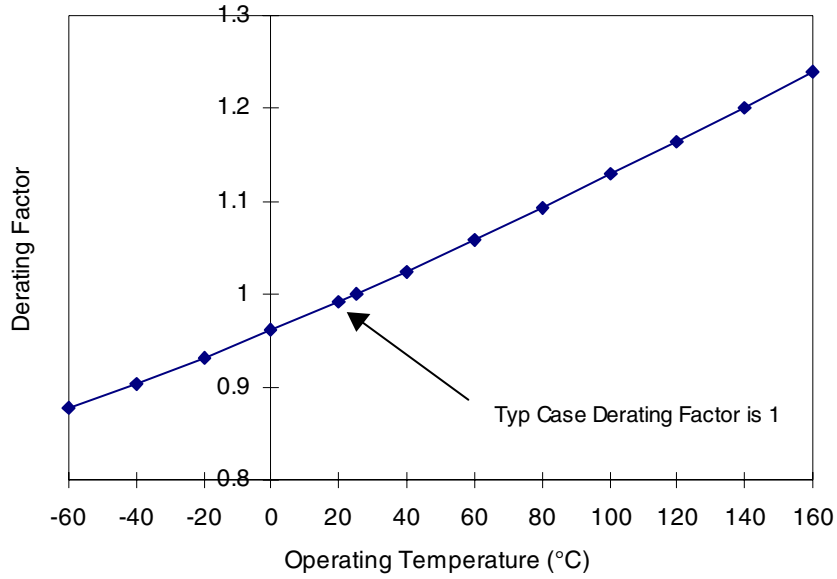
- $\delta_{T^\circ}$ is the derating factor in temperature given in Figure 1.
- $\delta_{VDDCORE}$ is the derating factor for the Core Power Supply given in Figure 2.
- $t_{DATASHEET}$ is the minimum or maximum timing value given in this datasheet for a load capacitance of 0 pF.
- $\delta_{VDDIO}$ is the derating factor for the IO Power Supply given in Figure 3.
- $C_{SIGNAL}$ is the capacitance load on the considered output pin.(1)
- $\delta_{CSIGNAL}$ is the load derating factor depending on the capacitance load on the related output pins given in Min and Max values in this datasheet.

The input delays are given as typical values.

Note: 1. The user must take into account the package capacitance load contribution ($C_{IN}$) described in Table 1 on page 2.

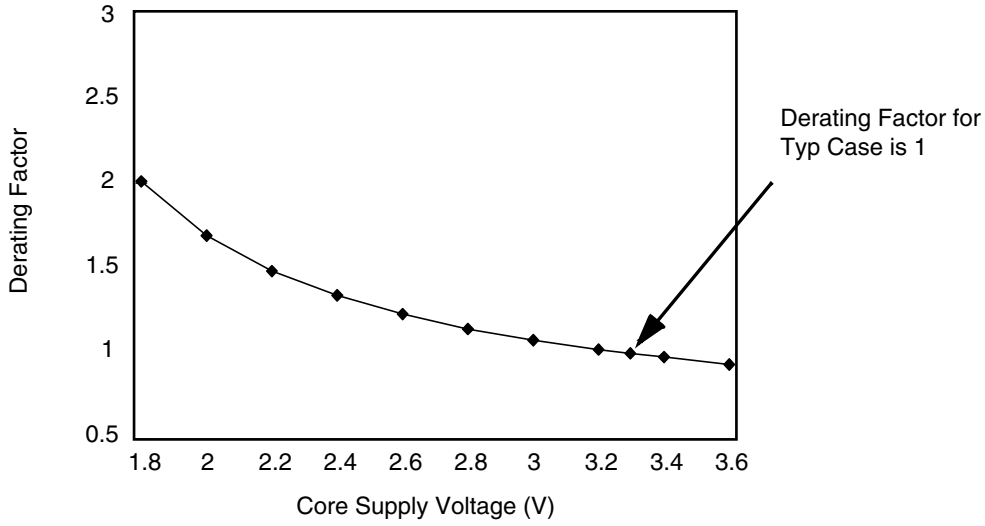
## Temperature Derating Factor

**Figure 1.** Derating Curve for Different Operating Temperatures



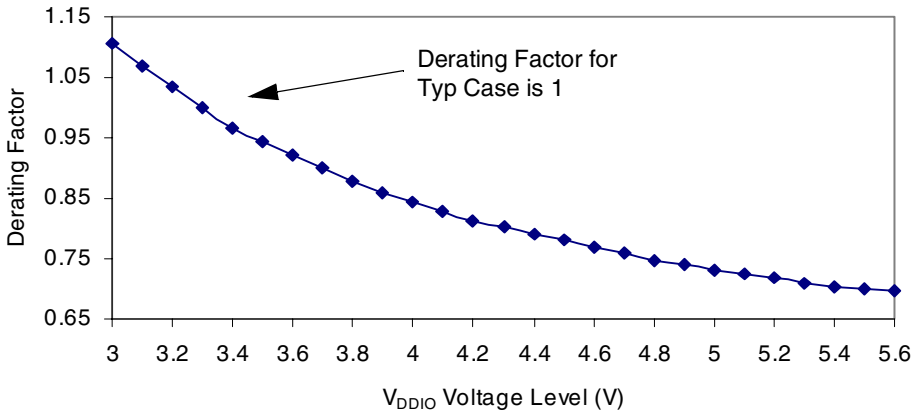
## Core Voltage Derating Factor

**Figure 2.** Derating Curve for Different Core Supply Voltages




## IO Voltage Derating Factor

**Figure 3.** Derating Curve for Different $V_{DDIO}$ Power Supply Levels



## Crystal Oscillator Characteristics

**Table 7.** Oscillator Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $1/(t_{CPOSC})$ | Crystal Oscillator Frequency | | | 32.768 | | kHz |
| $C_{L1}$, $C_{L2}$ | Internal Load Capacitance ($C_{L1} = C_{L2}$) | | | 20 | | pF |
| $C_L$ | Equivalent Load Capacitance | $C_{L1} = C_{L2} = 20$ pF | | 10 | | pF |
| | Duty Cycle | Measured at the MCKO output pin | 45 | 50 | 55 | % |
| $t_{ST}$ | Startup Time | | | | 1.5 | s |

## Clock Waveforms

**Table 8.** Master Clock Waveform Parameters

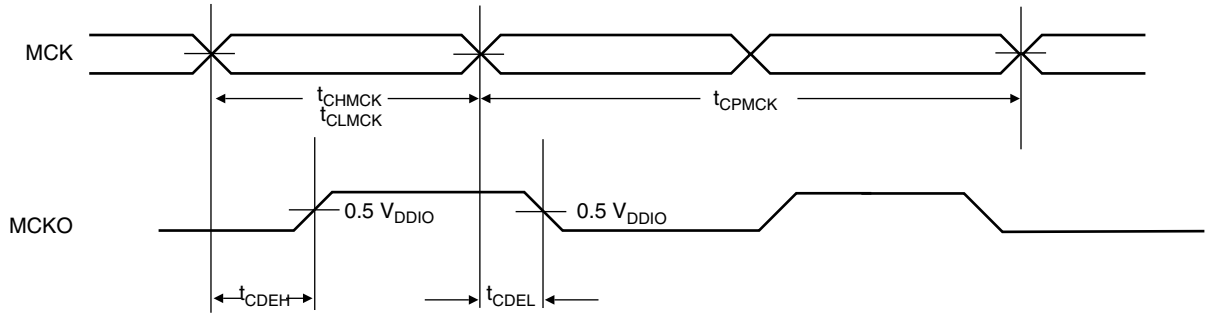
| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $1/(t_{CPMCK})$ | Master Clock Frequency | | | 38.1 | MHz |
| $t_{CPMCK}$ | Master Clock Period | | 26.2 | | ns |
| $t_{CHMCK}$ | Master Clock High Half-period | | 0.45 x $t_{CPMCK}$ | 0.55 x $t_{CPMCK}$ | ns |
| $t_{CLMCK}$ | Master Clock Low Half-period | | 0.45 x $t_{CPMCK}$ | 0.55 x $t_{CPMCK}$ | ns |

**Table 9.** Clock Propagation Times

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{CDEH}$ (1) | MCK Edge to MCKO Rising Edge | $C_{MCKO}$ = 0 pF | 7.8 | 12.3 | ns |
| | | $C_{MCKO}$ derating | 0.024 | 0.037 | ns/pF |
| $t_{CDEL}$ (1) | MCK Edge to MCKO Falling Edge | $C_{MCKO}$ = 0 pF | 8.2 | 12.8 | ns |
| | | $C_{MCKO}$ derating | 0.027 | 0.042 | ns/pF |

Note: 1. Applicable only when MCKO outputs Master Clock or inverted Master Clock.

**Figure 4.** Clock Waveform




## PMC Characteristics

**Table 10.** Master Clock Source Switch Times

| MCK Source | | Switch Time | | |
|---|---|---|---|---|
| From | To | Min | Typ | Max |
| Oscillator Output | PLL Output | | 3 x $t_{CPSLCK}$ + 2.5 x $t_{CPPLL}$ | |
| PLL Output | Oscillator Output | | 3.5 x $t_{CPSLCK}$ + 2.5 x $t_{CPPLL}$ | |

# AC Characteristics

## EBI Signals Relative to MCK

The following tables show timings relative to operating condition limits defined in the section “Timing Results” on page 6.

**Table 11.** General-purpose EBI Signals

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $EBI_1$ | MCK Falling to NUB Valid | $C_{NUB}$ = 0 pF | 8.3 | 18.8 | ns |
| | | $C_{NUB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_2$ | MCK Falling to NLB/A0 Valid | $C_{NLB}$ = 0 pF | 7 | 14.8 | ns |
| | | $C_{NLB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_3$ | MCK Falling to A1 - A23 Valid | $C_{ADD}$ = 0 pF | 6.7 | 15.8 | ns |
| | | $C_{ADD}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_4$ | MCK Falling to Chip Select Change | $C_{NCS}$ = 0 pF | 7.6 | 17.6 | ns |
| | | $C_{NCS}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_5$ | NWAIT Setup before MCK Rising | | 2.1 | | ns |
| $EBI_6$ | NWAIT Hold after MCK Rising | | 5.2 | | ns |

**Table 12.** EBI Write Signals

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $EBI_7$ | MCK Rising to NWR Active (No Wait States) | $C_{NWR}$ = 0 pF | 8.2 | 13.6 | ns |
| | | $C_{NWR}$ derating | 0.029 | 0.045 | ns/pF |
| $EBI_8$ | MCK Rising to NWR Active (Wait States) | $C_{NWR}$ = 0 pF | 8.5 | 14.1 | ns |
| | | $C_{NWR}$ derating | 0.029 | 0.045 | ns/pF |
| $EBI_9$ | MCK Falling to NWR Inactive (No Wait States) | $C_{NWR}$ = 0 pF | 8.1 | 13.4 | ns |
| | | $C_{NWR}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{10}$ | MCK Rising to NWR Inactive (Wait States) | $C_{NWR}$ = 0 pF | 8.3 | 13.9 | ns |
| | | $C_{NWR}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{11}$ | MCK Rising to D0 - D15 Out Valid | $C_{DATA}$ = 0 pF | 6.8 | 13.4 | ns |
| | | $C_{DATA}$ derating | 0 | 0.045 | ns/pF |
| $EBI_{12}$ | NWR High to NUB Change | $C_{NUB}$ = 0 pF | 5.3 | 11.3 | ns |
| | | $C_{NUB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{13}$ | NWR High to NLB/A0 Change | $C_{NLB}$ = 0 pF | 4.5 | 7.6 | ns |
| | | $C_{NLB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{14}$ | NWR High to A1 - A23 Change | $C_{ADD}$ = 0 pF | 4.2 | 9.7 | ns |
| | | $C_{ADD}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{15}$ | NWR High to Chip Select Inactive | $C_{NCS}$ = 0 pF | 4.9 | 11.4 | ns |
| | | $C_{NCS}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{16}$ | Data Out Valid before NWR High (No Wait States)[1] | C = 0 pF | $t_{CHMCK}$ - 0.7 | | ns |
| | | $C_{DATA}$ derating | -0.045 | | ns/pF |
| | | $C_{NWR}$ derating | 0.035 | | ns/pF |
| $EBI_{17}$ | Data Out Valid before NWR High (Wait States)[1] | C = 0 pF | n x $t_{CPMCK}$ - 0.3[2] | | ns |
| | | $C_{DATA}$ derating | -0.045 | | ns/pF |
| | | $C_{NWR}$ derating | 0.035 | | ns/pF |
| $EBI_{18}$ | Data Out Valid after NWR High | | 3 | | ns |
| $EBI_{19}$ | NWR Minimum Pulse Width (No Wait States)[1] | $C_{NWR}$ = 0 pF | $t_{CHMCK}$ - 0.9 | | ns |
| | | $C_{NWR}$ derating | -0.01 | | ns/pF |
| $EBI_{20}$ | NWR Minimum Pulse Width (Wait States)[1] | $C_{NWR}$ = 0 pF | n x $t_{CPMCK}$ - 1.0[2] | | ns |
| | | $C_{NWR}$ derating | -0.01 | | ns/pF |

Notes: 1. The derating should not be applied to $t_{CHMCK}$ or $t_{CPMCK}$.
2. n = number of standard wait states inserted.

**Table 13.** EBI Read Signals

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $EBI_{21}$ | MCK Falling to NRD Active(1) | $C_{NRD}$ = 0 pF | 8.1 | 14.3 | ns |
| | | $C_{NRD}$ derating | 0.029 | 0.045 | ns/pF |
| $EBI_{22}$ | MCK Rising to NRD Active(2) | $C_{NRD}$ = 0 pF | 7.8 | 13.5 | ns |
| | | $C_{NRD}$ derating | 0.029 | 0.045 | ns/pF |
| $EBI_{23}$ | MCK Falling to NRD Inactive(1) | $C_{NRD}$ = 0 pF | 7.9 | 13.9 | ns |
| | | $C_{NRD}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{24}$ | MCK Falling to NRD Inactive(2) | $C_{NRD}$ = 0 pF | 7.8 | 12.3 | ns |
| | | $C_{NRD}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{25}$ | D0 - D15 In Setup before MCK Falling Edge(5) | | -2.1 | | ns |
| $EBI_{26}$ | D0 - D15 In Hold after MCK Falling Edge(5) | | 6.2 | | ns |
| $EBI_{27}$ | NRD High to NUB Change | $C_{NUB}$ = 0 pF | 6.4 | 12.7 | ns |
| | | $C_{NUB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{28}$ | NRD High to NLB/A0 Change | $C_{NLB}$ = 0 pF | 5.4 | 8.8 | ns |
| | | $C_{NLB}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{29}$ | NRD High to A1 - A23 Change | $C_{ADD}$ = 0 pF | 5.1 | 11 | ns |
| | | $C_{ADD}$ derating | 0.022 | 0.045 | ns/pF |
| $EBI_{30}$ | NRD High to Chip Select Inactive | $C_{NCS}$ = 0 pF | 5.8 | 12.6 | ns |
| | | $C_{NCS}$ derating | 0.022 | 0.035 | ns/pF |
| $EBI_{31}$ | Data Setup before NRD High(5) | $C_{NRD}$ = 0 pF | 10.7 | | ns |
| | | $C_{NRD}$ derating | 0.035 | | ns/pF |
| $EBI_{32}$ | Data Hold after NRD High(5) | $C_{NRD}$ = 0 pF | -3.9 | | ns |
| | | $C_{NRD}$ derating | -0.022 | | ns/pF |
| $EBI_{33}$ | NRD Minimum Pulse Width(1)(3) | $C_{NRD}$ = 0 pF | $(n + 1)\ t_{CPMCK}$ - 1.8(4) | | ns |
| | | $C_{NRD}$ derating | -0.01 | | ns/pF |
| $EBI_{34}$ | NRD Minimum Pulse Width(2)(3) | $C_{NRD}$ = 0 pF | $n \times t_{CPMCK}$ + $(t_{CHMCK}$ - 1.2)(4) | | ns |
| | | $C_{NRD}$ derating | -0.01 | | ns/pF |

Notes:
1. Early Read Protocol.
2. Standard Read Protocol.
3. The derating should not be applied to $t_{CHMCK}$ or $t_{CPMCK}$.
4. n = number of standard wait states inserted.
5. Only one of these two timings needs to be met.

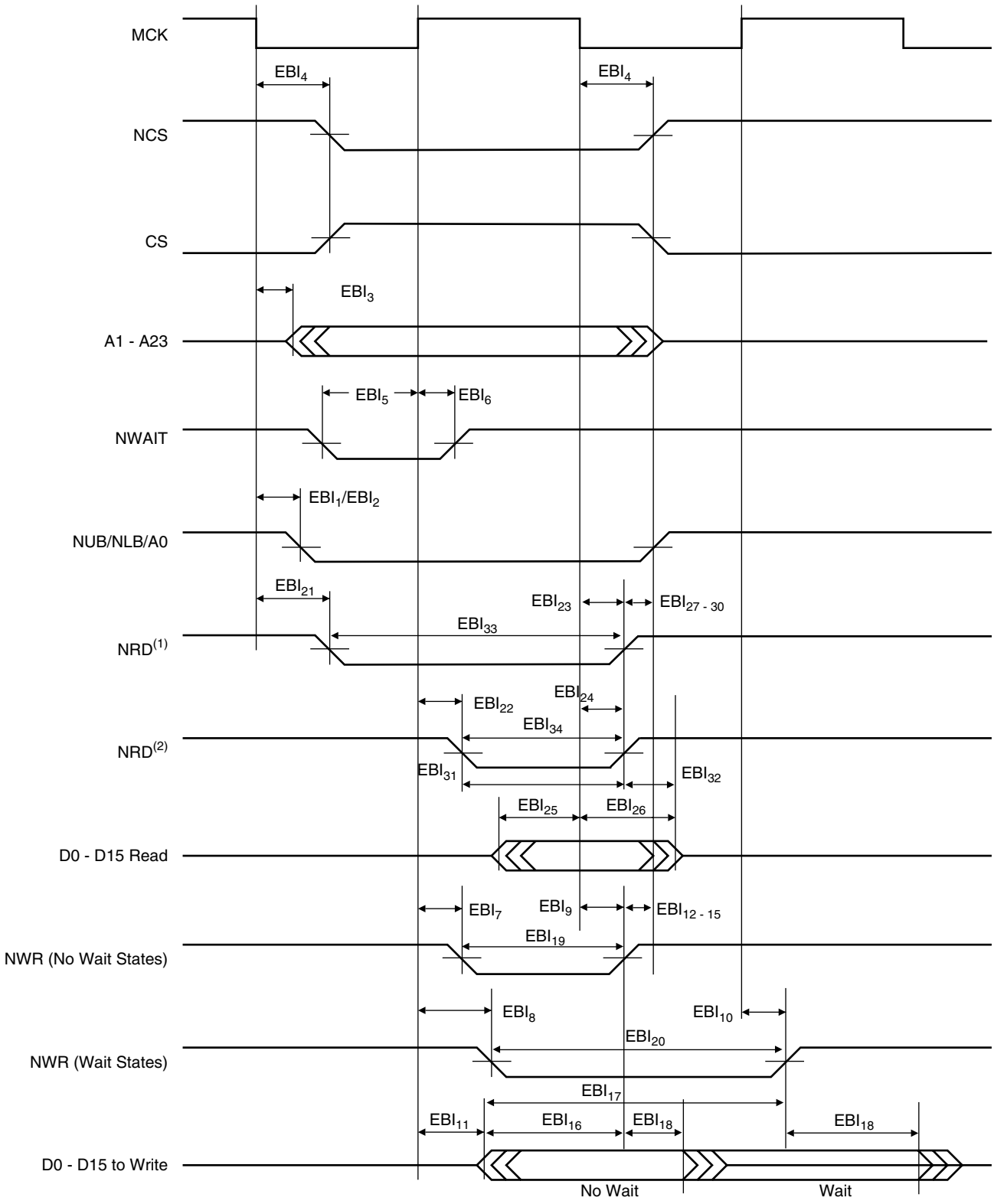
**Table 14.** EBI Read and Write Control Signals. Capacitance Limitation

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{CPLNRD}$ (1) | Master Clock Low Due to NRD Capacitance | $C_{NRD}$ = 0 pF | 13.8 | | ns |
| | | $C_{NRD}$ derating | 0.035 | | ns/pF |
| $T_{CPLNWR}$ (2) | Master CLock Low Due to NWR Capacitance | $C_{NWR}$ = 0 pF | 11.8 | | ns |
| | | $C_{NWR}$ derating | 0.035 | | ns/pF |

Notes: 1. If this condition is not met, the action depends on the read protocol intended for use.
- Early Read Protocol: Programing an additional $t_{DF}$ (Data Float Output Time) cycle.
- Standard Read Protocol: Programming an additional $t_{DF}$ Cycle and an additional wait state.

2. Applicable only for chip select programmed with 0 wait state. If this condition is not met, at least one wait state must be programmed.

**Figure 5.** EBI Signals Relative to MCK




Notes: 1. Early Read Protocol.
2. Standard Read Protocol.

## Peripheral Signals

### USART Signals

The inputs must meet the minimum pulse width and period constraints shown in Table 15 and Table 16, and represented in Figure 6.

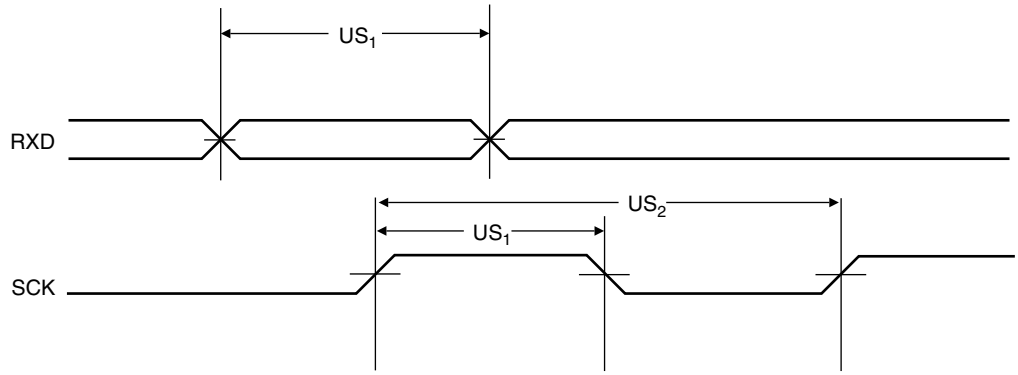
**Table 15.** USART Input Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $US_1$ | SCK/RXD Minimum Pulse Width | $5(t_{CPMCK}/2)$ | ns |

**Table 16.** USART Minimum Input Period

| Symbol | Parameter | Min Input Period | Units |
|---|---|---|---|
| $US_2$ | SCK Minimum Input Period | $9(t_{CPMCK}/2)$ | ns |

**Figure 6.** USART Signals



**SPI Signals**

The inputs must meet the minimum pulse width and period constraints shown in Table 17 and Table 18, and represented in Figure 7.

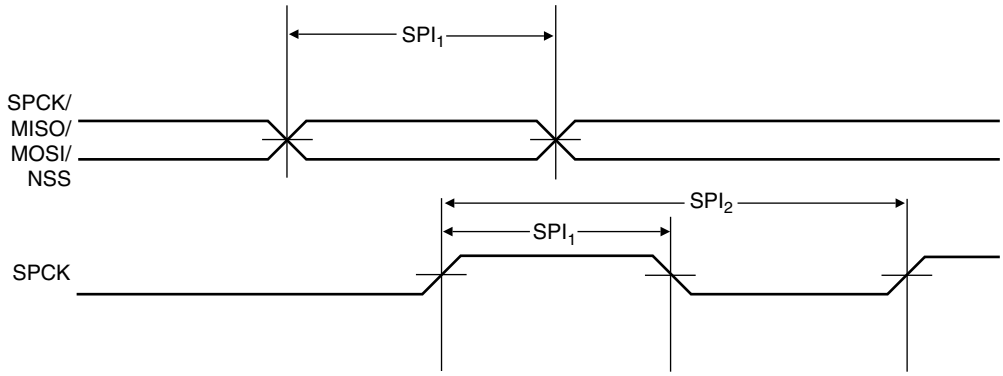
**Table 17.** SPI Input Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $SPI_1$ | SPK/MISO/MOSI/NSS Minimum Pulse Width | $3(t_{CPMCK}/2)$ | ns |

**Table 18.** SPI Minimum Input Period

| Symbol | Parameter | Min Input Period | Units |
|---|---|---|---|
| $SPI_2$ | SPCK Minimum Input Period | $5(t_{CPMCK}/2)$ | ns |

**Figure 7.** SPI Signals



**Timer/Counter Signals**

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CPMCK})$ in Waveform Event Detection mode and $4(t_{CPMCK})$ in Waveform Total-count Detection mode. The inputs must meet the minimum pulse width and minimum input period shown in Table 19 and Table 20, and as represented in Figure 8.

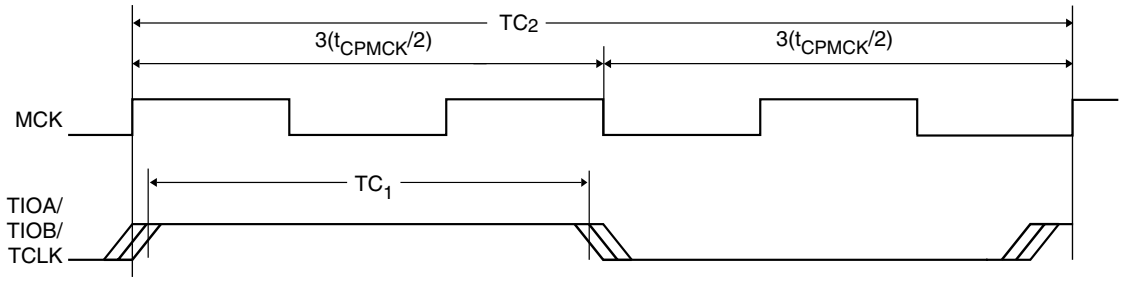
**Table 19.** Timer Input Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $TC_1$ | TCLK/TIOA/TIOB Minimum Pulse Width | $3(t_{CPMCK}/2)$ | ns |

**Table 20.** Timer Input Minimum Period

| Symbol | Parameter | Min Input Period | Units |
|---|---|---|---|
| $TC_2$ | TCLK/TIOA/TIOB Minimum Input Period | $5(t_{CPMCK}/2)$ | ns |

**Figure 8.** Timer Input



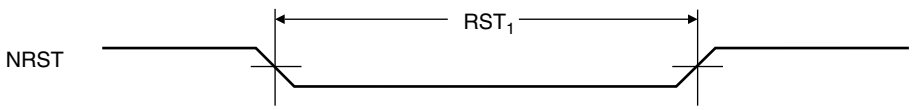

**Reset Signals**

A minimum pulse width is necessary, as shown in Table 21 and as represented in Figure 9.

**Table 21.** Reset Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $RST_1$ | NRST Minimum Pulse Width | 310 | µs |

**Figure 9.** Reset Signal




Only the NRST rising edge is synchronized with MCK. The falling edge is asynchronous.

### Advanced Interrupt Controller Signals

Inputs must meet the minimum pulse width and minimum input period shown in Table 22 and Table 23, and represented in Figure 10.

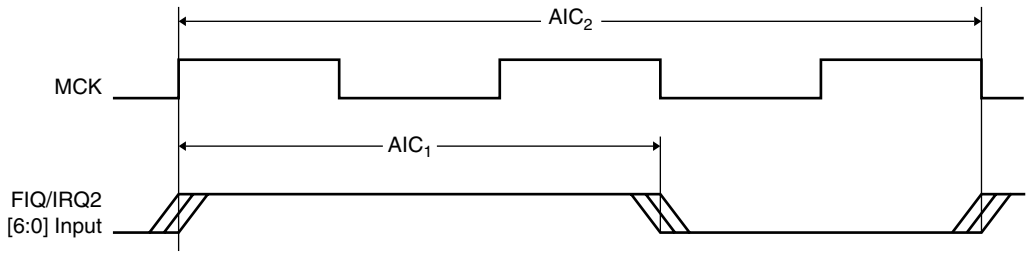
**Table 22.** AIC Input Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $AIC_1$ | FIQ/IRQ[6:0] Minimum Pulse Width | $3(t_{CPMCK}/2)$ | ns |

**Table 23.** AIC Input Minimum Period

| Symbol | Parameter | Min Input Period | Units |
|---|---|---|---|
| $AIC_2$ | AIC Minimum Input Period | $5(t_{CPMCK}/2)$ | ns |

**Figure 10.** AIC Signals



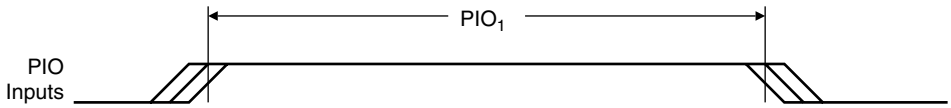

### Parallel I/O Signals

The inputs must meet the minimum pulse width shown in Table 24 and represented in Figure 11.

**Table 24.** PIO Input Minimum Pulse Width

| Symbol | Parameter | Min Pulse Width | Units |
|---|---|---|---|
| $PIO_1$ | PIO Input Minimum Pulse Width | $3(t_{CPMCK}/2)$ | ns |

**Figure 11.** PIO Signal

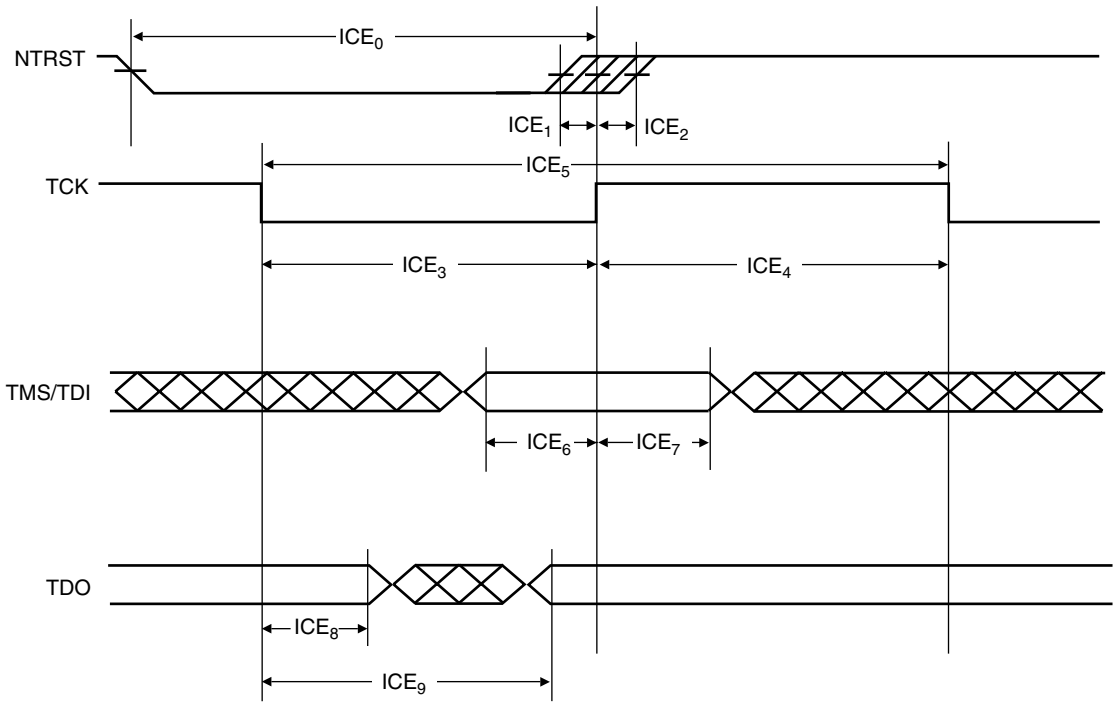


### ICE Interface Signals

**Table 25.** ICE Interface Timing Specifications

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $ICE_0$ | NTRST Minimum Pulse Width | | 19.2 | | ns |
| $ICE_1$ | NTRST High Recovery to TCK High | | 0.7 | | ns |
| $ICE_2$ | NTRST High Removal from TCK High | | 0.2 | | ns |
| $ICE_3$ | TCK Low Half-period | | 42.4 | | ns |
| $ICE_4$ | TCK High Half-period | | 40.1 | | ns |
| $ICE_5$ | TCK Period | | 82.5 | | ns |
| $ICE_6$ | TDI, TMS Setup before TCK High | | 1.0 | | ns |
| $ICE_7$ | TDI, TMS Hold after TCK High | | 0.8 | | ns |
| $ICE_8$ | TDO Hold Time | $C_{TDO}$ = 0 pF | 7.2 | | ns |
| | | $C_{TDO}$ derating | 0 | | ns/pF |
| $ICE_9$ | TCK Low to TDO Valid | $C_{TDO}$ = 0 pF | | 15.1 | ns |
| | | $C_{TDO}$ derating | | 0.042 | ns/pF |

**Figure 12.** ICE Interface Signal

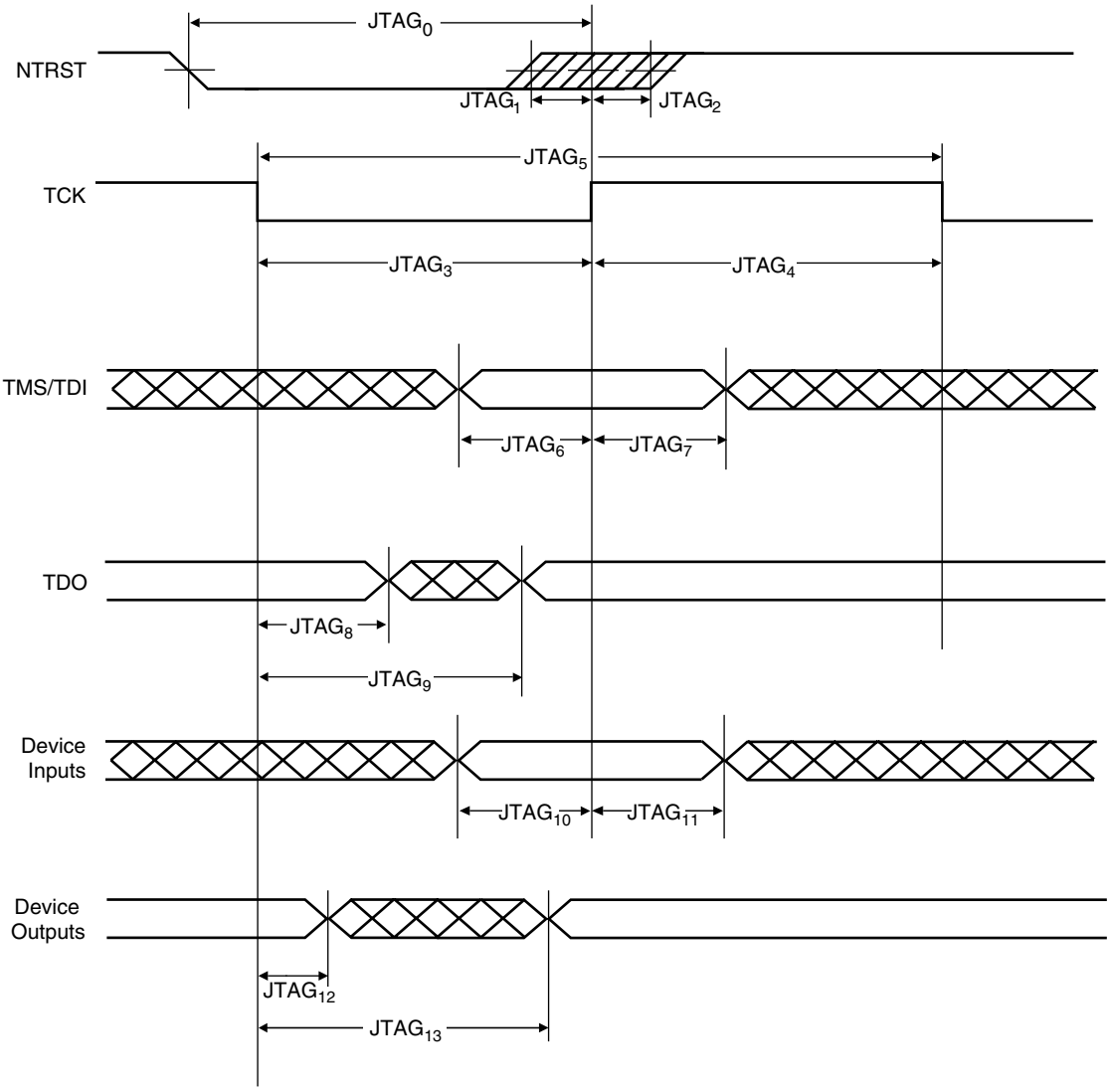


### JTAG Interface Signals

**Table 26.** JTAG Interface Timing Specifications

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $JTAG_0$ | NTRST Minimum Pulse Width | | 19.2 | | ns |
| $JTAG_1$ | NTRST High Recovery to TCK Toggle | | 0.8 | | ns |
| $JTAG_2$ | NTRST High Removal from TCK Toggle | | 1.6 | | ns |
| $JTAG_3$ | TCK Low Half-period | | 2.5 | | ns |
| $JTAG_4$ | TCK High Half-period | | 3.1 | | ns |
| $JTAG_5$ | TCK Period | | 5.6 | | ns |
| $JTAG_6$ | TDI, TMS Setup before TCK High | | 1.7 | | ns |
| $JTAG_7$ | TDI, TMS Hold after TCK High | | 2.5 | | ns |
| $JTAG_8$ | TDO Hold Time | $C_{TDO}$ = 0 pF | 3.3 | | ns |
| | | $C_{TDO}$ derating | 0 | | ns/pF |
| $JTAG_9$ | TCK Low to TDO Valid | $C_{TDO}$ = 0 pF | | 7.2 | ns |
| | | $C_{TDO}$ derating | | 0.042 | ns/pF |
| $JTAG_{10}$ | Device Inputs Setup Time | | -1.0 | | ns |
| $JTAG_{11}$ | Device Inputs Hold Time | | 3.0 | | ns |
| $JTAG_{12}$ | Device Outputs Hold Time | $C_{OUT}$ = 0 pF | 4.7 | | ns |
| | | $C_{OUT}$ derating | 0 | | ns/pF |
| $JTAG_{13}$ | TCK to Device Outputs Valid | $C_{OUT}$ = 0 pF | | 11.9 | ns |
| | | $C_{OUT}$ derating | | 0.037 | ns/pF |

**Figure 13.** JTAG Interface Signal



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