5.15–5.85GHz 802.11ac Front End Module

Description

The LX5586H is a complete integrated 5GHz Front-End Module (FEM) for an IEEE 802.11ac system. It includes a highly linear 5GHz Power Amplifier (PA) with power detector, Low Noise Amplifier (LNA) with bypass capability, and SPDT antenna switch. This highly integrated FEM only requires one bypass cap thus reducing system footprint, bill of materials, and manufacturing cost.

The LX5586H is available in a 16-pin low profile 2.5x2.5x0.45mm QFN Package.

Features

- 5V Supply Voltage
- Integrated 5GHz PA, LNA, and SPDT Tx/Rx Switch
- POUT = 19dBm (typical) at -36dB EVM (256QAM/80MHz)
- Bypassable Low Noise Figure LNA
- Small Footprint: 2.5 x 2.5mm²
- Low Profile: 0.45mm max
- RoHS Compliant & Halogen Free

Applications

- Tablets
- Access Points
- Mobile Devices
- Notebooks
- Gaming

Block Diagram

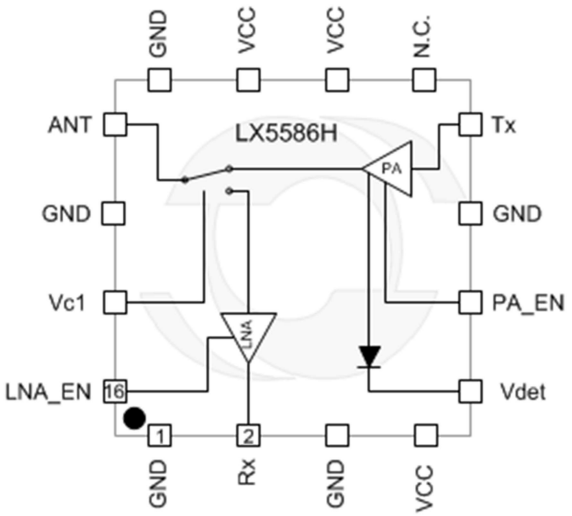


Figure 1 · Functional Block Diagram

Pin Configuration

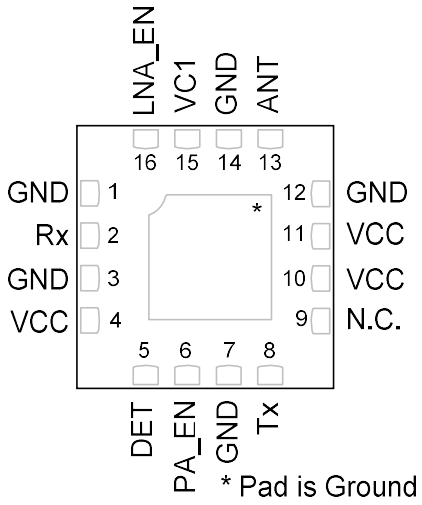


Figure 2 · Pinout (Top View)

Ordering Information

Ambient Temperature	Type	Package	Ordering Part Number	Packaging Type
-40°C to 85°C	RoHS2 compliant, Pb-free NiPdAu lead finish	QFN 2.5x2.5x0.45 16L	LX5586HLL-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	GND	Ground
2	Rx	DC blocked 50ohm output of bypassable LNA.
3	GND	Ground
4	VCC	5V nominal supply voltage
5	DET	Output of transmit power detector
6	PA_EN	Power amplifier control pin
7	GND	Ground

Pin Number	Pin Designator	Description
8	Tx	50 ohm input to PA. No DC voltage is generated by the FEM on this line. No external DC voltage should be applied to this pin as it present a DC short to GND.
9	Spare	No connect.
10	VCC	5V nominal supply voltage.
11	VCC	5V nominal supply voltage.
12	GND	Ground
13	ANT	DC blocked 50 ohm antenna port.
14	GND	Ground
15	VC1	Rx bypass mode control line.
16	LNA_EN	LNA control line.

Absolute Maximum Ratings

Parameter	Value	Units
DC Supply Voltage (VCC)	6	V
Control Inputs (LNA_EN, PA_EN, VC1)	3.6	V
Total Power Dissipation	1.5	W
RF Input power at ANT Port	10	dBm
Input Power at TXA Port	5	dBm
Maximum Junction Temperature (T_{JMAX})	+150	°C
Operational Ambient Temperature	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure)	260	°C

Note: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The LX5586H typical ESD threshold level is >1000 VDC using Human Body Model (HBM) testing for all pins.

Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Absolute maximum DC supply and control voltage is specified as 6V applied for 10 seconds over the entire lifetime of the part. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JP} Junction to Pad	18.3	°C/W
θ_{JA} Junction to Ambient	54.3	

Note: Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using TJ = TA + (PD x θ_{JA}). In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

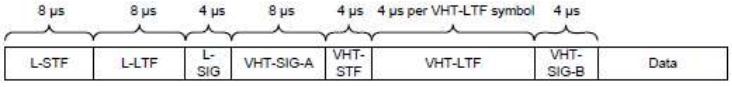
Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.53GHz, T_A = 25°C, VCC =5V. Min and max are across frequency, supply, and temperature.						
Operating Supply Current						
VCC	Supply Voltage VCC		4.75	5	5.25	V
I_{SLEEP}	Sleep Mode Current	PA_EN = LNA_EN = VC1= 0V, or floating.		1	100	µA
General Characteristics						
F_{RFhi}	High Band Frequency Range		5.15	5.53	5.85	GHz
CHBW	Channel Bandwidth	80MHz	20		80	MHz
V_{IH}	Control Logic Levels		3	3.3	3.6	V
V_{IL}			0		0.4	V
Ictrl	Maximum Control Current	3.3V logic level		5	6	mA
Δt_{onPA} Δt_{offPA}	Rx→Tx Switching Time	Difference between falling edge of LNA_EN and time when Tx output has settled to within 90% of its final power.		250	400	ns
Δt_{rxlvl}	Rx Gain Switching Time	Difference between edge of LNA_EN and time when Rx output has settled to within 90% of its final power.		50	100	ns
Δt_{onLNA}, Δt_{offLNA}	Tx→Rx Switching Time	Difference between edge of PA_EN and time when Rx output has settled to within 90% of its final power.		250	400	ns
ESD	ESD Susceptibility, ANT port		1000			V
	ESD Susceptibility, Other ports		1000			V

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.53GHz, T_A = 25°C, VCC = 5V. Min and max are across frequency, supply, and temperature.						
Detector Characteristics						
PDBW	Power Detector 3dB Bandwidth	RF two-tone spacing for which the PD output voltage swing is reduced to 0.707 of maximum with P_{OUT} = 16dBm.	1.5		2.5	MHz
PD_{SENS}	Power Detector Sensitivity	Sensitivity between 11dBm and 22dBm output power.	10		130	mV/dB
PD_{FREQ}	Power Detector Variation Over Frequency	$Vdet_{RMS}$ variation over 5.15 to 5.35. Variation is defined as (Max-Min).			1	dB
		$Vdet_{RMS}$ variation over 5.47 to 5.725. Variation is defined as (Max-Min).			1	
		$Vdet_{RMS}$ variation over 5.725 to 5.85. Variation is defined as (Max-Min)			1	
PD_{VFT}	Power Detector Maximum Output Voltage Limits	At any particular detector voltage, the measured $Vdet_{RMS}$ power variation over V, F and T must fall within this limit.			3	dB
PD_{BW}	Power Detector Variation Over Channel Bandwidth	At any particular detector voltage for output power from 11-22 dBm, the measured $Vdet_{RMS}$ power variation as the channel bandwidth is varied over 20/40/80MHz must fall within the limits shown.			0.5	dB
V_{DET}	Power Detector Voltage[1]	No RF	175	200	300	mV
		$Vdet_{RMS}$ at P_{OUT} = 22dBm measured in first 16µs of preamble	600	750	850	
Z_{DET}	Detector Output Impedance				5	kΩ
PD_{VSWR}	Power detector variation over 3:1 VSWR	To be met for forward power. Measured from 0° to 360° in 15° increments.		+/-1		dB

Detector voltage is to be measured during the first 16us of the preamble, using the L-STF and L-LTF fields as shown below.



Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.53GHz, T_A = 25°C, VCC = 5V. Min and max are across frequency, supply, and temperature.						
High Band Tx Characteristics						
S_{11}	Input Return Loss	TxA port with PA enabled	8	12		dB
S_{22}	Output Return Loss	ANT port with PA enabled	7	10		dB
S_{21}	Power Gain	Small signal gain in operating frequency band.	24	28	33	dB
ΔS_{21}	Power Gain Variation	Over single 80MHz-channel		0.2	1	dB
		5150 to 5700 MHz		0.2	2	
		5700 to 5850 MHz		1.3	3	
S_{21}	Gain Limit at Ref-vco freq	3433-3917 MHz			24	dB
S_{21}	Gain Limit at Ref-vco ÷ 2 Spur Frequency	1716-1959 MHz			20	dB
Dynamic EVM	DEVM	20 dBm, MCS7, 11a, 20MHz, 50% duty cycle, with 8and 76 symbols. EVM is to be measured at 5.18, 5.5, and 5.825GHz.		-33		dB
		19 dBm, MCS7, 11ac, 80MHz, 50% duty cycle, with 8, 50, and 1000 symbols. EVM is to be measured at 5.21, 5.53, and 5.775GHz.		-36		
		18 dBm MCS9, 11ac, 80MHz, 50% duty cycle, with 8, 50, and 1000 symbols. EVM is to be measured at 5.21, 5.53, and 5.775GHz at 5V, 25C		-37	-34	
		18 dBm MCS9, 11ac, 80MHz, 50% duty cycle, with 8, 50, and 1000 symbols. EVM is to be measured at 5.21, 5.53, and 5.775GHz over all voltage and temperature ranges		-37	-33	
Dynamic EVM floor	DEVMfloor	DEVM floor for 10-90% duty cycle, with 8, 50, 1000 symbols, from 7-17 dBm output power		-38		
$Mask_{11ac}$	802.11ac Mask	Mask compliance with, MCS0, 20MHz, RBW=100kHz, VBW= 30kHz, 100% duty cycle. Measured at 5.18GHz and 5.825GHz.		20		dBm
HD2, HD3	2^{nd} , 3^{rd} Harmonic PSD	P_{OUT} = 20dBm, 6Mbps, 20MHz BW		-35		dBm/MHz
Icc	Operating Current	P_{OUT} = 17 dBm		180		mA
		P_{OUT} = 18 dBm		195	230	
		P_{OUT} = 19 dBm		210	250	
		P_{OUT} = 20 dBm		230		
I_q	Quiescent Current	No RF input. PA enabled, V_{CC} = 5V		110	150	mA

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.53GHz, T_A = 25°C, VCC =5V. Min and max are across frequency, supply, and temperature.						
Rx Characteristics						
S_{11}	Input Return Loss	At ANT port for HG and bypass Rx states	10	14		dB
S_{22}	Output Return Loss	At RxA port for all Rx gain states	10	20		dB
S_{21}	Power Gain	LNA enabled	10	12.5	15	dB
		LNA bypass state (bypass)	-9	-7	-6	
ΔS_{21}	Power Gain Variation	Over single 80MHz-channel			1	dB
		Over entire F_{RFlo}			2	
Noise Figure	NF	LNA enabled, 25°C		2.7		dB
		LNA bypass state, 25°C		8		
IIP3	Input Third Order Intercept Point	At ANT port with LNA enabled. To be measured with total input power = -10dBm (-13 dBm/tone).	4	6.5		dBm
		At ANT port with LNA enabled and input tones at 2.412 and 2.437GHz. Total input power is 0 dBm (-3 dBm/tone).		10		
		At ANT port with LNA bypassed. Measured with total input power = 5 dBm (2dBm/tone).	18	26.5		
L_{loop}	ANT→RxA Loopback Isolation	PA enabled (T/R switch in Tx) and LNA bypassed (Loopback)	28	30	45	dB
I_q	Quiescent Current	LNA enabled, (No RF)		7		mA
		LNA in bypass mode, (No RF)		3.5	100	µA

Functional State Table

Vc1	LNA_EN[1]	PA_EN[2]	Default State
1	1	0	Rx High Gain
1	0	0	Rx Bypass State
0	0	1	Tx
0	0	0	Sleep Mode[3]

[1] LNA is on while LNA_EN is high and LNA is off and in bypass mode when LNA_EN is low and VC1 is high.

[2] PA_EN controls PA enable and T/R switch logic.

[3] The FEM will be placed into sleep mode when all control signals are logic 0 or if they are all floating.

Part Markings

•	Pin 1 identifier
MSC	Company name
586H	Part number
YNNN	Trace code

Figure 3 · Typical Part Markings

Characteristic Curves: Tx S-parameters

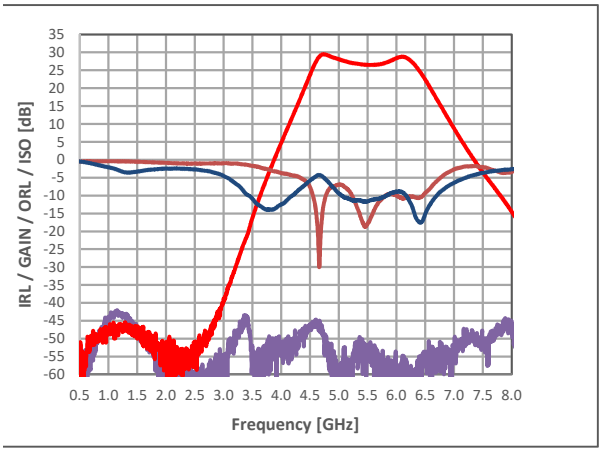


Figure 4 · Tx S-Parameters (VCC= 5V; 25°C)

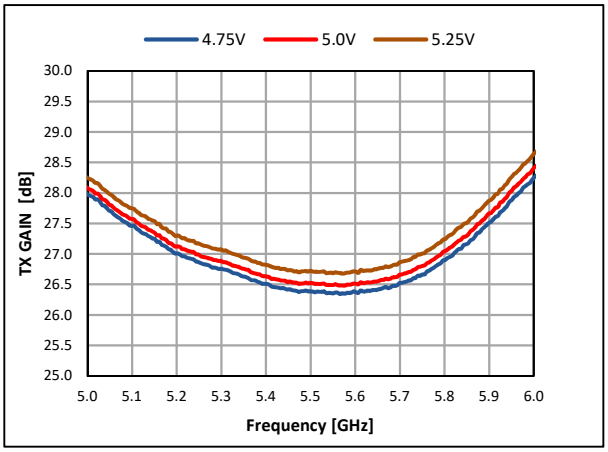


Figure 5 · Tx gain at 25°C

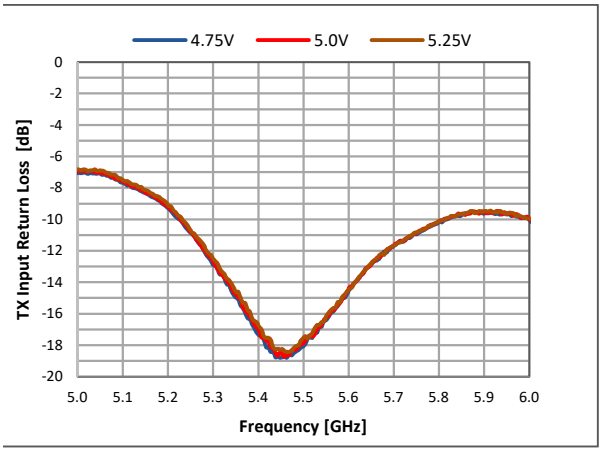


Figure 6 · Tx input return loss at 25°C

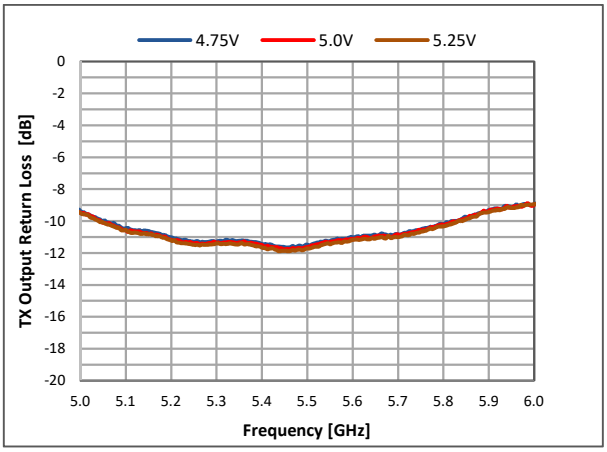


Figure 7 · Tx output return loss at 25°C

Characteristic Curves: Tx Linearity: 80MHz BW

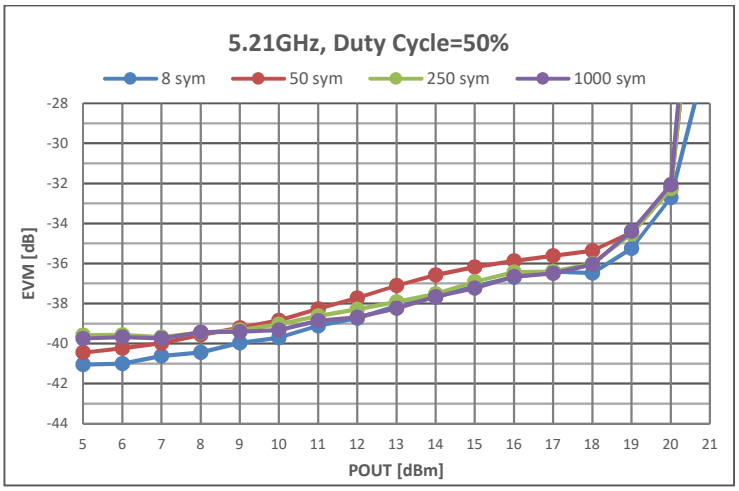


Figure 8 · Dynamic EVM (802.11ac, VHT-80, MCS 9, VCC=5V)

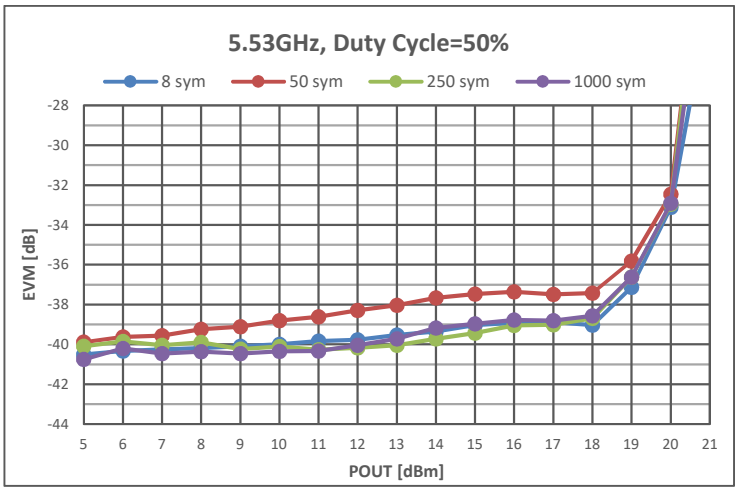


Figure 9 · Dynamic EVM (802.11ac, VHT-80, MCS 9, VCC=5V)

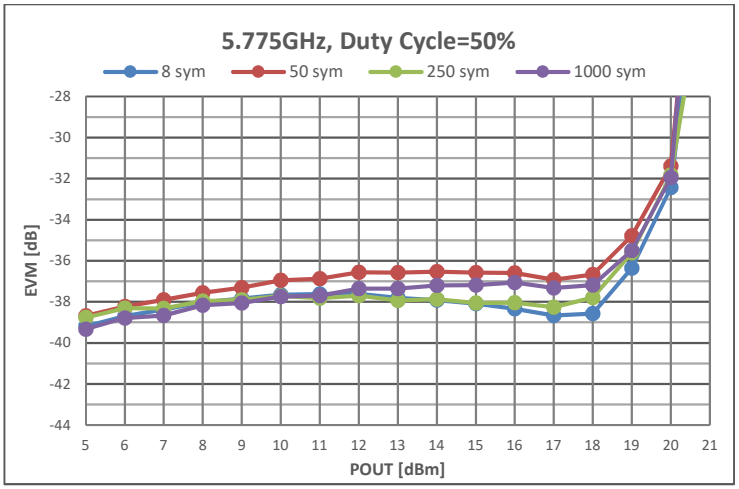


Figure 10 · Dynamic EVM (802.11ac, VHT-80, MCS 9, VCC=5V)

Characteristic Curves: Rx High Gain S-parameters

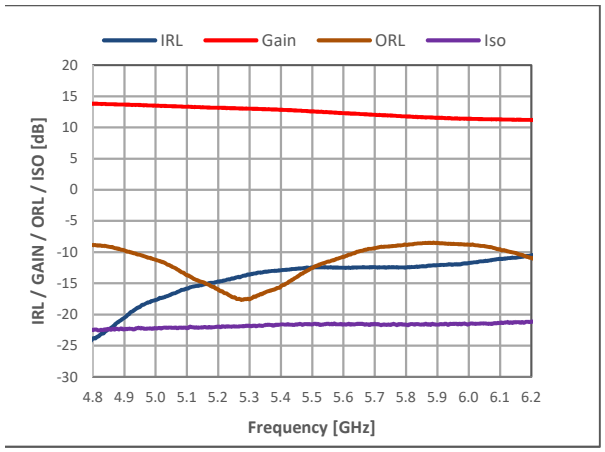


Figure 10 · Rx HG S-Parameters (VCC = 5V, 25°C)

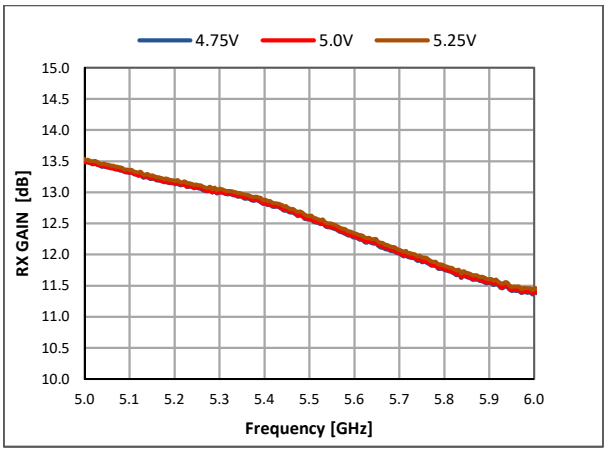


Figure 11 · Rx HG gain at 25°C

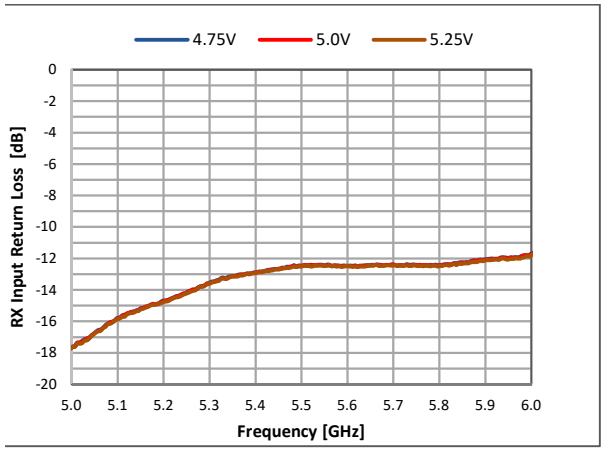


Figure 12 · Rx HG input return loss at 25°C

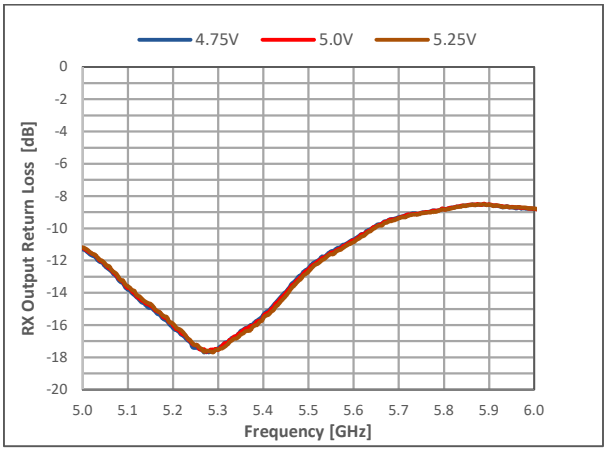


Figure 13 · Rx HG output return loss at 25°C

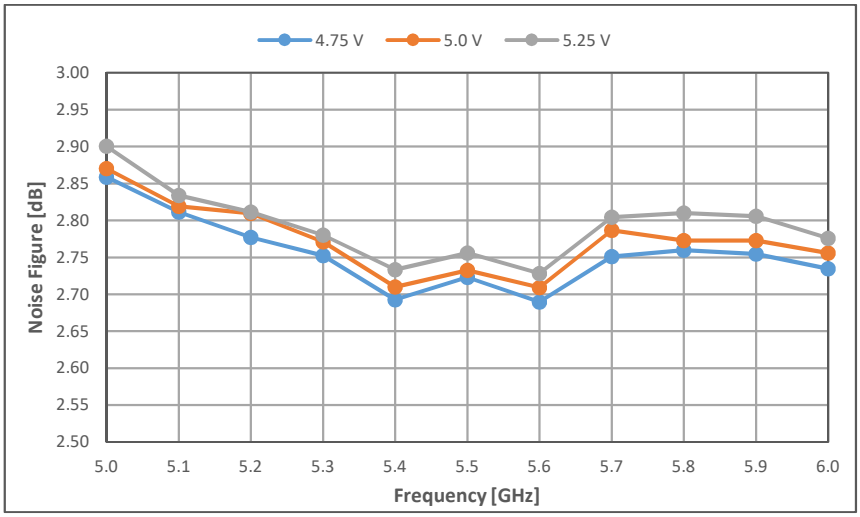


Figure 14 · LX5586H Noise Figure

Characteristic Curves: Rx Bypass Mode S-parameters

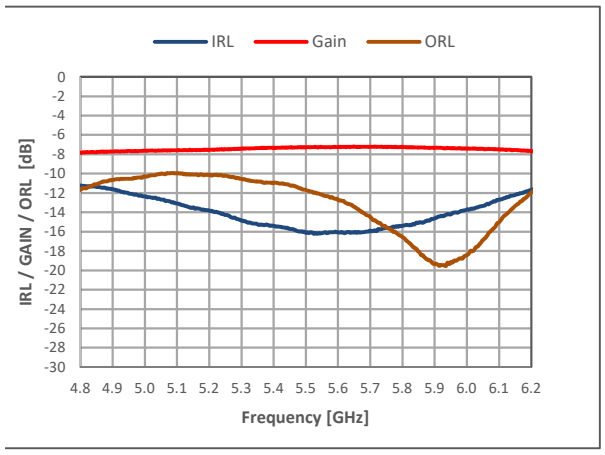


Figure 15 · Rx BP S-parameters (VCC = 5V, 25°C)

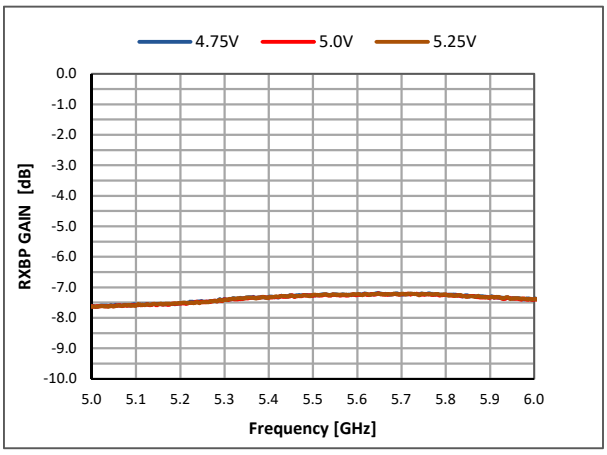


Figure 16 · Rx BP gain at 25°C

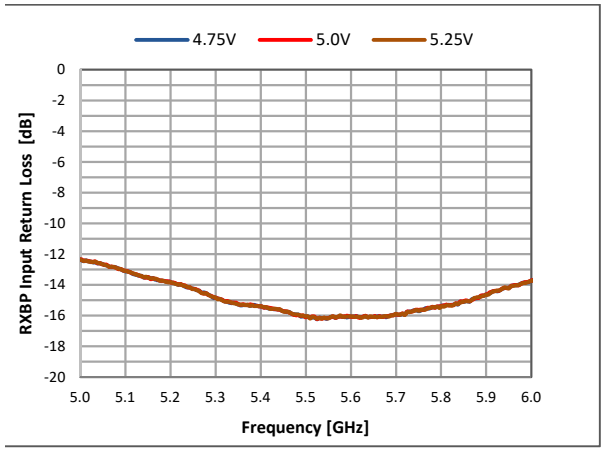


Figure 17 · Rx BP input return loss at 25°C

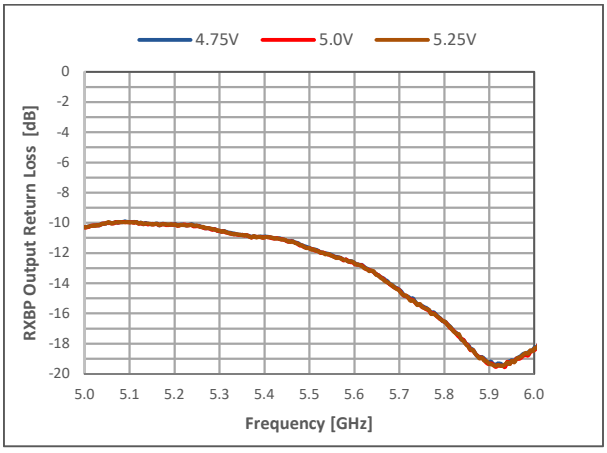
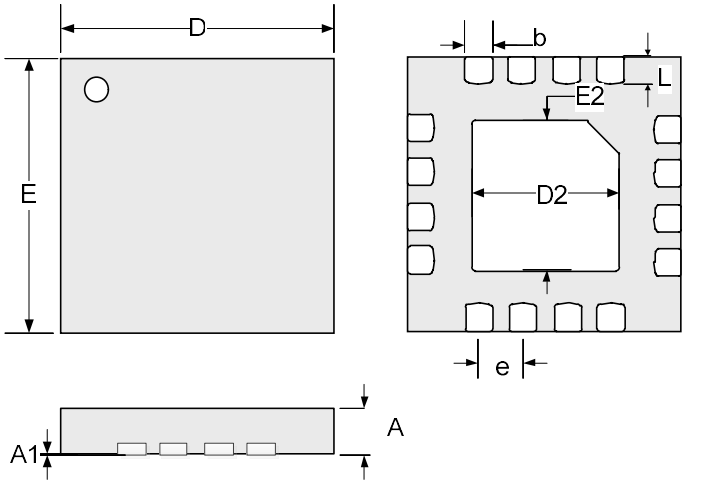


Figure 18 · Rx BP output return loss at 25°C

Package Outline Dimensions

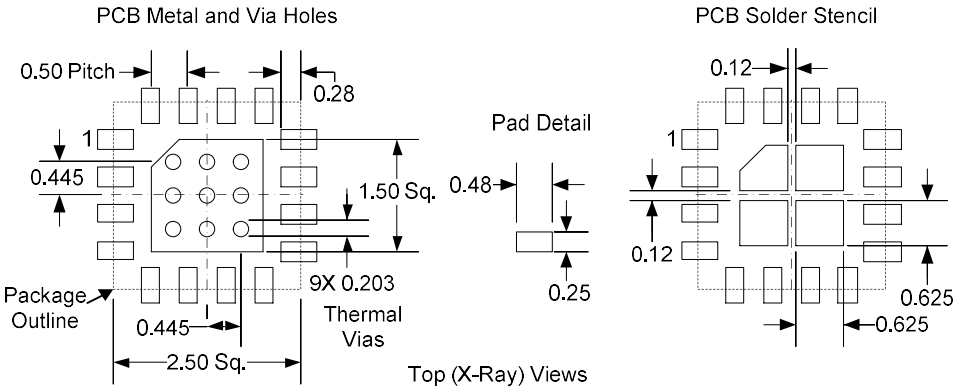
The package is halogen free and meets RoHS2 and REACH standards.

(MSL1, 260°C per JEDEC J-STD-020)



DIMENSION	MILLIMETERS	
	MIN	MAX
A		0.45
A1	0.01	0.05
L	0.20	0.30
b	0.20	0.30
D	2.45	2.55
D2	1.30	1.40
E	2.45	2.55
E2	1.30	1.40
e	0.50 BSC	

Figure 19 · 16 Pin QFN Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Unless specified dimensions are symmetrical about center lines.
3. OSP or NiAu planar surface finish recommended.
4. Non-Solder Mask Defined (NSMD) pads recommended for terminal pads.
5. Recommended tented thermal vias as shown with vias filled with solder.
6. Stencil thickness < 0.15mm.
7. Aperture design for thermal pads using multiple openings with 60 to 80% solder paste coverage.

Figure 20 · PCB Layout Footprint (Top View)

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