5.15–5.85GHz 802.11ac Front End Module

Description

The LX5586 is a complete integrated 5GHz Front-End Module (FEM) for an IEEE 802.11ac system. It includes a highly linear 5GHz Power Amplifier (PA) with power detector, Low Noise Amplifier (LNA) with bypass capability, and SPDT antenna switch. This highly integrated FEM only requires one bypass cap thus reducing system footprint, bill of materials, and manufacturing cost.

The LX5586 is available in a 16-pin low profile 2.5x2.5x0.4mm QFN Package.

Features

- Single Supply Voltage 3V to 4.6V
- Integrated 5GHz PA, LNA, and SPDT Tx/Rx Switch
- POUT = 17dBm (typical) at -35dB EVM (256QAM/80MHz)
- Bypassable low noise figure LNA
- Small Footprint: 2.5 x 2.5mm²
- Low Profile: 0.4mm max
- RoHS Compliant & Halogen Free

Applications

- Smartphones
- Tablets
- Access Points
- Mobile Devices
- Notebooks
- Gaming

Block Diagram

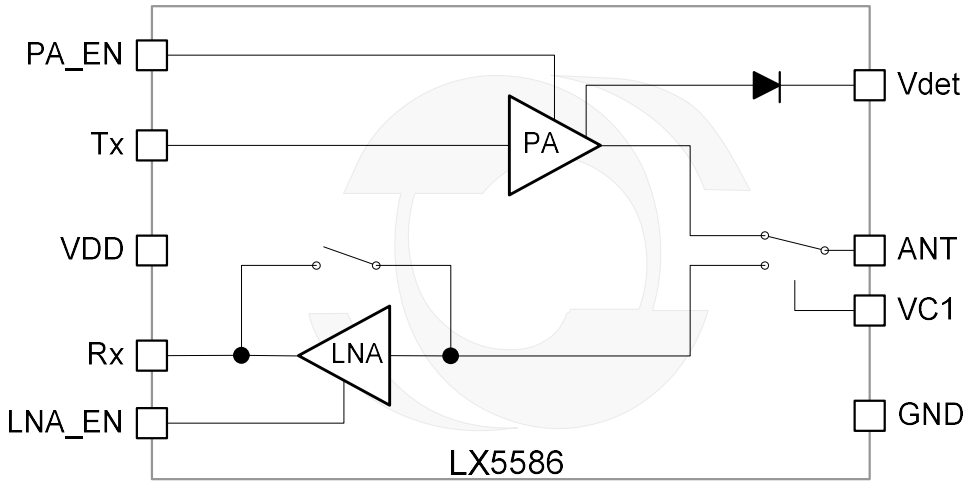


Figure 1 · Functional Block Diagram

Pin Configuration

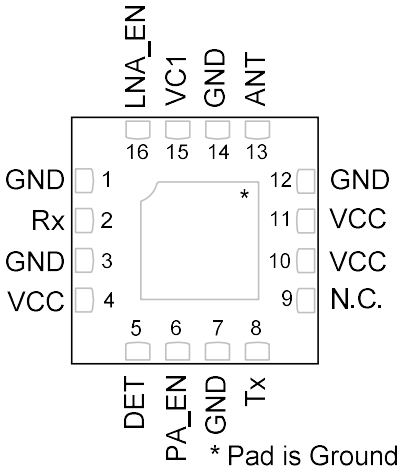


Figure 2 · Pinout (Top View)

Ordering Information

Ambient Temperature	Type	Package	Ordering Part Number	Packaging Type
-40°C to 85°C	RoHS2 compliant, Pb-free NiPdAu lead finish	QFN 2.5x2.5x0.4 16L	LX5586LL -TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	GND	Ground
2	Rx	DC blocked, 50ohm output of bypassable LNA.
3	GND	Ground
4	VCC	3.6V nominal supply voltage
5	DET	Output of transmit power detector
6	PA_EN	Power amplifier control pin
7	GND	Ground
8	Tx	50 ohm input to PA. No DC voltage is generated by the FEM on this line. No external DC voltage should be applied on this pin, as it presents a shunt inductor to ground.
9	Spare	No connect
10	VCC	3.6V nominal supply voltage
11	VCC	3.6V nominal supply voltage

Pin Number	Pin Designator	Description
12	GND	Ground
13	ANT	DC blocked, 50 ohm antenna port.
14	GND	Ground
15	VC1	Rx bypass mode control line
16	LNA_EN	LNA control line

Absolute Maximum Ratings

Parameter	Value	Units
DC Supply Voltage (VCC)	6	V
Control Inputs (LNA_EN, PA_EN, VC1)	6	V
Total Power Dissipation	1.5	W
RF Input power at ANT Port	10	dBm
Input Power at TXA Port	5	dBm
Maximum Junction Temperature (T_{JMAX})	+150	°C
Operational Ambient Temperature	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure)	260	°C

Note: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The LX5586 ESD threshold level is >1000V using Human Body Model (HBM) testing for all RF lines. The ESD threshold also exceeds 500V (CDM) on all pins.

Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Absolute maximum DC supply and control voltage is specified as 6V applied for 10 seconds over the entire lifetime of the part. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JP} Junction to Pad	18.3	°C/W
θ_{JA} Junction to Ambient	54.3	

Note: Note: The θJx numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta J_A)$. In particular, θJ_A is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC) with 9 thermal vias.

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.5GHz, T_A = 25°C, VCC = 3.6V. Min and max are across frequency, supply, and temperature.						
General Characteristics						
VCC	Supply Voltage VCC	Note: Part is fully functional from 3.0 to 4.6V. Gain and linearity will be degraded below 3.2V.	3.2	3.6	4.6	V
I_{SLEEP}	Sleep Mode Current	PA_EN = LNA_EN = VC1= 0V, or floating.		0.2	100	µA
F_{RFhi}	High Band Frequency Range	Note: Part is fully functional from 4.9 to 5.15GHz, but gain and linearity will be affected. Operation from 4.9 to 5.15GHz is best effort only.	5.15	5.53	5.85	GHz
CHBW	Channel Bandwidth	80MHz	20	80	80	MHz
V_{IH}	Control Logic Levels		3	3.3	3.6	V
V_{IL}			0		0.4	V
Ictrl	Maximum Control Current	3V logic level		5	6	mA
Δt_{onPA} Δt_{offPA}	Rx→Tx Switching Time	Difference between falling edge of LNA_EN and time when Tx output has settled to within 90% of its final power.		250		ns
Δt_{rxlvl}	Rx Gain Switching Time	Difference between edge of LNA_EN and time when Rx output has settled to within 90% of its final power.		100		ns
Δt_{onLNA}, Δt_{offLNA}	Tx→Rx Switching Time	Difference between edge of PA_EN and time when Rx output has settled to within 90% of its final power.		325		ns

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.5GHz, T_A = 25°C, VCC = 3.6V. Min and max are across frequency, supply, and temperature.						
Power Detector						
PDBW	Power Detector 3dB Bandwidth	RF two-tone spacing for which the PD output voltage swing is reduced to 0.707 of maximum.	2			MHz
PD_{SENS}	Power Detector Sensitivity	Sensitivity between 10dBM and 20dBm output power.	10		100	mV/dB
PD_{FREQ}	Power Detector Variation over Frequency	Variation over 5.15 to 5.35. Variation is defined as (Max-Min).			1	dB
		Variation over 5.47 to 5.725. Variation is defined as (Max-Min).			1	
		Variation over 5.725 to 5.825. Variation is defined as (Max-Min)			1.2	
VPD_{LIMITS}	Power Detector Maximum Output Voltage Limits	Spec driven by input voltage range of the ADC monitoring the detector output.	0		1.2	V
V_{DET}	Power Detector Voltage	No RF	170	225	290	mV
		P_{OUT} =20 dBm CW	800	950	1050	
Z_{DET}	Detector Output Impedance				3	kΩ
PD_{err}	Power Detector Error	Maximum delta in Tx output power measured between 3:1 VSWR load (all phases) and 50Ω at the ANT port.		+/-0.7		dB

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Tx Characteristics over 3.2-4.6V Supply Range						
S_{11}	Input Return Loss	TxA port with PA enabled	10	12		dB
S_{11}	Output Return Loss	ANT port with PA enabled	7	10		dB
S_{21}	Power Gain	Small signal gain in operating frequency band.	23	27	33	dB
ΔS_{21}	Power Gain Variation	Over single 80MHz-channel		0.2	1	dB
		5150 to 5700 MHz		0.2	2	
		5700 to 5875 MHz		1.3	3	
S_{21}	Gain Limit at Ref-vco freq	3433-3917 MHz			24	dB
S_{21}	Gain Limit at Ref-vco ÷ 2 Spur Frequency	1716-1959 MHz			20	dB
S_{12}	Reverse Isolation	Over F_{RFlo}	39			dB
DEVM[1]	Linear Power	256QAM, 80MHz, DEVM<-34dB, at 5.21, 5.53, 5.775GHz	14	17		dBm
		64QAM, 20MHz, DEVM<-30dB at 5.18<f<5.825GHz	15	18		
DEVM	Low Power EVM floor	256QAM, 80MHz, 5-14 dBm		-38		dBm
$Mask_{11ac}$	802.11ac Mask	P_{OUT} = 19dBm, BPSK, RBW = 100kHz, VBW = 30kHz, 10% duty cycle.	Meets 802.11ac mask (-20 dBr at 41MHz offset, -28 dBr at 80 MHz offset, -40 dBr at 120 MHz offset)			
OOB20	OOB Emissions	P_{OUT} with 20MHz channel BW meeting -50 dBm/MHz. Emissions measured at 4.5 to 5.15GHz (operating frequency set to 5.18GHz) and 5.35 to 5.46GHz (operating frequency of 5.32 and 5.5GHz). Best effort only.		14		dBm
OOB40		P_{OUT} with 40 MHz channel BW meeting -50 dBm/MHz. Emissions measured at 4.5 to 5.15GHz (operating frequency set to 5.18GHz) and 5.35 to 5.46GHz (operating frequency of 5.3 and 5.5GHz). Best effort only.		14		
OOB80		P_{OUT} with 80 MHz channel BW meeting -50 dBm/MHz Emissions measured at 4.5 to 5.15GHz (operating frequency set to 5.21GHz) and 5.35 to 5.46GHz (operating frequency of 5.29 and 5.53GHz). Best effort only.		14		
HD2, HD3	2^{nd} , 3^{rd} Harmonic PSD	P_{OUT} = 20dBm, 6Mbps, 20MHz BW		-27	-22	dBm/MHz

Electrical Characteristics

I_{CC}	I_{CC}	P_{OUT} = 14 dBm		165	195	mA
		P_{OUT} = 15 dBm		175		
		P_{OUT} = 16 dBm		185	220	
		P_{OUT} = 17 dBm		200		
Quiescent Current	I_q	No RF input. PA enabled, V_{CC} = 3.3V		125		mA
[1]DEVM (dynamic EVM) is measured with 10% or 50% duty cycle and with burst durations from 60µs to 1ms.						

Typical Tx Characteristics at 3.3V						
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Units**
DEVM	Linear Power	256QAM, 80MHz, DEVM<-34dB, at 5.21, 5.53, 5.775GHz		16.5		dBm
		64QAM, 20MHz, DEVM<-30dB at 5.18<f<5.825GHz		17.5		
$Mask_{11ac}$	802.11ac Mask	P_{OUT} = 18.5dBm, BPSK, RBW = 100kHz, VBW = 30kHz, 10% duty cycle.	Meets 802.11ac mask (-20 dBr at 41MHz offset, -28 dBr at 80 MHz offset, -40 dBr at 120 MHz offset)			
HD2, HD3	2^{nd} , 3^{rd} Harmonic PSD	P_{OUT} = 20dBm, 6Mbps, 20MHz BW		-27		dBm/MHz
I_{CC3V}	I_{CC}	P_{OUT} = 14 dBm		165		mA
		P_{OUT} = 15 dBm		175		
		P_{OUT} = 16 dBm		185		
		P_{OUT} = 17 dBm		200		
Quiescent Current	I_q	No RF input. PA enabled, V_{CC} = 3.3V		125		mA

Electrical Characteristics

Rx Characteristics over 3.2-4.6V Supply Range						
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Units**
Unless otherwise noted: Typical conditions are at 5.5GHz, T_A = 25°C, VCC =3.6V. Min and max are across frequency, supply, and temperature.						
S_{11}	Input Return Loss	At ANT port for HG and bypass Rx states	10	14		dB
S_{22}	Output Return Loss	At RxA port for all Rx gain states	10	20		dB
S_{21}	Power Gain	LNA enabled	10	12.5	15	dB
		LNA bypass state (bypass)	-9	-7	-6	
ΔS_{21}	Power Gain Variation	Over single 80MHz-channel			0.5	dB
		Over entire F_{RFlo}			2	
Noise Figure	NF	LNA enabled, 25°C		2.8	3.5	dB
		LNA bypass state, 25°C		8		
IIP3	Input Third Order Intercept Point	At ANT port with LNA enabled. To be measured with total input power = -10dBm (-13 dBm/tone).	4	6.5		dBm
		At ANT port with LNA enabled and input tones at 2.412 and 2.437GHz. Total input power is 0 dBm (-3 dBm/tone).		10		
		At ANT port with LNA bypassed. Measured with total input power = 5 dBm (2dBm/tone).	18	26.5		
L_{loop}	ANT→RxA Loopback Isolation	PA enabled (T/R switch in Tx) and LNA bypassed (Loopback)	35	40	45	dB
I_{cc}	Operating Current	LNA enabled		8.5	14.5	mA
		LNA in bypass mode		1	100	µA

Functional State Table

Vc1	LNA_EN[1]	PA_EN[2]	Default State
1	1	0	Rx High Gain
1	0	0	Rx Bypass State
0	0	1	Tx
0	0	0	Sleep Mode[3]

[1] LNA is on while LNA_EN is high and LNA is off and in bypass mode when LNA_EN is low and VC1 is high.

[2] PA_EN controls PA enable and T/R switch logic.

[3] The FEM will be placed into sleep mode when all control signals are logic 0 or if they are all floating.

Part Markings

•	Pin 1 identifier
MSC	Company name
5586	Part number
YNNN	Trace code

Figure 3 · Typical Part Markings

Characteristic Curves: Tx S-parameters

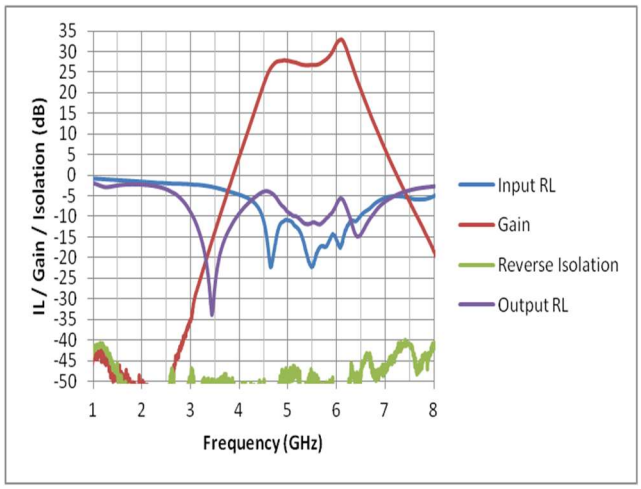


Figure 4 · Tx S-Parameters (VCC= 3.6V; 25°C)

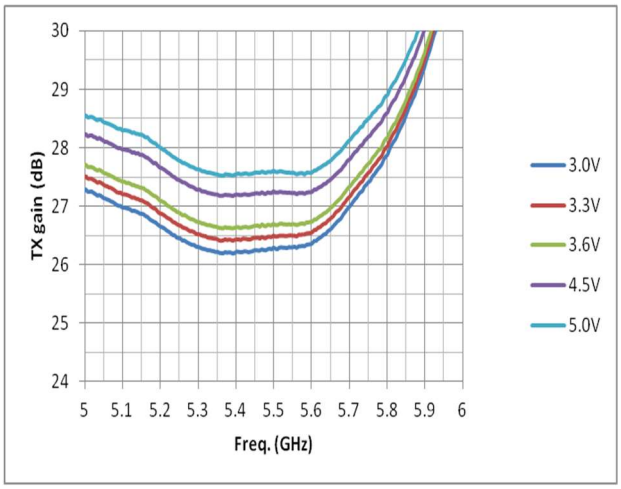


Figure 5 · Tx S-Parameters at 25°C

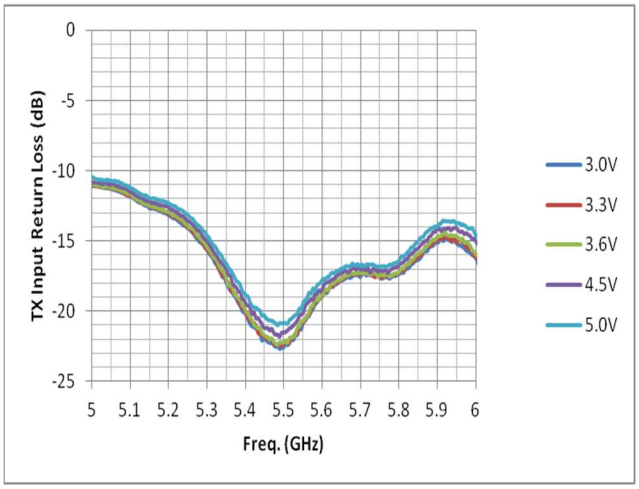


Figure 6 · Tx S-Parameters at 25°C

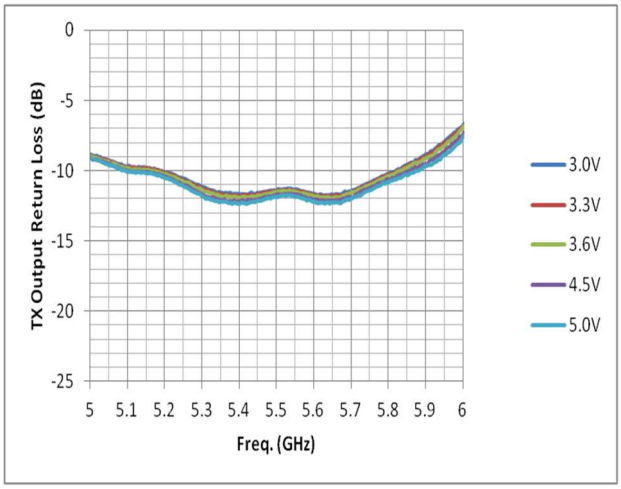


Figure 7 · Tx S-Parameters at 25°C

Characteristic Curves: Tx Linearity: 20MHz BW

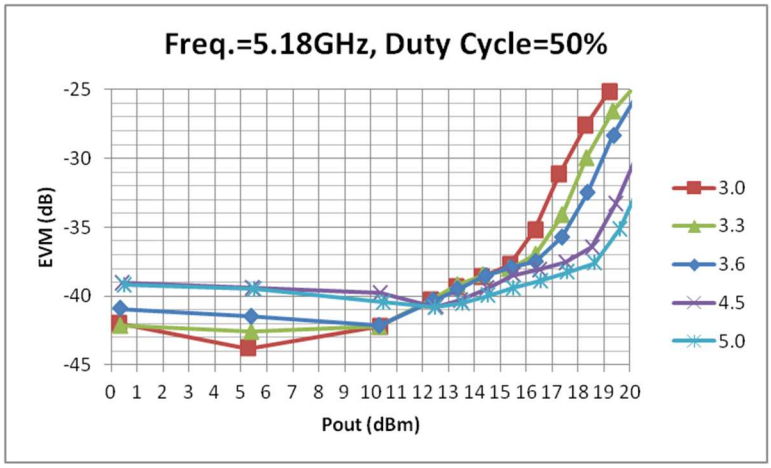


Figure 8 · Dynamic EVM (802.11ac, VHT-20, MCS 8)

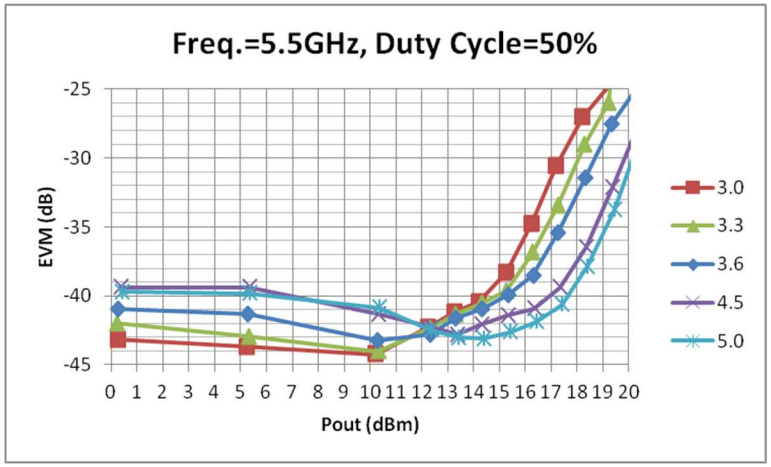


Figure 9 · Dynamic EVM (802.11ac, VHT-20, MCS 8)

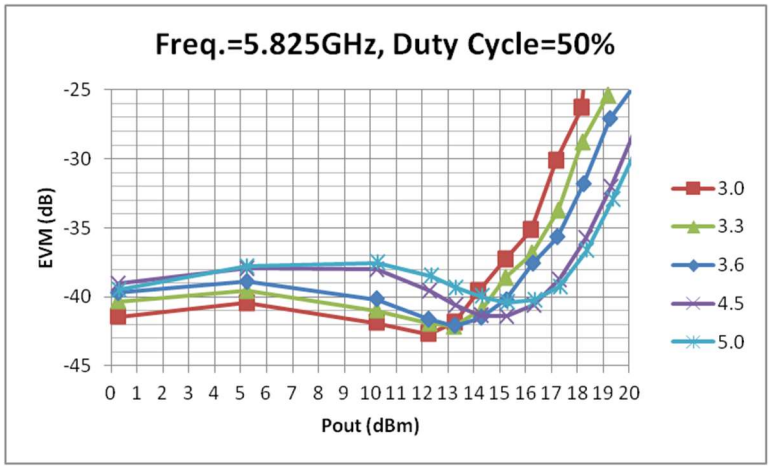


Figure 10 · Dynamic EVM (802.11ac, VHT-20, MCS 8)

Characteristic Curves: Tx Linearity: 80MHz BW

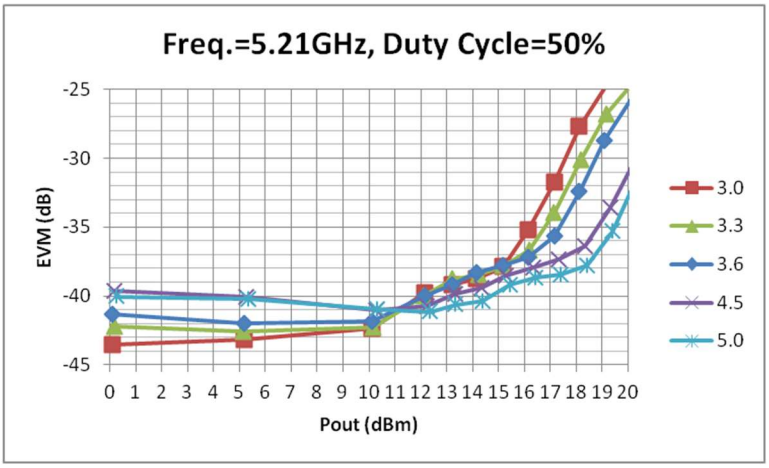


Figure 11 · Dynamic EVM (802.11ac, VHT-80, MCS 9)

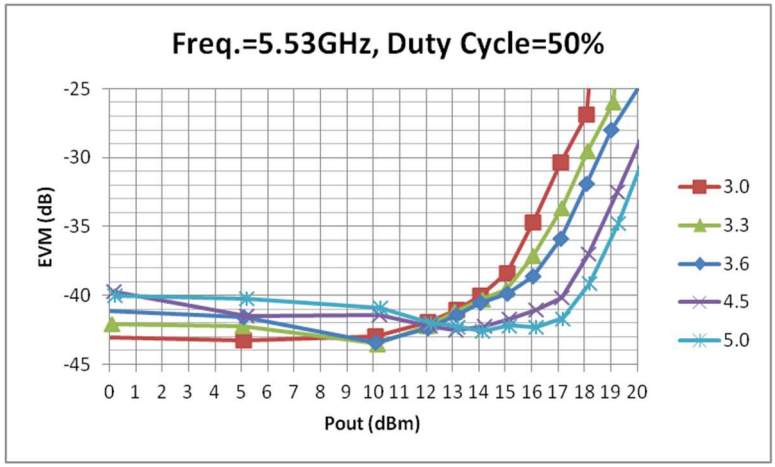


Figure 12 · Dynamic EVM (802.11ac, VHT-80, MCS 9)

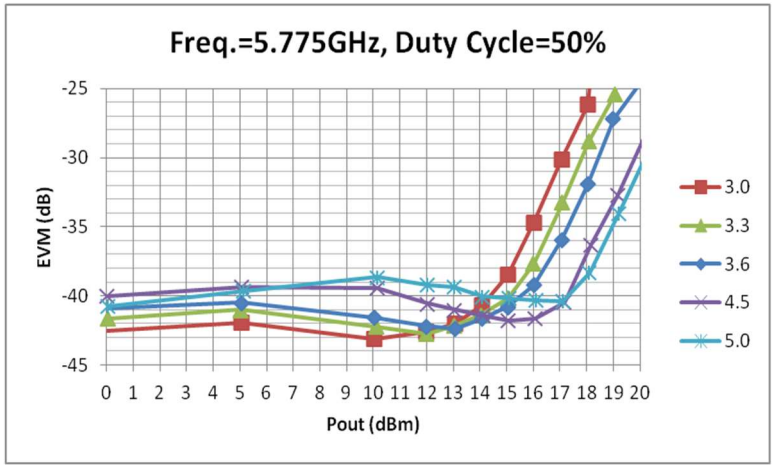


Figure 13 · Dynamic EVM (802.11ac, VHT-80, MCS 9)

Characteristic Curves: Rx High Gain S-parameters

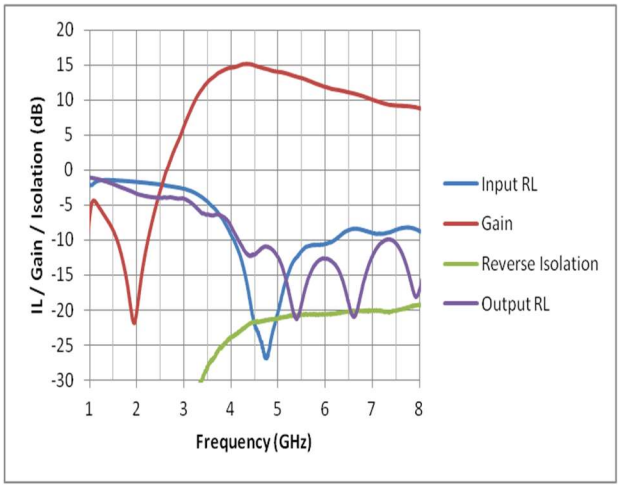


Figure 14 · Rx HG S-Parameters (VCC = 3.6V, 25°C)

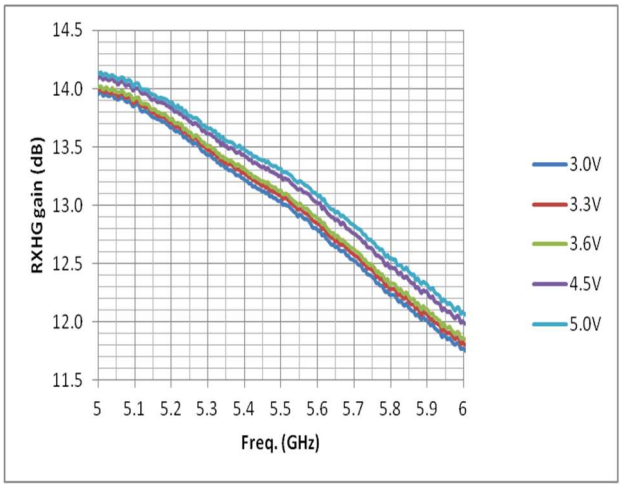


Figure 15 · Rx HG S-Parameters at 25°C

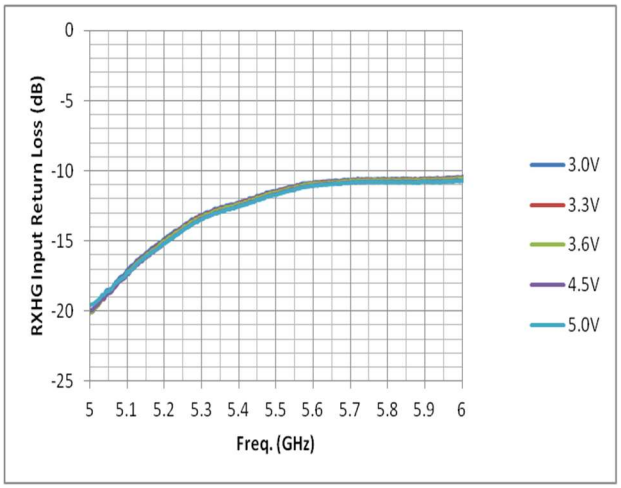


Figure 16 · Rx HG S-Parameters at 25°C

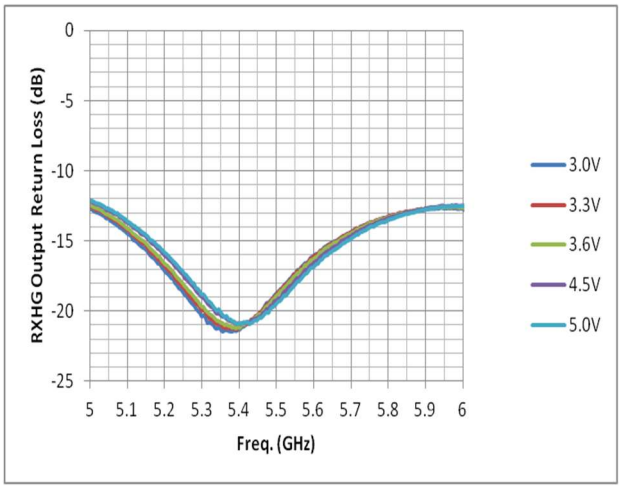


Figure 17 · Rx HG S-Parameters at 25°C

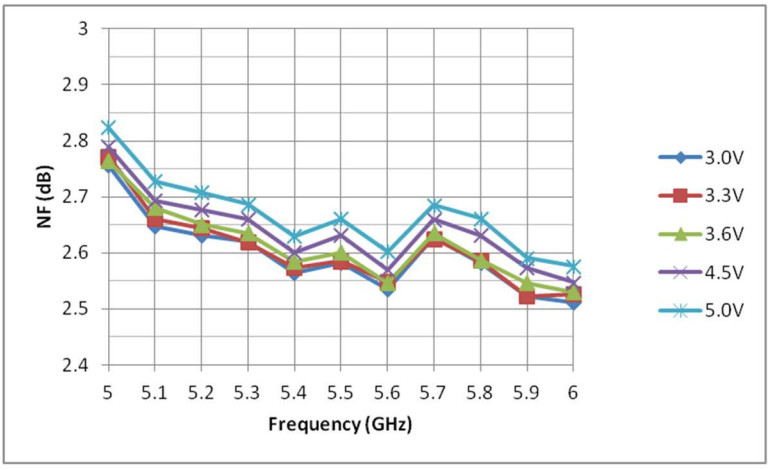


Figure 18 · LX5586 Noise Figure at 25C

Characteristic Curves: Rx Bypass Mode S-parameters

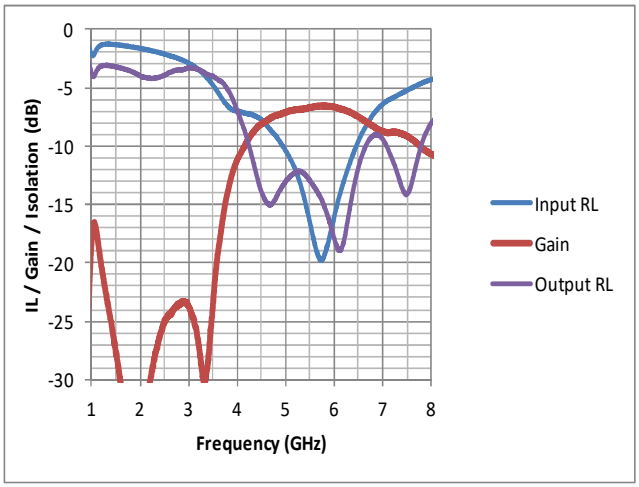


Figure 19 · Rx BP S-parameters (VCC = 3.6V, 25°C)

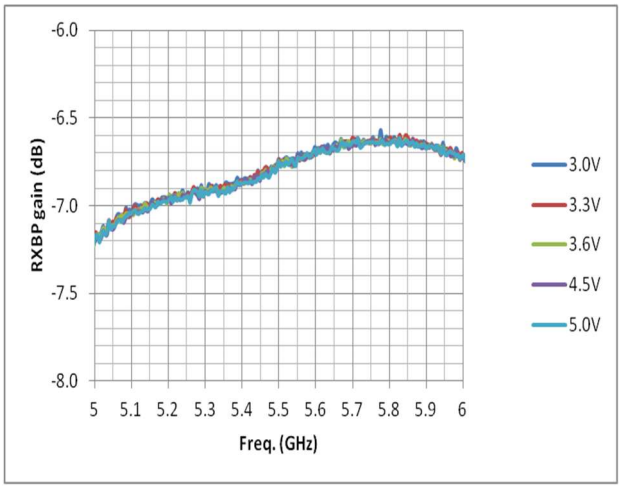


Figure 20 · Rx BP S-parameters at 25°C

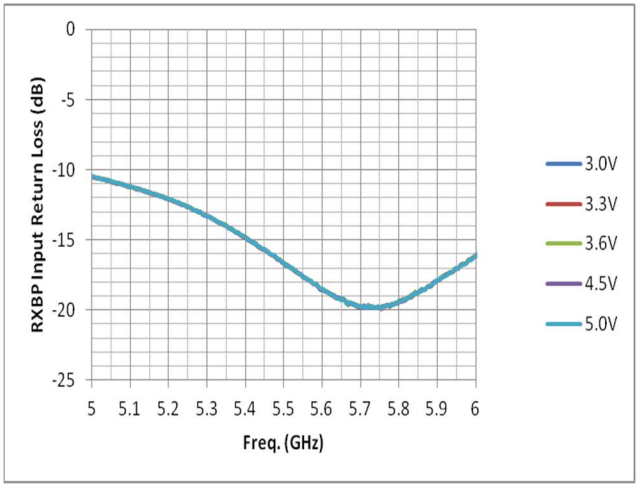


Figure 21 · Rx BP S-parameters at 25°C

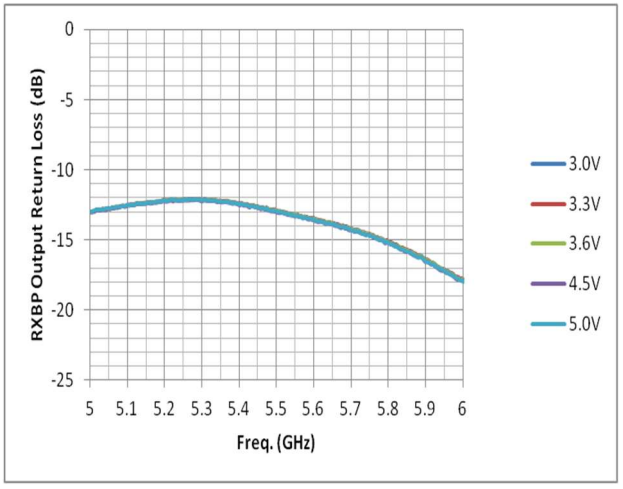
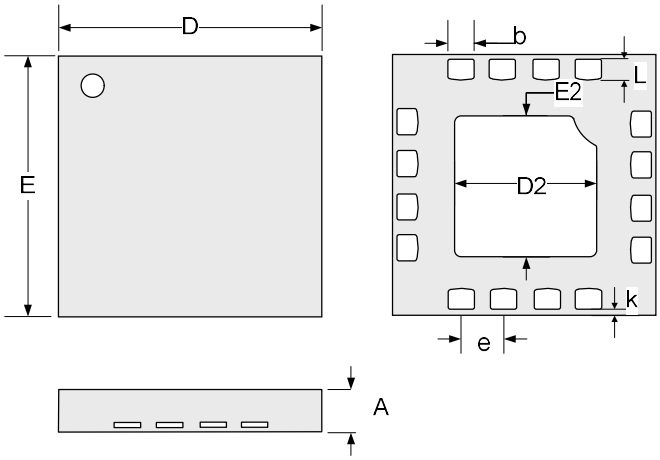


Figure 22 · Rx BP S-parameters at 25°C

Package Outline Dimensions

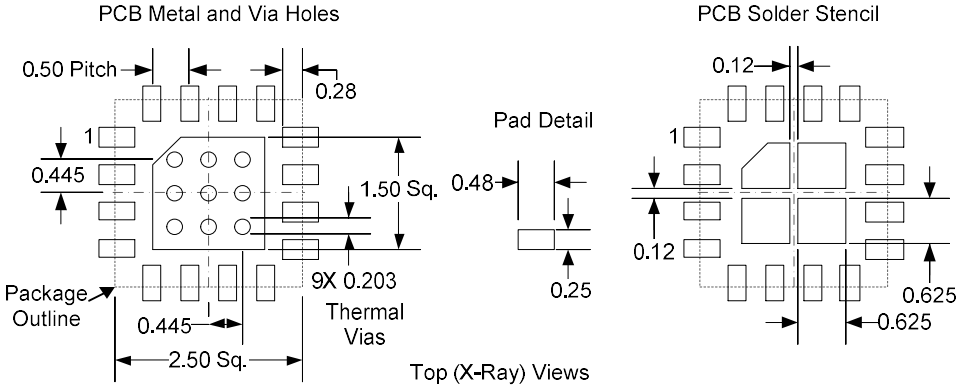
The package is halogen free and meets RoHS2 and REACH standards.

(MSL1, 260°C per JEDEC J-STD-020)



DIMENSION	MILLIMETERS	
	MIN	MAX
A		0.40
L	0.15	0.25
b	0.20	0.30
D	2.45	2.55
D2	1.3	1.40
E	2.45	2.55
E2	1.3	1.40
e	0.50 BSC	
k	0.05 REF.	

Figure 23 · 16 Pin QFN Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Unless specified dimensions are symmetrical about center lines.
3. OSP or NiAu planar surface finish recommended.
4. Non-Solder Mask Defined (NSMD) pads recommended for terminal pads.
5. Recommended tented thermal vias as shown with vias filled with solder.
6. Stencil thickness < 0.15mm.
7. Aperture design for thermal pads using multiple openings with 60 to 80% solder paste coverage.

Figure 24 · PCB Layout Footprint (Top View)

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