5.15–5.85 GHz 802.11ac Front End Module

Description

The LX5589H is a complete integrated 5GHz Front-End Module (FEM) for an IEEE 802.11ac system. It includes a highly linear 5GHz Power Amplifier (PA) with power detector, Low Noise Amplifier (LNA) with bypass capability, and SPDT antenna switch. This highly integrated FEM reduces the system footprint, bill of materials, and manufacturing cost.

The LX5589H is available in a 16-pin 2.5mm x 2.5mm QFN Package.

Features

- 5V Supply Voltage
- Integrated 5GHz PA, LNA, and SPDT Tx/Rx Switch
- P_{OUT} = 20dBm (256QAM / 80MHz)
- Bypassable LNA
- 2.5mm x 2.5 mm QFN package
- RoHS2 Compliant & Halogen Free

Applications

- Tablets
- Access Points
- Mobile Devices
- Notebooks
- Gaming

Block Diagram

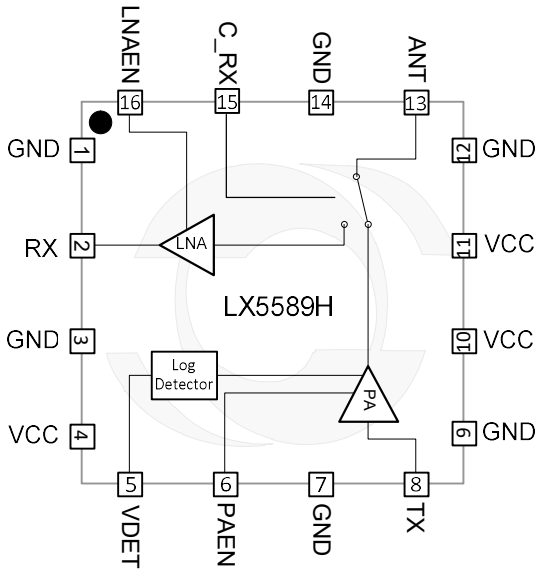


Figure 1 · Functional Block Diagram

Pin Configuration

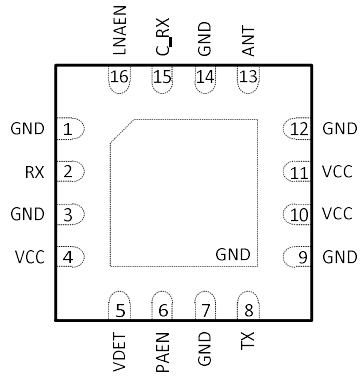


Figure 2 · Pinout (Top View)

Ordering Information

Ambient Temperature	Type	Package	Ordering Part Number	Packaging Type
-40°C to 85°C	RoHS2 compliant, Pb-free NiPdAu lead finish	QFN 2.5x2.5x0.9 16L	LX5589HLQ-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	GND	Ground
2	RX	DC blocked 50ohm output of LNA.
3	GND	Ground
4	VCC	5V nominal supply voltage
5	VDET	Output of transmit power detector
6	PAEN	Power amplifier digital enable
7	GND	Ground
8	TX	RF is 50 Ohm input to PA. DC is shorted to GND.

Pin Number	Pin Designator	Description
9	GND	Ground
10	VCC	5V nominal supply voltage.
11	VCC	5V nominal supply voltage.
12	GND	Ground
13	ANT	DC blocked 50 ohm antenna port.
14	GND	Ground
15	C_RX	T/R switch digital control
16	LNAEN	LNA digital enable

Absolute Maximum Ratings

Parameter	Value	Units
DC Supply Voltage (VCC)	5.5	V
Control Inputs (PAEN, LNAEN, C_RX)	3.6	V
Input Power at TX Port	+5	dBm
Maximum Junction Temperature (T_{JMAX})	+150	°C
Operational Ambient Temperature	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Peak Package Solder Reflow Temperature (30 seconds maximum exposure)	260	°C
Electrostatic Discharge Human Body Model (HBM), Class 1C	1000	V

Note: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The LX5589H ESD threshold level is >1000 VDC using Human Body Model (HBM) testing for all pins.

Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JP} Junction to Pad	12.6	°C/W
θ_{JA} Junction to Ambient	50.7	

Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A$ + (Power dissipation x θ_{JA}) or $T_J = T_P$ + (Power dissipation x θ_{JP}). In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics - General

Vcc=5.0V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Operating Supply Current						
VCC	Supply Voltage VCC		4.75	5	5.25	V
I_{SLEEP}	Sleep Mode Current	All control pins logic low.		10		µA
General Characteristics						
F_{RF}	Frequency Range		5.15	5.5	5.85	GHz
CHBW	Channel Bandwidth		20		80	MHz
V_{IH}	Control Logic Levels		3	3.3	3.6	V
V_{IL}			0		0.4	V
I_{CTRL}	Maximum Control Current	3.3V logic level		10		µA
Δt_{onPA} Δt_{offPA}	RX→TX Switching Time	Difference between falling edge of LNAEN and time when TX output has settled to within 90% of its final power.		400		ns
Δt_{rxlvl}	RX Gain Switching Time	Difference between edge of LNAEN and time when RX output has settled to within 90% of its final power.		100		ns
Δt_{onLNA}, Δt_{offLNA}	TX→RX Switching Time	Difference between edge of PAEN and time when RX output has settled to within 90% of its final power.		400		ns
T_{oper}	Operating temperature range	Case temperature	-40		85	°C
Ru	Ruggedness	P_{IN} = 5 dBm VSWR = 6:1 802.11n	No damage			

Electrical Characteristics - Detector

Vcc=5.0V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Detector Characteristics						
PD_{RANGE}	Power detector range		5		24	dBm
PD_{SENS}	Power Detector Sensitivity	Vdet RMS Sensitivity Measured during the first 16us of the preamble.		25		mV/dB
PD_{FREQ}	Power Detector Variation Over frequency	Vdet RMS variation (Max-Min) Measured in each of 3 sub-bands: 5.15-5.35, 5.47-5.725, 5.725-5.85 At any particular detector voltage, and at any particular supply voltage and temperature, the measured RF output power variation over the sub-band must fall within the limits shown.			1	dB
PD_{VFT}	Power detector Variation Over supply, process, and temperature	V_{DET} RMS variation (Max-Min) At any particular detector voltage, the measured RF output power variation over P, V, and T must fall within the limits shown.			2	dB
PD_{BW}	Power Detector Variation Over channel bandwidth	V_{DET} RMS variation (Max-Min) At any particular detector voltage, the measured RF output power variation over all channel bandwidths.			2	dB
V_{DET}	Power Detector Voltage	DC detector voltage No RF input		340		mV
		RMS detector voltage P_{OUT} = 24dBm Measured in first 16µs of preamble		930		
Z_{DET}	Detector Output Impedance			2.1		kΩ

Electrical Characteristics - Transmit

Vcc=5.0V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
TX Characteristics						
RL_{TXIN}	Input Return Loss	TX port PA enabled		10		dB
RL_{TXOUT}	Output Return Loss	ANT port PA enabled		10		dB
$GAIN_{TX}$	Power Gain	TX to ANT power gain PA enabled Within operating frequency band.	27	30		dB
$\Delta GAIN_{TX}$	Power Gain Variation	5150 to 5700 MHz		4		dB
		5700 to 5850 MHz		2		
P_{LIN}	Linear Output Power	802.11ac VHT80, MCS9 Dynamic EVM < -34 dB	19	20		dBm
		802.11n HT40, MCS7 Dynamic EVM < -30dB	21	22		
MASK	802.11ac Mask	Mask compliance power limit 802.11ac, VHT20, MCS0 RBW=100kHz, VBW= 30kHz 100% duty cycle Measured at 5.18GHz and 5.825GHz.	23	24		dBm
HD2	2nd harmonic PSD	802.11ac VHT20, MCS0 P_{OUT} = 23dBm		-35		dBm/MHz
HD3	3rd Harmonic PSD	802.11ac VHT20, MCS0 P_{OUT} = 23dBm		-40		dBm/MHz
Icc	Operating Current	P_{OUT} = 19 dBm		230		mA
		P_{OUT} = 23 dBm		325		
$I_{CQ,TX}$	Quiescent Current	V_{CC} = 5V No RF input. PA enabled		150		mA

Electrical Characteristics - Receive

Vcc=5.0V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Rx Characteristics						
RL_{RXIN}	Input Return Loss	At ANT port LNA enabled or bypassed		8		dB
RL_{RXOUT}	Output Return Loss	At RX port LNA enabled		14		dB
$GAIN_{RX}$	Small Signal Gain	LNA enabled	10.5	12		dB
		LNA bypassed	-9	-7		
$\Delta GAIN_{RX}$	Small Signal Gain Variation	Over single 80MHz-channel		0.5		dB
		Over entire F_{RF}		1		
Noise Figure	NF	LNA enabled T = 25°C		2.7		dB
IIP3	Input Third Order Intercept Point	At ANT port LNA enabled P_{IN} = -13 dBm/tone		9		dBm
		At ANT port LNA enabled P_{IN} = -3 dBm/tone F_{LO} = 2.412GHz, F_{HI} = 2.437GHz		10		
		At ANT port LNA bypassed P_{IN} = +2 dBm/tone		28		
$I_{CQ,RX}$	Operating Current	LNA enabled No RF input		10		mA
		LNA bypassed No RF input		10		µA

Functional State Table

C_RX	LNAEN	PAEN	Operation Mode
1	1	0	RX, LNA enabled
1	0	0	RX, LNA bypassed
0	0	1	TX
0	0	0	Sleep / Standby Mode

[1] Logic HI / LOW voltage ranges are as defined previously.

[2] All control signals must be driven. Operation Mode is undefined if any control signal is floating.

Part Markings

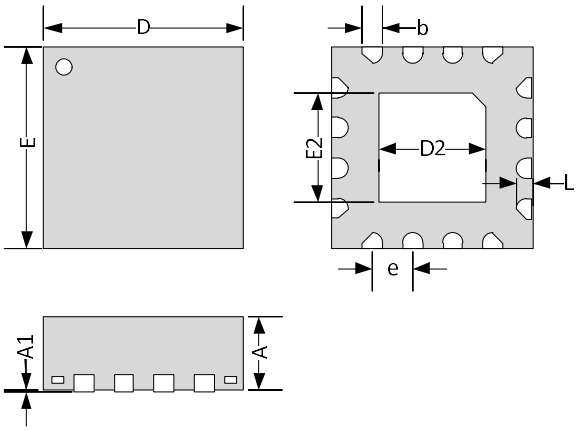
•	Pin 1 identifier
MSC	Company name
589H	Part number
YNNN	Trace code

Figure 3 · Typical Part Markings

Package Outline Dimensions

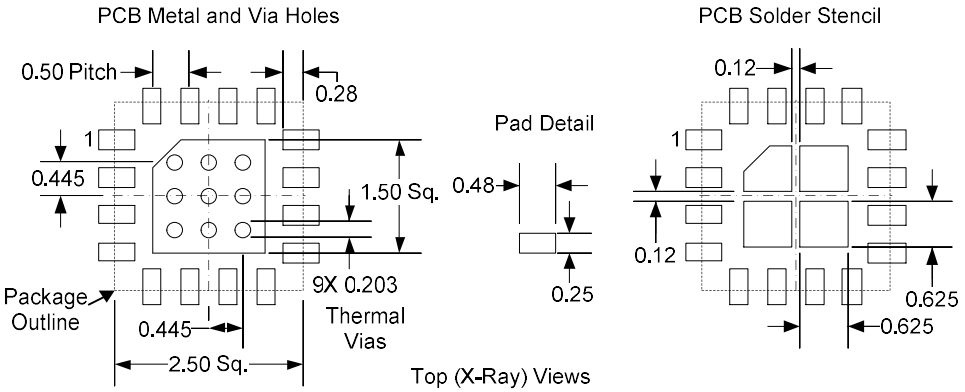
The package is halogen free and meets RoHS2 and REACH standards.

(MSL1, 260°C per JEDEC J-STD-020)



DIMENSION	MILLIMETERS	
	MIN	MAX
A		1.00
A1	0.01	0.05
L	0.15	0.25
b	0.20	0.30
D	2.45	2.55
D2	1.30	1.40
E	2.45	2.55
E2	1.30	1.40
e	0.50 BSC	

Figure 4 · 16 Pin QFN Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Unless specified dimensions are symmetrical about center lines.
3. OSP or NiAu planar surface finish recommended.
4. Non-Solder Mask Defined (NSMD) pads recommended for terminal pads.
5. Recommended tented thermal vias as shown with vias filled with solder.
6. Stencil thickness < 0.15mm.
7. Aperture design for thermal pads using multiple openings with 60 to 80% solder paste coverage.

Figure 5 · PCB Layout Footprint (Top View)

Evaluation Board Schematic

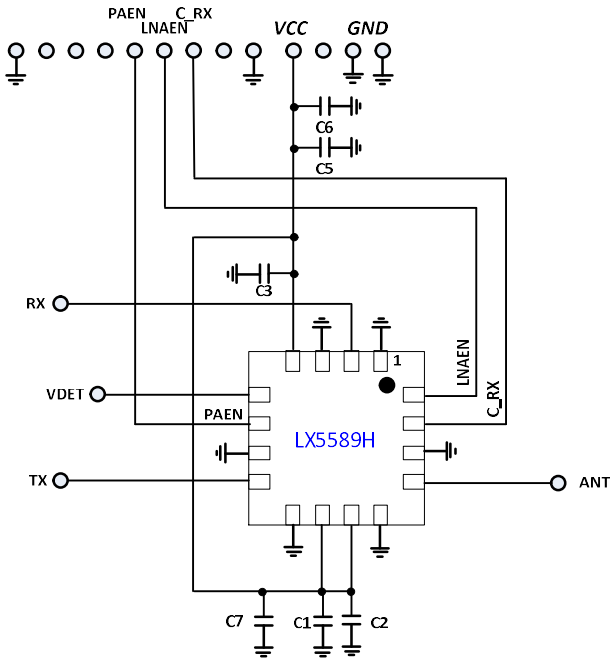


Figure 6 · Evaluation Board Schematic

Evaluation Board BOM

Part Number	Value	Package Size	Component
GRM188R71A105KA61D	1uF	0402	C1, C2, C3, C5
F981C475MMA	4.7uF	0603	C6
C1608X5R1A685K080AC	6.8uF	0603	C7

Figure 7 · Evaluation Board Bill of Materials

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