Dual Band 802.11ac Front End Module

Description

The LX5591 is a complete integrated dual band Front End Module (FEM) for an IEEE 802.11ac system. It includes highly linear 2.4 and 5GHz Power Amplifier (PAs) with power detector, 2.4 and 5 GHz Low Noise Amplifiers (LNA) with bypass capability, an integrated diplex filter, and T/R switches on both bands.

The LX5591 is available in a 28-pin 4mm x 3mm QFN Package.

Features

- Single Supply Voltage 3V to 3.6V
- Integrated 2.4 and 5GHz PA, LNA, SPDT T/R switch (5GHz) and SP3T T/R/BT switch (2.4GHz), and integrated diplex filter
- P_{OUT} = 16dBm (5 GHz) and 16dBm (2.4 GHz) with -35dB EVM (256QAM/80MHz)
- Bypassable LNA with Low NF
- RoHS2 Compliant & Halogen Free

Applications

- WiFi Access Points
- Notebooks

Block Diagram

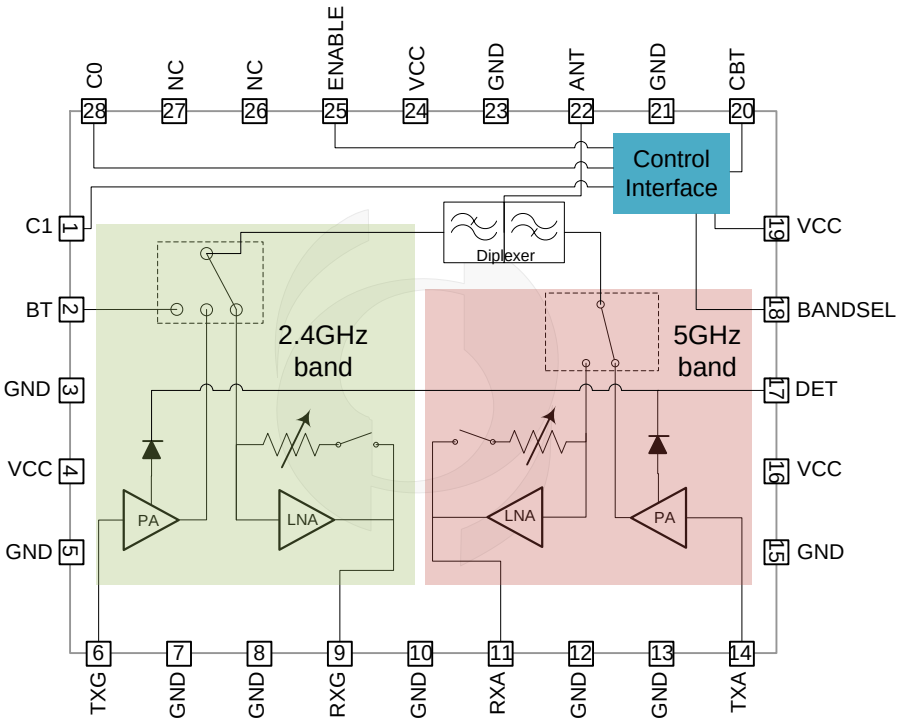


Figure 1 · Functional Block Diagram

Pin Configuration

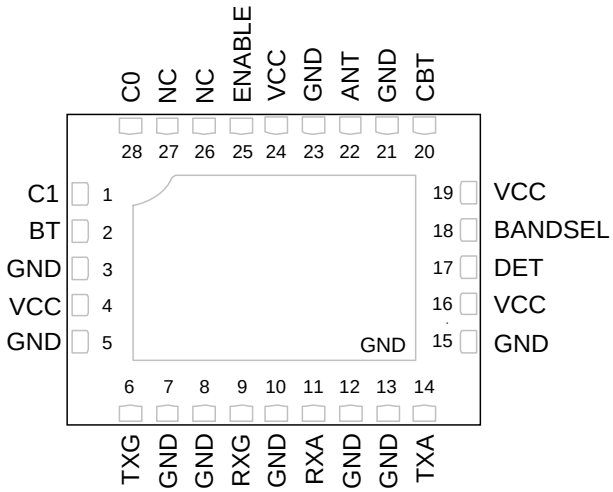


Figure 2 · Pinout (Top View)

Top mark
- MSC
- 5591
- YWWNNN = Trace code

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS2 compliant, Pb-free NiPdAu finish	QFN 4x3x0.9 28L	LX5591LQ -TR	Tape and Reel

Pin Descriptions

Pin Number	Pin Designator	Description
1	C1	Mode control
2	BT	Bluetooth RF input/output 50 Ohm, DC blocked
3	GND	Ground
4	VCC	3.3V nominal supply voltage
5	GND	Ground
6	TXG	Low-band TX RF input 50 Ohm, DC is tied to GND
7	GND	Ground
8	GND	Ground
9	RXG	Low-band RX output 50 Ohm, DC blocked
10	GND	Ground
11	RXA	High-band RX output 50 Ohm, DC blocked
12	GND	Ground
13	GND	Ground
14	TXA	High-band TX RF input 50 Ohm, DC is tied to GND
15	GND	Ground
16	VCC	3.3V nominal supply voltage
17	DET	Power Detector Output
18	BANDSEL	Band select control pin
19	VCC	Must be connected to 3.3V supply (logic high).
20	CBT	Bluetooth control pin
21	GND	Ground
22	ANT	Antenna (Common) RF Input/Output 50 Ohm, DC is tied to GND
23	GND	Ground
24	VCC	3.3V nominal supply voltage
25	ENABLE	Chip enable control pin
26	NC	NC
27	NC	NC
28	C0	Mode control pin

Absolute Maximum Ratings

Parameter	Value	Units
DC supply voltage	4.2	V
Control input voltage (C0, C1, CBT, ENABLE, BANDSEL)	3.6	V
RF input power at TX ports (with 50 Ohm load at ANT port)	+10	dBm
Maximum junction temperature (T_J max)	+150	°C
Maximum storage temperature	-65 to +150	°C
Peak package solder reflow temperature (30 seconds maximum exposure)	260	°C
Electrostatic discharge Human Body Model (HBM), Class 1C	1000	V

Note: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Properties

Thermal Resistance	Typ	Units
G-band θ_{JP} Junction to Pad	22	°C/W
A-band θ_{JP} Junction to Pad	30	
G-band θ_{JA} Junction to Ambient	37	
A-band θ_{JA} Junction to Ambient	45	

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A +$ (Power dissipation x θ_{JA}) or $T_J = T_P +$ (Power dissipation x θ_{JP}). In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics - General

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
F_{RFLB}	Low band frequency range		2.402		2.482	GHz
F_{RFHB}	High band frequency range		5.15		5.85	
CHBW	Channel bandwidth	Low Band	20		40	MHz
		High Band	20		80	
VCC	Supply voltage		3	3.3	3.6	V
V_{HI}	Control pin logic levels (C0, C1, ENABLE,CBT, BANDSEL)	High	VCC-0.2	VCC	VCC+0.2	
V_{LOW}		Low	0	0	0.4	
I_{SLEEP}	Sleep mode current draw	ENABLE pin low, all control pins except CBT low, CBT in any state.		50		µA
$I_{standby}$	Standby current	In any Rx bypass state.		50		
I_{CRTL}	Control pin current	Control pin current for all control pins except CBT. Current is measured with logic high applied to pin.		5		µA
I_{CBT}	CBT control pin current	BT control pin current consumption with logic high applied to pin.		5		
Δt_{SLEEP}	Sleep to Rx switching time	Difference between edge of ENABLE control pin transition and time when Rx output has settled to within 90% of its final power.			500	ns
Δt_{onPA} Δt_{offPA}	Rx toTx switching time	Difference between edge of control pin transition and time when Tx output has settled to within 90% of its final power.			500	ns
Δt_{onLNA}, Δt_{offLNA}	Tx to Rx switching time	Difference between edge of control pin transition and time when Rx output has settled to within 90% of its final power.			1000	
Δt_{rxlvl}	Rx gain switching time	Difference between edge of control pin transition and time when Ant/Rx output has settled to within 90% of its final power.			500	ns
T_{oper}	Operating temperature range	Case temperature	-40		85	°C

Electrical Characteristics - Detector

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$PD_{RANGE-LB}$	Power detector range: Low band	Mode = TXG Power range over which PD_{SENS} requirements are met in low band.	7		22	dBm
$PD_{RANGE-HB}$	Power detector range: High band	Mode = TXA Power range over which PD_{SENS} requirements are met in high band.	7		21	
PD_{SENS}	Power detector sensitivity	$V_{DET-RMS}$ sensitivity. Sensitivity to be measured during first 16µs of preamble.	5		150	mV/dB
$PD_{VAR,F}$	Power detector variation over frequency	Variation in output power required to maintain a constant $V_{DET-RMS}$ output voltage. Power range, LB = 10-22dBm Power range, HB = 10-21dBm			±1	dB
$PD_{VAR,VT}$	Power detector variation over supply, and temperature				±2	
$PD_{VAR,BW}$	Power detector variation over channel bandwidth				±0.75	
$V_{DET-NORF}$	Detector voltage (RMS) – low band	Mode = TXG No RF Input		220		mV
	Detector voltage (RMS) – high band	Mode = TXA No RF Input		220		mV
$V_{DET-PEAK}$	Detector voltage (Peak) – low band	Mode = TXG P_{OUT} = 22 dBm Peak voltage at DET pin Measured in first 16µs of preamble.		1000		mV
	Detector voltage (Peak) – high band	Mode = TXA P_{OUT} = 21dBm Peak voltage at DET pin Measured in first 16µs of preamble.		925		mV
Z_{DET}	Detector output impedance			2.25		kΩ

Electrical Characteristics – Transmit Low-Band

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$S11_{TXG}$	Input return loss	At TXG port with low-band PA enabled		10		dB
$S22_{TXG}$	Output return loss	At ANT port with low-band PA enabled		8		
$S21_{TXG}$	Power gain	Small signal gain in operating frequency band.		29		
$\Delta S21_{TXG}$	Power gain variation	Over single 40MHz-channel at 2422, 2462MHz.		1		
		Over entire F_{RFLB}		2		
$P_{LIN, TXG}$	Linear output power	802.11ac, VHT40, MCS9 Dynamic EVM < -34 dB		16		dBm
		802.11n, HT40, MCS7 Dynamic EVM < -30dB		18		
$P_{MASK,TXG}$	Spectral emission mask power	802.11b, 1 Mbps, Root Cosine		21		dBm
$P_{HD2,TXG}$	2nd Harmonic PSD power	802.11b, 1Mbps PSD < -48dBm/MHz		21		dBm
$P_{HD3,TXG}$	3rd Harmonic PSD power	802.11b, 1Mbps PSD < -48dBm/MHz		21		dBm
$I_{CC,TXG}$	Operating current	802.11ac, VHT40, MCS9 P_{OUT} = 15dBm		185		mA
		802.11b, 1Mbps P_{OUT} = 20dBm		240		
$I_{CQ,TXG}$	Quiescent current	No RF input. PA enabled		150		
$P_{IN,MAX,TXG}$	Maximum RF drive at TXG pin	Continuous into 6:1 VSWR at Ant port.	0			dBm

Electrical Characteristics – Receive Low-Band

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$S11_{RXG}$	Input return loss	At ANT port for all low-band Rx gain states		10		dB
$S22_{RXG}$	Output return loss	At RXG port for all low-band Rx gain states		10		dB
$S21_{RXG}$	Power gain	Control Logic **C1** **C0**				dB
		LNA Enabled Low Low		12		
		LNA Bypassed Low Attenuation Low High		-3		
		LNA Bypassed High Attenuation High Low		-9		
$G_{STEP,RXG}$	Gain step	Change in gain between high and low gain state. High Gain [C1, C0] = [L,L] Bypass, Max Atten. [C1, C0] = [H,L]		21		dB
$\Delta S21_{RXG}$	Power gain variation	Over single 40MHz channel at 2422 and 2462MHz		1		dB
		Over entire F_{RFLB}		2		dB
NF_{RXG}	Noise figure	Control Logic **C1** **C0**		3		dB
		LNA Enabled Low Low				
$IIP3_{RXG}$	Input Third Order Intercept Point	At ANT port with LNA enabled. P_{IN} = -15 dBm (Total power) 10MHz Tone spacing		7		dBm
		At ANT port with LNA bypassed. Measured with 0 dBm input power (total) and 10MHz tone spacing.		30		dBm
$I_{CC,RXG}$	Operating current	LNA enabled		9		mA

Electrical Characteristics – Bluetooth

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$S11_{BT}$	Input return loss	At ANT port for CBT high		8		dB
$S22_{BT}$	Output return loss	At BT port for CBT high		10		
$S21_{BT}$	Insertion loss	ANT port to BT port with CBT high		2.2		
$\Delta S21_{BT}$	Insertion loss variation	Over entire F_{RFLB}		±0.25		

Electrical Characteristics – Transmit High-Band

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$S11_{TXA}$	Input return loss	At TXA port with high-band PA enabled		10		dB
$S22_{TXA}$	Output return loss	At ANT port with high-band PA enabled		8		
$S21_{TXA}$	Power gain	Small signal gain in operating frequency band.		27		
$\Delta S21_{TXA}$	Power gain variation	Over single 80MHz-channel at 5.21, 5.53 and 5.775 GHz		1		
		Over entire F_{RFLB}		2		
$P_{LIN,TXA}$	Linear output power	802.11ac, VHT80, MCS9 Dynamic EVM < -34 dB		16		dBm
		802.11n, HT40, MCS7 Dynamic EVM < -30dB		18		
$P_{MASK,TXA}$	Spectral emission mask power	802.11ac, VHT20, MCS0		20		dBm
$P_{HD2,TXA}$	2nd Harmonic PSD power	802.11ac, VHT20, MCS0 PSD < -48dBm/MHz		20		dBm
$P_{HD3,TXA}$	3rd Harmonic PSD power	802.11ac, VHT20, MCS0 PSD < -48dBm/MHz		20		dBm
$I_{CC,TXA}$	Operating current	802.11ac, VHT80, MCS9 P_{OUT} =15 dBm		210		mA
		802.11ac, VHT20, MCS9 P_{OUT} =19 dBm		290		
$I_{CCQ,TXA}$	Quiescent current	No RF input. PA enabled.		120		
$P_{IN,MAX,TXA}$	Maximum RF drive at TXA pin	Continuous into 6:1 VSWR at Ant port	0			dBm

Electrical Characteristics – Receive High-Band

(Vcc=3.3V, T_A=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$S11_{RXA}$	Input return loss	At ANT port for all high-band Rx gain states		9		dB
$S22_{RXA}$	Output return loss	At RXA port for all high-band Rx gain states		10		
$S21_{RXA}$	Power gain	Control Logic **C1** **C0**				
		LNA Enabled Low Low		11		
		LNA Bypassed Low High Low Attenuation		-4		
		LNA Bypassed High Low High Attenuation		-7		
$G_{STEP,RXA}$	Gain step	Change in gain between high and low gain state. High Gain [C1, C0] = [L,L] Bypass, Max Atten. [C1, C0] = [H,L]		18		
$\Delta S21_{RXA}$	Power gain variation	Over single 80MHz channel		1		
		Over entire F_{RFHB}		2.6		
NF_{RXA}	Noise figure	Control Logic **C1** **C0**		3.3		dB
		LNA Enabled Low Low				
$IIP3_{RXA}$	Input Third Order Intercept Point	At ANT port with LNA enabled. P_{IN} = -15 dBm (Total power) 10MHz Tone spacing		7		dBm
		At ANT port with LNA bypassed. P_{IN} = 0 dBm (Total power) 10MHz Tone spacing		28		
$I_{CC,RXA}$	Operating current	LNA enabled		11		mA

Functional State Table

BAND SEL	C1	C0	CBT	ENABLE	Mode Name	State
0	0	0	0	1	RXG-HG	Low band Rx mode LNA in high gain state.
0	0	1	0	1	RXG-BP1	Low band Rx mode LNA bypassed Minimum attenuation
0	1	0	0	1	RXG-BP2	Low band Rx mode LNA bypassed Maximum attenuation
0	1	1	0	1	TXG	Low band Tx mode PA enabled
0	X	X	1	1	BT	Bluetooth mode All low band Rx and Tx functions are disabled.
1	0	0	0	1	RXA-HG	High band Rx mode LNA in high gain state.
1	0	1	0	1	RXA-BP1	High band Rx mode LNA bypassed Minimum attenuation.
1	1	0	0	1	RXA-BP2	High band Rx mode LNA bypassed Maximum attenuation
1	1	1	0	1	TXA	High band Tx mode PA enabled
1	0/1	0/1	1	1	BT-HB	Concurrent high band + BT mode High band RF path operates according to C0 & C1 settings. Low band RF path in BT mode.
X	X	X	1	0	BT-SLEEP	Standby / Sleep with BT mode. BT RF path enabled.
X	X	X	0	0	SLEEP	Standby / Sleep mode State of RF switches are undefined.

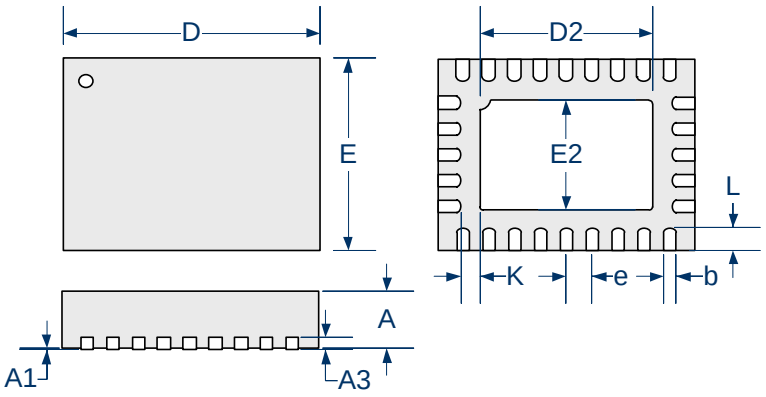
Notes:

X=Don’t care; control pin can be either logic LOW or HIGH
All control inputs must be driven to either logic LOW or HIGH. Proper operation is not guaranteed if any control pin is left floating or in a HI-Z condition.

Pull-down resistors >1MΩ are present on BANDSEL, ENABLE, C0, and C1 control pin inputs, but should not be relied on for proper operation.

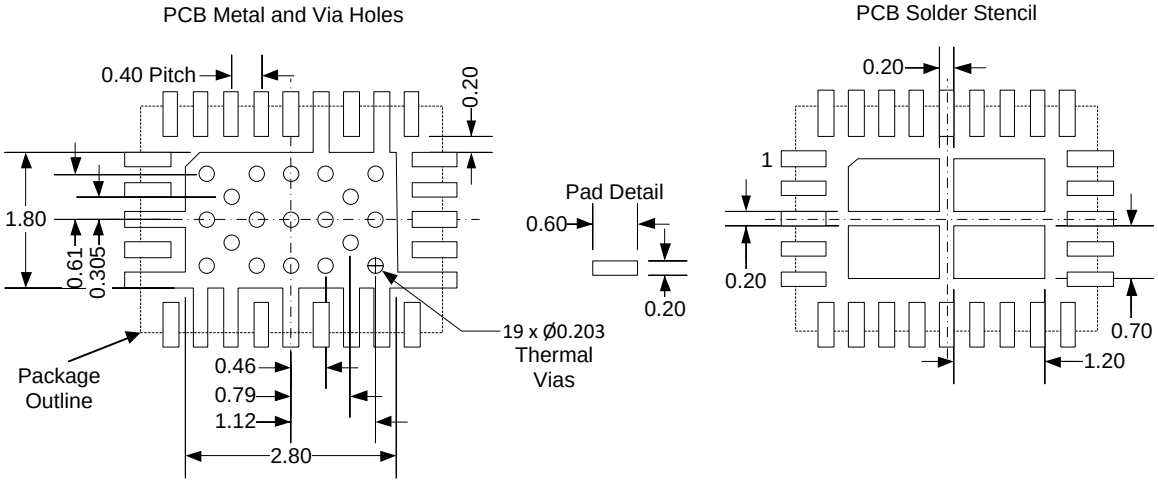
Package Outline Dimensions

The package is halogen free and meets RoHS2 and REACH standards.



DIM	Millimeters		
	MIN	TYP	MAX
A	0.8	0.9	1.0
A1	0.00	0.02	0.05
A3		0.20 Ref	
b	0.15	0.20	0.25
D	3.95	4.00	4.05
E	2.95	3.00	3.05
e	0.35	0.40	0.45
D2	2.55	2.70	2.80
E2	1.55	1.70	1.80
K	0.20	N/A	N/A
L	0.25	0.35	0.40

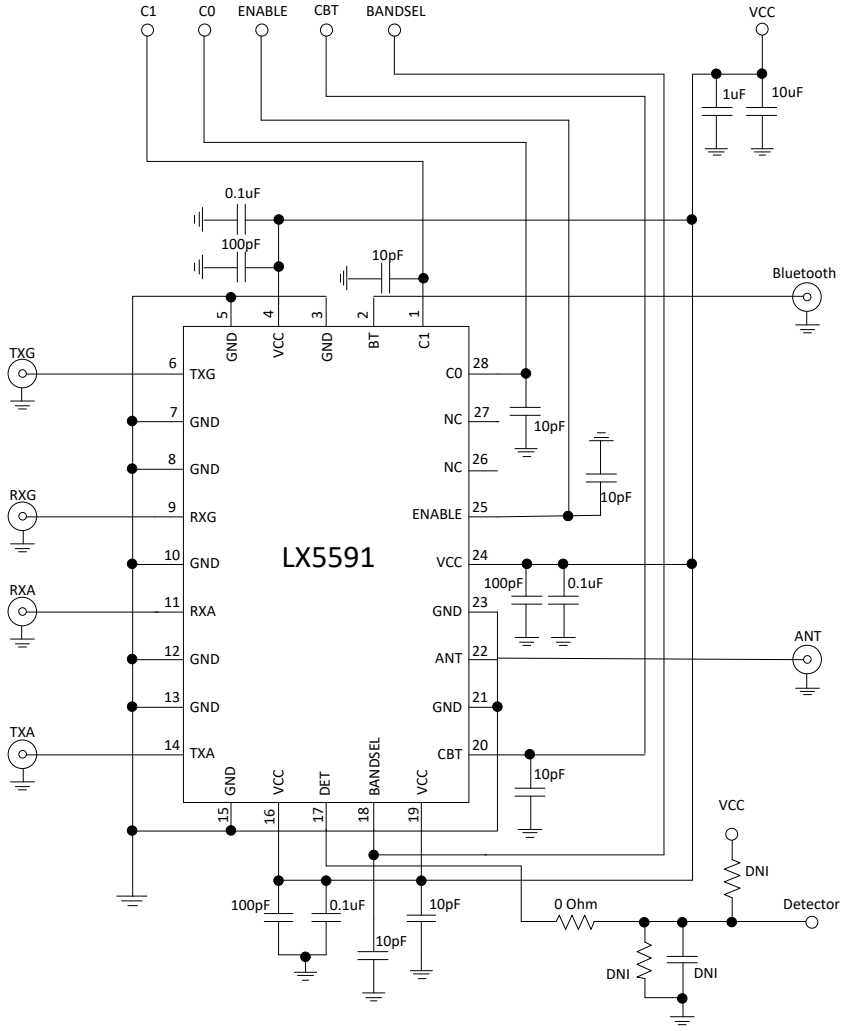
Figure 3 · 28 Pin QFN Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Unless specified dimensions are symmetrical about center lines.
3. OSP or NiAu planar surface finish recommended.
4. Non-Solder Mask Defined (NSMD) pads recommended for terminal pads.
5. Recommended tented thermal vias as shown with vias filled with solder.
6. Stencil thickness < 0.15mm.
7. Aperture design for thermal pads using multiple openings with 60 to 80% solder paste coverage.

Figure 4 · PCB Layout Footprint (Top View)

Evaluation Board Schematic



Notes :

1. Place all bypass caps close to pins.
2. DNI - Do Not Install. Prepare the place holder.
3. BT, RXG, and RXA pins are internally DC blocked with a series capacitor.
   If an external DC voltage is applied to these pins, the RF signal may be distorted because the combination of DC+RF signal can trigger the ESD diodes on these pins. If any significant external DC voltage is applied to these pins, external blocking capacitors may be required.
4. TXG and TXA pins are shorted to GND through internal inductors.DC blocking capacitors will be required if an external DC voltage is applied to these pins.

Figure 5 · Evaluation Board Schematic

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