ZARLINK SEMICONDUCTOR

VoiceEdge

Le79112

VoiceEdge™ Control Processor
VE790 Series

A Legerity Voice Solution

APPLICATIONS

- CO
- DLC
- IVD
- Voice-enabled DSLAM
- PBX/KTS
- Test head
- Pair gain

FEATURES

- Software interface using VP API-II
- Software downloadable, field upgradeable, expandable
- Provides expanded line and circuit testing in conjunction with Legerity's VE790 Series chip sets
- DTMF detection (Q.24, up to 16 channels simultaneously)
- Quad tone and howler tone generation
- Arbitrary single tone detection
- 15-kHz energy detection
- SNR tests
- Dial pulse measurement
- Aggregated codec/filter control lowers demand on host micro-processor
- Master MPI port to the Legerity SLAC™ device
- Slave PCM port can be used as an alternative
- Internal PLL and timing circuits with programmable dividers
- Serial and parallel controller interface options
- 16 I/Os to support controlling up to 32 lines
- 3.3-V compliant I/O; Internal 3.3-V to 2.5-V linear regulator for the core logic

ORDERING INFORMATION

Device	Package (Green)[1]	Packing[2]
Le79112AKVC	128-pin TQFP	Tray
Le79112ADGC	144-pin BGA	Tray

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

The Le79112 VoiceEdge™ Control Processor (VCP) is a digital signal processing platform that works with the Legerity VE790 series chip sets using the MPI interface, PCM port, and an interrupt line from the codec/filter. The primary functions of the Le79112 VCP are to program and control the codec/filter to implement enhanced call control and test capabilities.

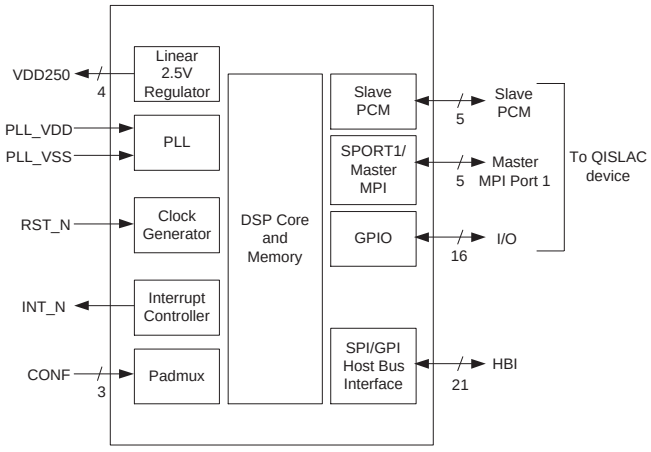
The Le79112 VCP, in combination with the VE790 series chip set, supports up to 32 channels of universal telephone line interface with higher level voice functionality. This enables the design of a low-cost, high-performance, fully software programmable line interface for multiple country applications. All AC, DC, signaling parameters, and data are fully programmable. Additionally, the Le79112 VCP has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

The Le79112 VCP is compatible with Le79Q2281, Le79Q2284, and Le792288 ISLAC devices.

RELATED LITERATURE

- 081237 Le79232 SLIC Device Data Sheet
- 081152 Le79242 SLIC Device Data Sheet
- 081185 Le79252 SLIC Device Data Sheet
- 081256 Le79228 SLAC™ Device Data Sheet
- 081190 Le792288 Octal SLAC™ Device Data Sheet

BLOCK DIAGRAM



NOTE: On August 3, 2007, Zarlink Semiconductor acquired the products and technology of Legerity Holdings.

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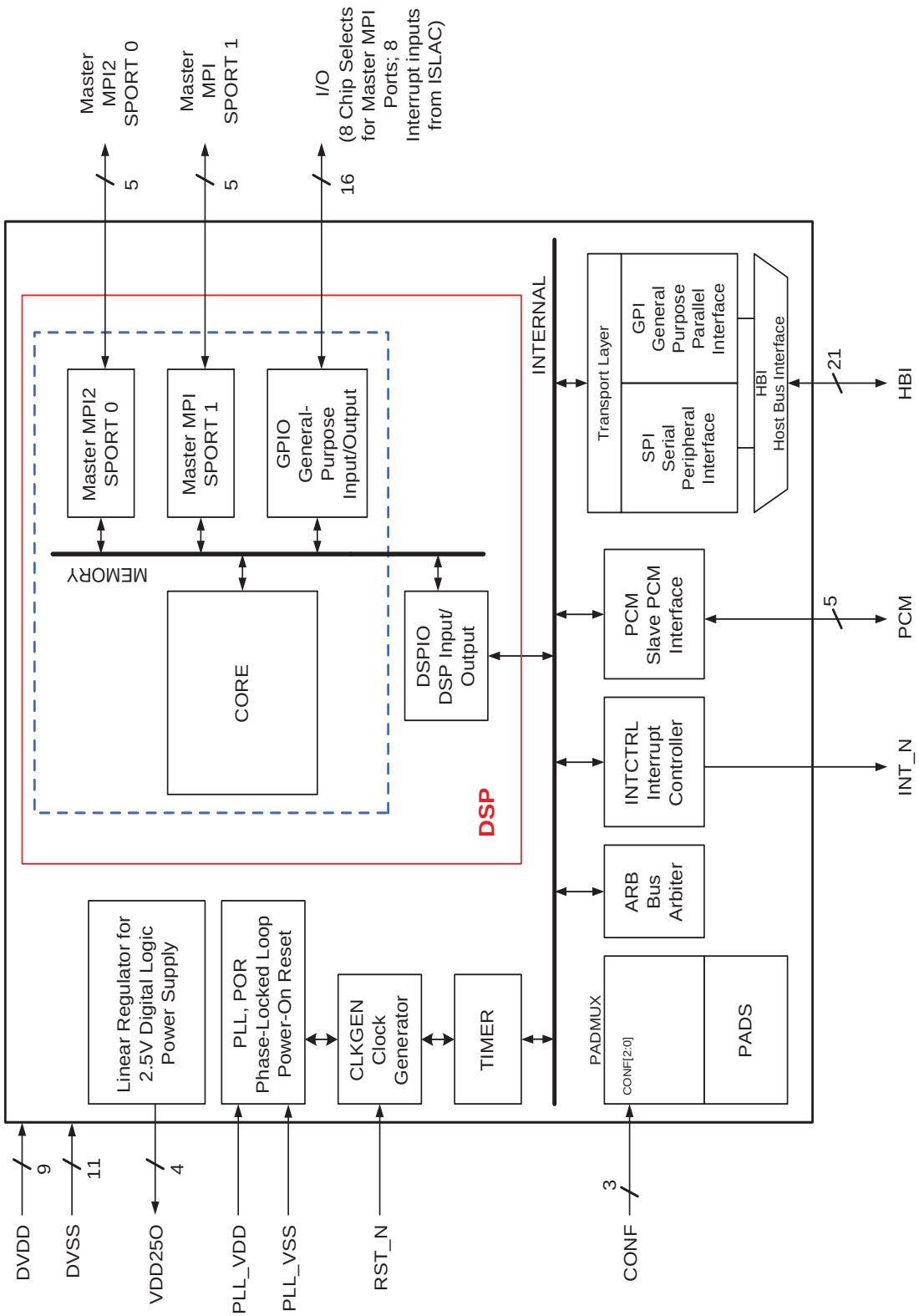
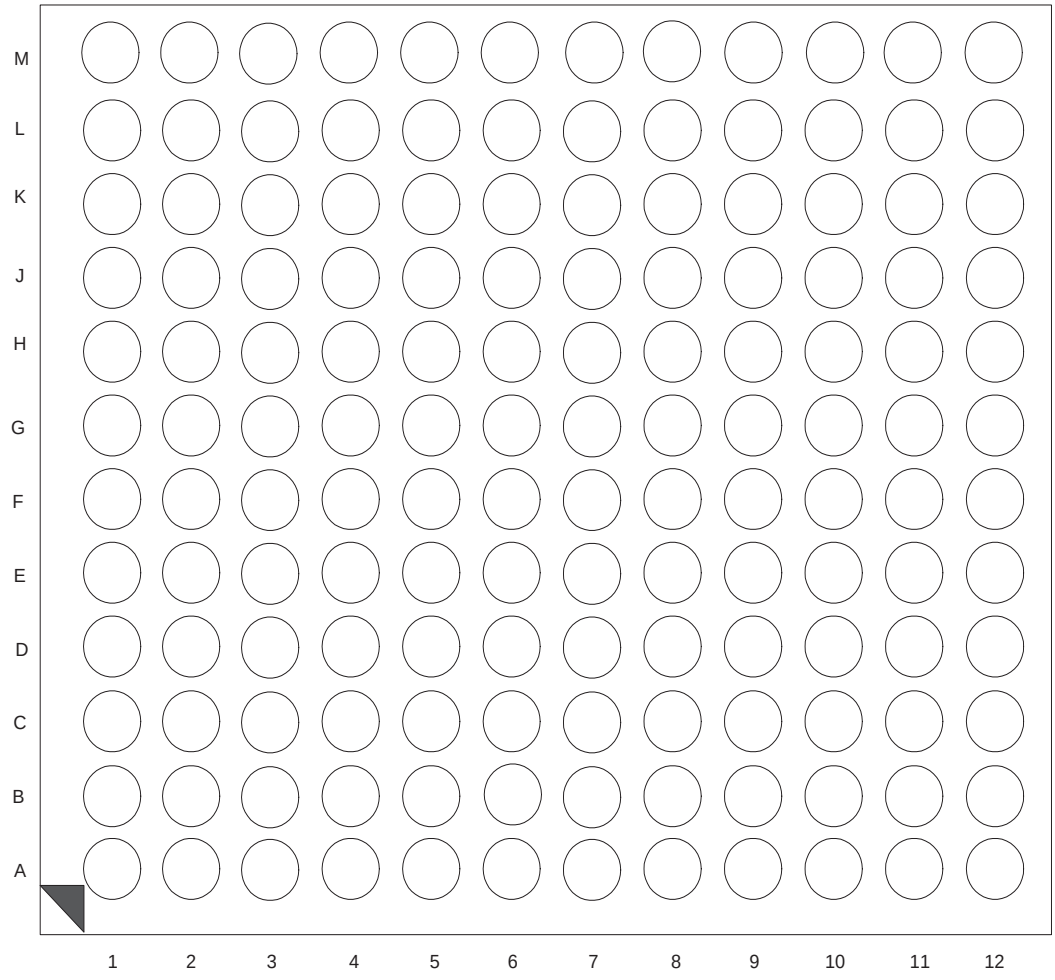
LE79112 VCP INTERNAL BLOCK DIAGRAM



CONNECTION DIAGRAMS

Below is the pin diagram for the Le79112ADGC device. Refer to Table 1, on page 5 for the associated pin names.

Figure 1. 144-Pin BGA Connection Diagram

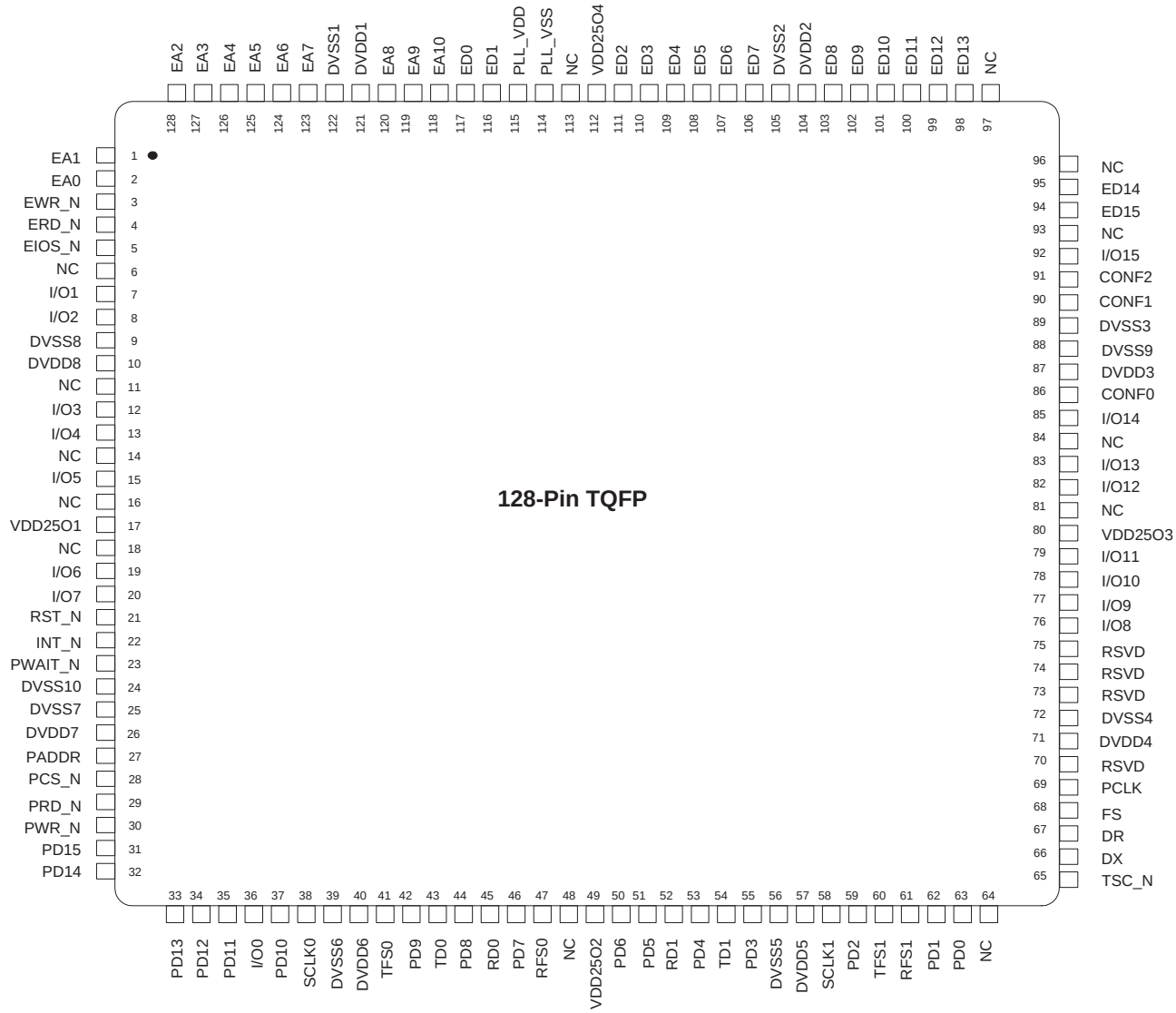


BOTTOM VIEW

Table 1. Le79112ADGC Assigned Pin Names and Numbers and Le79112AKVC Cross Reference

Pin Name	BGA Pin #	TQFP Pin #	Pin Name	BGA Pin #	TQFP Pin #	Pin Name	BGA Pin #	TQFP Pin #	Pin Name	BGA Pin #	TQFP Pin #	Pin Name	BGA Pin #	TQFP Pin #
$CONF_2$	L10	91	EA_6	A9	124	I/O_{15}	B2	92	NC	H1	—	$PD_2/I/O_8$	C2	59
$CONF_1$	L9	90	EA_5	A11	125	I/O_{14}	B1	85	NC	H12	—	$PD_1/I/O_7$	B3	62
$CONF_0$	B9	86	EA_4	B11	126	I/O_{13}	A2	83	NC	J1	—	$PD_0/I/O_6$	C1	63
DR	L7	67	EA_3	B12	127	I/O_{12}	C3	82	NC	J8	—	PLL_VDD	E5	115
$DVDD_1$	H7	121	EA_2	C12	128	I/O_{11}	B4	79	NC	J9	—	PLL_VSS	G5	114
$DVDD_2$	H8	104	EA_1	C11	1	I/O_{10}	C4	78	NC	J12	—	($\overline{PRD}$ or PRD/$\overline{WR}$)/ SI	J2	29
$DVDD_3$	G8	87	EA_0	D12	2	I/O_9	A3	77	NC	K7	—	$\overline{PWAIT}$/ I/O_{14}	H3	23
$DVDD_4$	G7	71	ED_{15}	D10	94	I/O_8	D5	76	NC	K9	—	($\overline{PWR}$ or $\overline{PDS}$)/SCK	K2	30
$DVDD_5$	E6	57	ED_{14}	D11	95	I/O_7	M4	20	NC	L6	—	RD1/MDIN	H4	52
$DVDD_6$	F6	40	ED_{13}	E9	98	I/O_6	K3	19	NC	L8	—	RD0/ MDIN2	L5	45
$DVDD_7$	F5	26	ED_{12}	E10	99	I/O_5	L3	15	NC	M8	—	RFS1	E8	61
$DVDD_8$	A8	10	ED_{11}	E11	100	I/O_4	M3	13	NC	M9	—	RFS0	M10	47
$DVDD_9$	K6	—	ED_{10}	E12	101	I/O_3	L2	12	NC	M11	—	$\overline{RST}$	L12	21
$DVSS_1$	H5	122	ED_9	F11	102	I/O_2	M2	8	PADDR/ I/O_{13}	H2	27	RSVD	J10	70
$DVSS_2$	F9	105	ED_8	F10	103	I/O_1	L1	7	PCLK	J6	69	RSVD	K10	74
$DVSS_3$	F8	89	ED_7	G11	106	I/O_0	K1	36	$\overline{PCS}/\overline{SS}$	J3	28	RSVD	K11	75
$DVSS_4$	F7	72	ED_6	F12	107	NC	A4	11	PD_{15}/ (I/O_{13} or I/O_5)	G3	31	RSVD	K12	—
$DVSS_5$	E7	56	ED_5	G10	108	NC	A5	16	PD_{14}/ (I/O_{12} or I/O_{15})	F3	32	RSVD	L11	73
$DVSS_6$	G6	39	ED_4	H11	109	NC	A6	84	$PD_{13}/I/O_{11}$	G2	33	SCLK1/ MDCLK	K5	58
$DVSS_7$	M1	25	ED_3	G12	110	NC	A7	14	$PD_{12}/I/O_{10}$	F2	34	SCLK0/ MDCLK2	J5	38
$DVSS_8$	M12	9	ED_2	H10	111	NC	B5	48	$PD_{11}/I/O_9$	E3	35	TD1/ MDOUT	M5	54
$DVSS_9$	A1	88	ED_1	H9	116	NC	B6	64	$PD_{10}/I/O_8$	F1	37	TD0/ MDOUT2	M6	43
$DVSS_{10}$	A12	24	ED_0	J11	117	NC	B7	93	$PD_9/I/O_7$	E2	42	TFS1/$\overline{MCS}$	D9	60
$DVSS_{11}$	G4	—	$\overline{EIOS}$	K4	5	NC	B8	81	$PD_8/I/O_6$	E4	44	$\overline{TFS0}$/ $\overline{MCS2}$	M7	41
DX	H6	66	$\overline{ERD}$	L4	4	NC	C5	96	PD_7/SO	E1	46	$\overline{TSC}$	D8	65
EA_{10}	A10	118	$\overline{EWR}$	J4	3	NC	C7	18	$PD_6/I/O_{12}$	D2	50	$VDD25O_1$	D6	17
EA_9	C10	119	FS	K8	68	NC	C8	97	$PD_5/I/O_{11}$	D3	51	$VDD25O_2$	F4	49
EA_8	C9	120	$\overline{INT}$	C6	22	NC	D7	6	$PD_4/I/O_{10}$	D4	53	$VDD25O_3$	G9	80
EA_7	B10	123				NC	G1	113	$PD_3/I/O_9$	D1	55	$VDD25O_4$	J7	112

Figure 2. Le79112AVC 128-Pin TQFP Package



PIN DESCRIPTIONS

Note:

Pads are not 5-V tolerant. Do not exceed 3.3 V.

Table 2. Le79112 VCP Device Pin Descriptions

Pin Name	Type	Description
$\overline{RST}$	Input	Active-low reset.
$CONF_2$-$CONF_0$	Input	Le79112 configuration pins that determine serial or parallel modes (8-bit, 16-bit, separate read and write strobes, data strobe and combined read/write strobe). See Table 3, on page 8 for configuration assignments.
$\overline{PCS}/\overline{SS}$	Input	Parallel interface: active-low chip select. Serial interface: active-low slave select.
($\overline{PRD}$ or PRD/$\overline{WR}$)/ SI	Input	Parallel interface: active-low read strobe or combined active-high read strobe/active-low write strobe. Serial interface: data input.
($\overline{PWR}$ or $\overline{PDS}$)/SCK	Input	Parallel interface: active-low write strobe or active-low data strobe. Serial interface: data clock.
PD_{15}/ (I/O_{13} or I/O_5)	Input/ Output	16-bit parallel interface: bi-directional data bit 15. 8-bit parallel interface: general purpose I/O bit 13. Serial interface: general purpose I/O bit 5.
PD_{14}/ (I/O_{12} or I/O_{15})	Input/ Output	16-bit parallel interface: bi-directional data bit 14. 8-bit parallel interface: general purpose I/O bit 12. Serial interface: general purpose I/O bit 15.
PD_{13}-PD_8/ I/O_{11}-I/O_6	Input/ Output	16-bit parallel interface: bi-directional data bits 13 through 8. 8-bit parallel interface: general purpose I/O bits 11 through 6. Serial interface: reserved.
PD_7/SO	Input/ Output	Parallel interface: bi-directional data bit 7. Serial interface: data output.
PD_6-PD_0/ I/O_{12}-I/O_6	Input/ Output	Parallel interface: bi-directional data bits 6 through 0. Serial interface: general purpose I/O bits 12 through 6.
$\overline{PWAIT}$/ I/O_{14}	Ouput	Parallel interface: programmable active-low or active-high signal to extend the current access cycle. $\overline{PWAIT}$ should be connected to a resistor pulled to the inactive state. Serial interface: general purpose I/O bit 14.
PADDR/ I/O_{13}	Input/ Output	Parallel interface: signal to indicate the start of a command sequence. Serial interface: general purpose I/O bit 13.
DR	Input	PCM receive data is input serially through the DR port. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate.
DX	Output	PCM transmit data is transmitted serially through the DX port. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DX is in the high-impedance state between bursts and while the device is in the inactive mode.
FS	Input/ Output	PCM Frame Sync. This 8-kHz pulse identifies the beginning of a frame. The Le79112 references individual timeslots with respect to this input, which must be synchronized to PCLK. See PCLKSEL[FSCFG] register for programming options. Input: FS is driven by the host (default, PCLKSEL[FSCFG] = 00). Output: FS is driven by Le79112 (PCLKSEL[FSCFG] = 11).
PCLK	Input	PCM Clock which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any integer multiple of 512 kHz up to 16.384 MHz. PCLK is also the chip clock.
$\overline{TSC}$	Output	$\overline{TSC}$ is active low when PCM data is output on the DX pin. This output is open-drain and is normally inactive (high impedance); it should be connected to a pull-up resistor.
$\overline{INT}$	Output	Active low Le79112 device interrupt output.
I/O_{15}–I/O_0	Input/ Output	General purpose, TTL-threshold compatible, logic input/output pins. When configured as an input, I/O_i transitions can cause interrupts to the DSP.
$\overline{TFS0}$/ $\overline{MCS2}$	Input/ Output	SPORT0: serial port transmitter frame sync. Master MPI2: chip select (output only).
SCLK0/ MDCLK2	Input/ Output	SPORT0: serial port data clock. Master MPI2: clock (output only).
TD0/ MDOUT2	Output	SPORT0: serial port transmit data. Master MPI2: data output.

Table 2. Le79112 VCP Device Pin Descriptions (Continued)

Pin Name	Type	Description
RD0/MDIN2	Input	SPORT0: serial port receive data. Master MPI2: receive data.
RFS0	Input/ Output	SPORT0: serial port receive frame sync.
TFS1/$\overline{MCS}$	Input/ Output	SPORT1: serial port transmit frame sync. Master MPI: chip select (output only). $\overline{MCS}$ is an active-low signal which enables serial data transmission into or out of the data ports of the Legerity SLAC device.
SCLK1/ MDCLK	Input/ Output	SPORT1: serial port data clock. Master MPI: data clock (output only). MDCLK determines the rate at which MPI data is serially shifted into or out of the data ports of the Legerity SLAC device.
TD1/ MDOUT	Output	SPORT1: serial port transmit data. Master MPI: data output. MDOUT is shifted out, MSB first, at the MDCLK rate into the DIN port of the Legerity SLAC device.
RD1/MDIN	Input	SPORT1: serial port receive data. Master MPI: data input. MDIN is shifted in, MSB first, at the MDCLK rate from the DOUT port of the Legerity SLAC device.
RFS1	Input/ Output	SPORT1: serial port receive frame sync.
EA_{10}-EA_0	Output	DSP expansion port address bus.
ED_{15}-ED_0	Input/ Output	DSP expansion port bi-directional data bus.
$\overline{EIOS}$	Output	DSP expansion port active-low chip select.
$\overline{ERD}$	Output	DSP expansion port active-low read.
$\overline{EWR}$	Output	DSP expansion port active-low write.
PLL_VDD	Power	+3.3 VDC supply to the PLL circuitry.
PLL_VSS	Power	PLL circuitry ground return.
$DVDD_1$– $DVDD_{8/9}$	Supply	+3.3 VDC digital supplies. Number of pins vary by package type.
$DVSS_1$– $DVSS_{9/11}$	Supply	Digital ground returns. Number of pins vary by package type.
$VDD25O_1$ - $VDD25O_4$	Supply	External filter connection points for the internal 2.5 VDC regulator. These pins must be tied together and filtered, see Figure 27, on page 39 for proper configuration. The 2.5 V regulator is for internal use only, do not use as a 2.5 V supply for other devices.
NC	–	No connect. These pins are not internally connected.
RSVD	–	Reserved. These pins are internally connected. Pins must be left floating.

Table 3. Configuration assignments ($CONF_2$ - $CONF_0$)

$CONF_2$ - $CONF_0$	Host Interface	Parallel Data Width	Parallel Read/Write Strobes
000	Parallel	8	Combined
001	Parallel	8	Separate
010	Parallel	16	Combined
011	Parallel	16	Separate
100	Serial	NA	NA
101	Reserved		
110			
111			

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–60ºC ≤ T_A ≤ +125ºC
Ambient Temperature, under Bias	–40ºC ≤ T_A ≤ +85ºC
Ambient relative humidity (non condensing)	5 to 95%
PLL_VDD with respect to PLL_VSS or DVSS	–0.4 to + 4.0 V
DVDD with respect to PLL_VSS or DVSS	–0.4 to + 4.0 V
PLL_VDD with respect to DVDD	±0.4V
PLL_VSS	DVSS ± 0.4 V
Latch up immunity (any pin)	±100 mA
Any other pin with respect to DVSS	–0.4 V to (DVDD + 0.4)
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Operating Ranges

Legerity guarantees the performance of this device over commercial (0º to 70ºC) and industrial (–40º to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40 to +85ºC
Ambient Relative Humidity	15 to 85%

Electrical Ranges

PLL_VDD	+3.3 V ± 5%, DVDD ± 50 mV
DVDD	+3.3 V ± 5%
DVSS	0 V
AVSS, PLL_VSS	DVSS ±10 mV
Digital pins with respect to DVSS	DVSS to +3.465V

DC Specifications

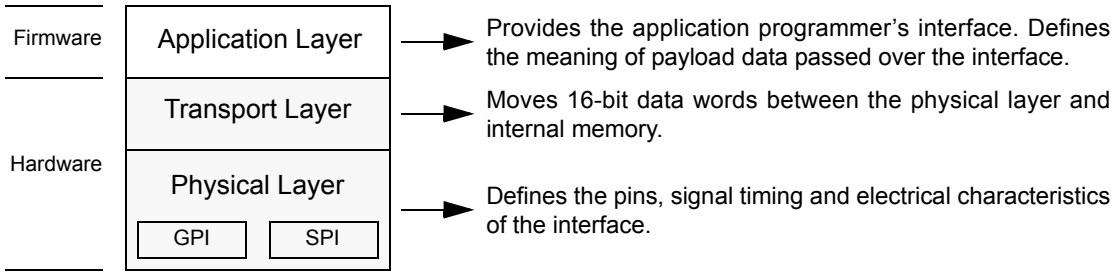
No.	Item	Condition	Min	Typ	Max	Unit
1	Input Low Voltage		–0.5	—	0.8	V
2	Input High Voltage		2.0	—	3.465	
3	Input Leakage Current	0 to DVDD	–10	—	+10	µA
4	Input hysteresis		0.15	0.225	0.3	V
6	Output Low Voltage	Iol = 8 mA	—	—	0.4	
7	Output High Voltage	Ioh = 400 µA	DVDD –0.4	—	—	
8	Power Dissipation		330	—	495	mW

HOST BUS INTERFACE (HBI) OVERVIEW

The Host Bus Interface provides a means for exchanging control, configuration and status information with an external host processor. This is accomplished by allowing the host to access regions of the DSP memory, and selected hardware registers on the internal bus. Essentially, the host peeks and pokes internal memory to exchange data.

This interface is implemented through a combination of hardware and firmware. The design is layered as shown in Figure 3. Hardware provides a generic means for transporting data between the host and internal memory. The interpretation of the data is provided by firmware running on the DSP. This layered architecture allows the definition of the application level interface to change by modifying the DSP firmware.

Figure 3. Host Bus Interface Layers



Physical Layer

The physical layer provides the functionality needed to electrically interface with a host processor. It defines the pins, signal timing and electrical characteristics of the interface. Two physical interfaces are provided. The General Purpose Parallel Interface (GPI) implements an 8-bit or 16-bit wide parallel interface. The Serial Peripheral Interface (SPI) implements a 3-wire or 4-wire synchronous serial slave interface.

Transport Layer

The transport layer moves 16-bit data words between the physical interface and internal DSP memory or hardware registers on the internal bus. It defines the structure of a transport frame, which consists of a 16-bit command word followed by 0 or more 16-bit payload data words. It also defines the interface address model, and provides mapping between interface and internal addresses.

Application Layer

The application layer defines the programmer's interface, and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the programmer's interface can change by providing new software.

PHYSICAL LAYER

The physical layer will provide both parallel and synchronous serial interfaces. These are described in the following sections.

General Purpose Parallel Interface (GPI)

The General Purpose Parallel Interface provides an external parallel interface used to communicate control information with a host processor. The GPI has several configuration options and has been architected to connect gluelessly to a variety of host

processors. The GPI interface uses a combination of write, read, data, address and wait strobes; thus, a dedicated clock is not needed to synchronize transfers.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface is a common 3-wire or 4-wire synchronous serial interface included with many DSPs and microcontrollers. The HBI includes a slave SPI implementation, which means the serial clock is supplied by an external master. The slave SPI includes support for 8-bit or 16-bit masters, and for masters that independently control chip select.

TRANSPORT LAYER

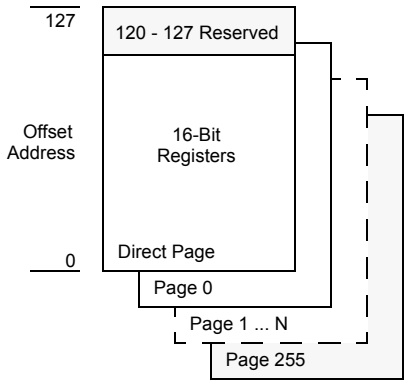
The primary responsibility of the transport layer is to move 16-bit data words between the physical interface and locations on the internal bus, which includes DSP memory. Data is organized into transport frames, which consist of a 16-bit command word followed by 0 or more data words. The command word provides address and length information to the transport hardware. In a sense, this hardware provides an internal DMA-like function, moving data over the internal bus under host control. Both the GPI and SPI physical layers share a common transport layer.

Interface Addressing

The transport command word provides address information to the interface hardware.

The host interface address model is based on a paged memory scheme as shown in Figure 4. The command design permits up to 257 pages, with up to 128 offset-addressable 16-bit wide register locations. Therefore, an interface address is composed of an 8-bit page number and a 7-bit register offset. Pages are selected by using a command to write the page register. All data access commands operate on the selected page. One exception is the direct page, which can be accessed at any time without changing the page register.

Figure 4. Host Bus Interface Address Model



Note:
1. Page 255 is reserved for loading code.

Command Structure

All transport frames start with a 16-bit command word followed by 0 or more 16-bit data words. The same command format is used for both the GPI and the SPI. Table 4, on page 12 provides a list of transport commands. Following is a short description of each command.

Table 4. Host Bus Interface Transport Commands

Transport Command	Command Bit Position								Number of 16-bit Data Words
	15	14	13	12	11	10	9	8	
	7	6	5	4	3	2	1	0	
Paged Offset Access	0	Offset Address (0 - 127)							Length + 1
	r/w[a]	Length (0 - 127)							
Direct Offset Access	1	Offset Address[b] (0 - 119)							Length + 1
	r/w[a.]	Length[b.](0 - 119)							
Start Mailbox Access	1	1	1	1	1	0	0	r/w[a.]	Length + 1
	Length (0 - 255)								
Configure Interface	1	1	1	1	1	1	0	1	0
	Interface Option Bits								
Select Page	1	1	1	1	1	1	1	0	0
	Page Number (0 - 255)								
NOP	1	1	1	1	1	1	1	1	0
	1	1	1	1	1	1	1	1	

a. Read/Write select bit. 0 = Read. 1 = Write.
b. Addresses 120 - 127 on the Direct Page are reserved.

Paged Offset Access

This command accesses one or more contiguous 16-bit registers on the currently selected page. The 7-bit offset specifies the starting address on the page. The command is followed by (Length + 1) 16-bit data words. The 7-bit Length field allows accessing between 1 and 128 locations with a single transport frame. For nonzero Lengths, the address automatically increments, and consecutive locations are accessed.

Direct Offset Access

The same as Paged Offset Access, except that the direct page is the target. By using this command, the direct page can be accessed at any time without modifying the page register.

Start Mailbox Access

This command accesses a contiguous stream of 16-bit data words starting from offset 0 on the currently selected page. The command is followed by (Length + 1) 16-bit data words. The 8-bit Length field allows accessing between 1 and 256 locations (i.e. up to 512 bytes) with a single transport frame. Access always begins from offset 0, and the address automatically increments.

Configure Interface

This command is used to configure various physical interface options. It is a write only command and is followed by 0 data words. The Interface Option Bits field allows the following features to be programmed by the host: Wait Pin Polarity (active High or active Low), Wait Pin Enable (default is tri-state), Wait Pin Drive Mode (open-source/open-drain or TTL), Interrupt Pin Drive Mode (open-drain or TTL), Endian Control (Big or Little), and Pad Slew Rate Control (for the general purpose I/O pins).

Select Page

This command selects the active interface page. It is a write only command and is followed by 0 data words. The 8-bit page field allows up to 256 selectable pages to be defined.

NOP

A command is reserved to serve as a NOP. Note that all commands except for the Offset Access commands are implemented by reserving an address from the direct page.

Associated Registers

There are several registers used by the HBI. These registers are listed below.

Mailbox Offset Register

This register is automatically updated by the hardware and contains the incremented address offset used for any non-direct access by the host. The host has the ability to read and write this register allowing different page accesses to be interleaved (if desired).

Note:

A mailbox access may be partitioned into smaller blocks, but a particular command must be completed before performing another command or switching to another mailbox. If the host is not interleaving the page accesses, then the host would not need to use the Mailbox Offset register.

Table 5. Mailbox Offset Register

	D15	D14	D13	D12	D11	D10	D9	D8
Data Byte	RSVD							

	D7	D6	D5	D4	D3	D2	D1	D0
Data Byte	r/w	Offset Address (0-127)						

Mailbox Flag Register

This register is used to communicate the handshaking control flags between the DSP and the host. There is one flag for each mailbox in the system.

Table 6. Mailbox Flag Register

	D15	D14	D13	D12	D11	D10	D9	D8
Data Byte	MBOX_FLAG[15:8]							

	D7	D6	D5	D4	D3	D2	D1	D0
Data Byte	MBOX_FLAG[7:0]							

MBOX_FLAG[15:0]: Mailbox flags. These bits will be allocated for downstream or upstream handshaking in order to determine whether the host or the DSP owns a particular mailbox at any given point in time.

CODE LOADING

The VCP device will always come up in boot mode during a power-on reset or when the reset pin of the chip is deasserted. The DSP will hold off program execution until the boot sequence is completed by the host via the SPI or GPI interface. The enabling or disabling of the boot operation during a hardware reset command is controlled by the boot sequence register bit in the Hardware Reset register. If the boot sequence is disabled when the hardware reset command is issued, the DSP immediately starts program execution without any boot operation.

Host Boot Procedure

The download code will be composed of a sequence of bytes that must be presented to the device via the GPI/SPI. These images can be broken up at 128-byte boundaries if needed. The first byte of the sequence (or after a break in the sequence of 128 blocks) must have the PADDR signal asserted. After all the images are loaded, the Code Checksum register should return AA55h.

APPLICATION LAYER

The application layer defines the programmer’s interface and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the programmer’s interface can change by providing new software. The primary elements of the model are system registers, mailbox buffers and an event queue. The following sections describe these elements in more detail.

SYSTEM REGISTERS

VCP Hardware Register Summary

Table 7 provides an overview listing of the hardware derived registers.

Table 7. VoiceEdge™ VCP Hardware Derived Register Space

Register Name	Register Description	Page	Offset	Length (Words)
INTIND	Used by **`VpGetEvent()`** to get the next event from the queue.	Direct	0x00	1
INTPARAM	Used by **`VpGetEvent()`** to get the next event's parameter.	Direct	0x01	1
MBFLAG	Used by the VCP firmware and VP-API to provide mailbox handshaking.	Direct	0x02	1
CodeChecksum	CRC of Boot Load data. A valid load should always produce a 0xAA55 value.	Direct	0x03	1
BASE255	Used for Boot Load.	Direct	0x04	1
MBOFFSET	Allows for interleaved mailbox accesses. Not used by the VoiceEdge API.	Direct	0x05	1
HWRES	Hardware Reset Register. Used by **`VpBootLoad()`**	Direct	0x06	1
CLKSEL	PCLK Select Register: VCP defaults to autodetect the PCLK rate.	Direct	0x07	1
PCMCLKSLT	VCP defaults to 0 clockslot offset for both TX and RX.	Direct	0x08	1
INTSTAT	System Interrupt (fault) status.	Direct	0x09	1
INTMASK	System Interrupt (fault) mask.	Direct	0x0A	1
PGSEL	HBI page selection.	Direct	0xFE	1
PINCONFIG	HBI User Interface pin configuration.	Direct	0xFD	1

System (Hardware) Registers

This section details each of the VoiceEdge VCP registers provided by the hardware (as opposed to firmware derived registers). These registers are provided for debugging purposes only. The VP-API has corresponding definitions for their addresses (and bit definitions) and knows how to read/write these registers.

Note:

In all registers, "RSVD" should be written 0 and reads as indeterminate, unless otherwise indicated.

Interrupt Indication (INTIND) **Direct page address 0x00 (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT_SRC	INT_IND[14:8]						
INT_IND[7:0]							

This register reports the source information for the current interrupt. It returns 0x0000 if there is no active interrupt. Reading this register clears the associated interrupt and loads the INTPARAM register with the associated parameter. In most cases the host should read the INTPARAM register after reading this register. This can be accomplished with one multi-word read, since the INTPARAM register immediately follows the INTIND register.

INT_SRC Interrupt source bit.

0: Event queue.
1: System interrupt register.

INT_IND[14:0] Interrupt indication field. The contents of this field depend on the interrupt source bit. If the INT_SRC indicates a system interrupt, each subsequent bit indicates a transition on the corresponding system interrupt status register bit (refer to the SYSINTSTAT register for details). Only unmasked system interrupts will appear in this manner.

Interrupt Parameter (INTPARAM) **Direct page address 0x01 (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT_PARAM[15:8]							
INT_PARAM[7:0]							

This register returns the parameter for the last interrupt read from the INTIND register. It is updated whenever the INTIND register is read. Reading this register does not change the state of the interrupt hardware.

INT_PARAM[15:0] Interrupt parameter field. The meaning of this field depends on the associated interrupt. System interrupts will mirror the system interrupt status (SYSINTSTAT) register at the time the INTIND read occurred.

Mailbox Flag (MBFLAG) **Direct page address 0x02 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSP_FLAG	CMD_FLG

This register indicates access rights to the VCP's command and response mailboxes. A zero in any of these bits indicates that the host has access to the corresponding mailbox. The register is a write 1 to clear so the host transfers mailbox control by writing a 1 to the bit which corresponds to the mailbox to which the host is relinquishing control. Note that the host and the VCP can only relinquish control of a mailbox. Neither can request control and it is therefore important that both relinquish control in a reasonably expedient manner.

CMD_FLAG The host sets the Command Mailbox flag by writing a 1 to the associated bit. Writing a 0 to any bit has no affect.

0: Host owns associated mailbox.
1: DSP owns associated mailbox.

RSP_FLAG The host sets the Response Mailbox flag by writing a 1 to the associated bit. Writing a 0 to any bit has no affect.

0: Host owns associated mailbox.
1: DSP owns associated mailbox.

Page 255 CRC (CodeChecksum) **Direct page address 0x03 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CHKSUM[15:8]							
CHKSUM[7:0]							

The register holds the checksum for any boot operation. The VCP firmware release images are constructed such that the final value of this register should be 0xAA55.

Page 255 Base Address (BASE255) **Direct page address 0x04 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	BASE_ADDR[17:11]						
BASE_ADDR[10:8]			RSVD				

This register is used for code booting. The API uses this register accordingly. The host software needs no further manipulation of this register.

BASE_ADDR[17:8] Internal address bits 17 - 8 for interface Page 255.

Mailbox Offset (MBOFFSET) **Direct page address 0x05 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD							
RSVD	MB_OFFSET[6:0]						

Mailbox Offset contains a pointer to the address of the next transaction into the current mailbox. This register allows interleaved access to a given mailbox. To implement interleaved access, the host must read this register prior to changing the active mailbox. After restoring the active mailbox the host must restore the Mailbox Offset to continue accesses from the previous position.

MB_OFFSET[6:0] Address of the next access to the currently selected mailbox.

Hardware Reset (HWRES) **Direct page address 0x06 (WO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MMAP	HWRES
RSVD	RSVD	RSVD	RSVD	RSVD	CLKNOCLR	MMAP	HWRES

This register allows the host to force a hardware reset.

MMAP: Specifies whether or not the VCP follows its usual boot sequence. Normally, during power-up, the VCP waits for a code load before starting the VCP firmware. This wait can be disabled to allow for a software reset that does not require performing another code load.

0: Enable the boot sequence after a hardware reset (code load expected before VCP code execution).
1: Disable the boot sequence after a hardware reset (VCP code execution occurs immediately upon reset, without waiting for code load).

CLKNOCLR: Do not reset PCLKSEL register with HWRES.

0: Reset PCLKSEL to default values with HWRES. (default)
1: Keep PCLKSEL values during HWRES.

HWRES: Hardware reset bit.

0: Normal operation.
1: Perform a hardware reset. This bit is self clearing.

Note:

Writing MMAP bit D9 and HWRES bit D8 is optional. Writing these bits is advisable if the PINCONFIG register is not properly set.

PCLK Selection (CLKSEL) **Direct page address 0x07 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FSCFG[1:0]	FSCFG[1:0]	AUTODET	CSEL[12]	CSEL[11]	CSEL[10]	CSEL[9]	CSEL[8]
CSEL[7]	CSEL[6]	CSEL[5]	CSEL[4]	CSEL[3]	CSEL[2]	CSEL[1]	CSEL[0]

CLKSEL is used to configure the VCP PLL, depending on the relationship between frame sync (FS) and PCLK.

FSCFG: Configure the source of the 8 KHz Frame Sync (FS).

00: FS is externally provided and is synchronous to PCLK.(default)
01: FS is externally provided and is asynchronous to PCLK.
10: FS is internally generated, any external FS is ignored.
11: FS is internally generated and driven as an output.

AUTODET: Auto detect PCLK frequency using FS reference.

0: Auto-detection disabled. CSEL[12:0] under user control.
1: Auto-detection enabled. CSEL[12:0] controlled by PCLK & FS. (default)

CSEL[12:0]: PCLK Frequency Select
When writing AUTODET = 1, the default is restored to these bits until the auto-detection is complete.

0000000111111: PCLK = 512kHz.
0000010111111: PCLK = 1.536MHz
0000011111111: PCLK = 2.048MHz.
0000111111111: PCLK = 4.096MHz.
0001111111111: PCLK = 8.192MHz.
0011111111111: PCLK = 16.384MHz.
1000100111111: PCLK = 35.328MHz ADSL clock
1001011111011: PCLK = 38.880MHz (default)

Using FS as an 8-kHz reference, the device will automatically select the correct CSEL[12:0] value based the current PCLK frequency. The initial CSEL[12:0] setting will be 1001011111011 (PCLK=38.880 MHz). If the FS or PCLK pulses are absent, the device will maintain CSEL[12:0] = 1001011111011 until it detects transitions on both the FS and PCLK inputs. Automatic frequency detection will occur after 9 consistent FS periods but can be overridden by clearing the AUTODET bit and writing CSEL[12:0] with the desired value. This can be accomplished in a single write.

PCM Transmit/Receive Clock Slot (PCMCLKSLT) **Direct page address 0x08 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RSVD	XE	RCS2	RCS1	RCS0	TCS2	TCS1	TCS0

This register is used to control the PCM interface clock slot.

XE Transmit changes bit.

0: Transmit changes on falling edge of PCLK (default)
1: Transmit changes on rising edge of PCLK

RCS Receive PCM clock slot delay number (default = 0).

TCS Transmit PCM clock slot delay number (default = 0).

System Interrupt Status (INTSTAT) **Direct page address 0x09 (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	EV_OV	WDT	CFAIL	RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

This register allows the host to determine the present status of the system faults. It differs from the INTPARAM register in that no interrupt is required to determine the system fault status.

EV_OV Event queue overflow detected. This bit indicates that an event was lost due to event queue overflow. If events are being serviced events and generated at the same time it is possible that this flag will be set multiple times. This bit will remain set until read.

WDT Watchdog timer timeout occurred.

CFAIL Clock failure occurred. At start-up, this bit clears 200 μsec after clocks auto-detected.

System Interrupt Mask (INTMASK) **Direct page address 0x0A (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$RSVD^{W0*}$	MEV_OV	MWDT	$RSVD^{W1*}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$
$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$	$RSVD^{W1}$

This register is used to mask system interrupt sources. There is a one to one correspondence between the bit definitions in INTMASK and INTIND when INTIND represents a system interrupt.

Mask Bits (Refer to INTSTAT register bit descriptions above.)

0: The corresponding interrupt is unmasked.
1: The corresponding interrupt is masked.

Note:
W0 = Write 0. W1 = Write 1.

HBI page selection (PGSEL) **Command 0xFE (W)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
PG_SEL [7:0]							

PG_SEL: Page addressed by any non-direct HBI access.

HBI user interface pin configuration (PINCONFIG) **Command 0xFD(W)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	INT_DRV	PWAIT_DRV	PWAIT_EN	PWAIT_POL	END_SEL

INT_DRV:	$\overline{\text{INT}}$ pin drive mode. 0: open drain (default). 1: TTL.
PWAIT_DRV:	PWAIT pin drive mode. 0: TTL (default). 1: open source or drain depending on polarity.
PWAIT_EN:	PWAIT pin enable. 0: disabled (default). 1: enabled.
PWAIT_POL:	PWAIT pin polarity. 0: active low (default). 1: active high.
END_SEL:	Endian select. 0: big endian (default). 1: little endian.

Software (Firmware Derived) Registers

The remainder of the registers defined in the HBI register space are firmware defined registers. For detailed information on these registers, refer to the *VoiceEdge API II Reference Guide for VCP Devices*.

Mailboxes Buffers

Mailbox buffers are composed of a dedicated interface page and an associated hardware semaphore (i.e. mailbox flag) to control ownership. Mailbox buffers pass information in one direction only. The host writes to a downstream mailbox and reads from an upstream mailbox. The reverse is true for the DSP. The flag indicates mailbox status and guards against race conditions.

All mailbox flags are located in a 16-bit mailbox flag register implemented in hardware. They exhibit the following characteristics. Only the host can set a mailbox flag. Likewise, only the DSP can clear a mailbox flag. High-to-low transitions generate a maskable interrupt towards the host. Low-to-high transitions generate a maskable interrupt towards the DSP.

The following steps illustrate how a mailbox is used to pass information in the downstream (i.e. host-to-DSP) direction. For an upstream exchange, roles are simply reversed.

1. The host waits for the appropriate mailbox flag to go low, indicating that the mailbox is now empty. To do this, the host can either poll the mailbox flag register, or unmask the associated interrupt and wait for an interrupt to be generated.
2. The host selects the mailbox by issuing a Select Page command.
3. The host writes data into the mailbox using either the Paged Offset or Mailbox Access commands. Data can be written with one command or with several. The first location of the mailbox is used to indicate the length of the data being passed to the DSP. The host is responsible for writing this length value.
4. When the host is finished writing data to the mailbox, it then sets the associated mailbox flag by writing a one to the appropriate bit in the mailbox flag register. This indicates to the DSP that data is waiting in the mailbox, and ownership has passed to the DSP.
5. The DSP either polls the mailbox flag register, or receives an interrupt indicating data is available.
6. The DSP reads and processes the contents of the mailbox taking any required actions. It reads the first location in the mailbox to determine the length of the data.
7. The DSP clears the associated mailbox flag, indicating to the host that it is finished processing and passing ownership back to the host.

Command/Response Mailboxes

This mailbox pair provides a channel for exchanging command and status messages with the host. Refer to the VP-API code for commands.

Event Queue

A key element of the host interface is an event queue. Events relay asynchronous information back to the host. Buffering events in a queue gives the host flexibility on when to read them, and ensures that no events are lost if the host is unable to service them immediately.

The host reads the event queue through the interrupt indication and parameter registers. Events are composed of a 16-bit indication value that includes channel and event type fields, and an optional 16-bit parameter. Several of the Le79112 VCP events require a 32-bit timestamp. The timestamp can be reduced to 16-bits by creating a timestamp rollover event, and letting the host maintain the upper 16-bits. An event reports the lower 16-bits of the timestamp in the parameter register.

GENERAL PURPOSE PARALLEL INTERFACE (GPI)

The General Purpose Parallel Interface (GPI) is an external interface of the VCP device that is used to communicate command information to/from an external host processor. The GPI has several configuration options and has been architected to connect gluelessly to a variety of external processors. The GPI interface uses a combination of write, read, data, address, and wait strobes; thus, a dedicated clock is not needed to synchronize the transfers. The structure of the commands and data both take the form of a command word followed by data in order to preserve the same logical view as the Serial Peripheral Interface (SPI). This allows the host to issue the same commands to a VCP device regardless of the physical interface.

GPI External Pin List

The pins related to the GPI are described below. Pins associated with clocks, reset, or interrupts are described in another section

Table 8. GPI Pins

Pin Name	Type	Reset	Description
$\overline{\text{PCS}}$	I		GPI Chip Select (active Low)
PADDR	I		GPI Address Pin (Command or Data Indicator)
$\overline{\text{PWAIT}}$	O/Z	Z	GPI Wait (active Low, programmable, external pull-inactive required)
PD[15:0] (PD[7:0])	I/O/Z	Z	GPI Data Bus. Alternate configuration as 8-bit Data Bus.
$\overline{\text{PRD}}$ ($\overline{\text{PDS}}$)	I		GPI Read Strobe (active Low). Alternate configuration as GPI Data Strobe (active Low)
$\overline{\text{PWR}}$ (PRD/$\overline{\text{WR}}$)	I		GPI Write Strobe (active Low). Alternate configuration as GPI Read/Write Strobe (Read=High, Write=Low)

GPI Features

The GPI has been designed to connect to a variety of external host processors. The capabilities of the GPI are enumerated below.

1. Commands and data can be transferred across the parallel interface using either separate read and write strobes or using a combined read/write strobe and a data strobe.
2. The GPI can be configured for either 8-bit or 16-bit data bus transfers.
3. A wait strobe can be used to indicate to the external processor that the interface is available for a transfer. When the wait strobe goes active, the interface is busy. The transfer will complete after the wait signal deasserts. The wait strobe pin polarity is programmable and defaults to tri-state. Note: an external pull-up or pull-down (depending on the programmed active state) is required.
4. Data byte swap allows the GPI to support big and little endian systems. (Note that the command is always evaluated as big endian, so little endian systems should byte swap the command word accordingly).
5. A read status register is available to the external processor by performing a read while the address pin is High. The contents of this register contains a wait status indication, which can be used by external processors that do not support the wait pin.

Parallel Interface Status (GPISTATUS) (R)

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	RSVD	RSVD	CMD_PROG	INT	PWAIT

Read GPISTATUS with PADDR high.
CMDPROG: Command in progress.
INT: $\overline{\text{INT}}$ logic state.
PWAIT: PWAIT logic state.

6. The address pin is used as a command word demarcation. The command interface is reset during a write operation when the address pin is High. (Note that the command interface is not reset during a read operation when the address pin is High.) This ensures that the command and data sequences between the external processor and the VCP device will be interpreted properly. Refer to Table 9 for a list of the GPI access modes.

Table 9. GPI Interface Access Types

Address	Read or $\overline{\text{Write}}$	Access Type
0	0	write data
0	1	read data
1	0	write command
1	1	read status

GPI Connections to an External Host

The external interface connection diagrams for two different GPI configurations is shown in Figure 5 and Figure 6.

Figure 5. GPI Connections Using Separate Read and Write Strobes

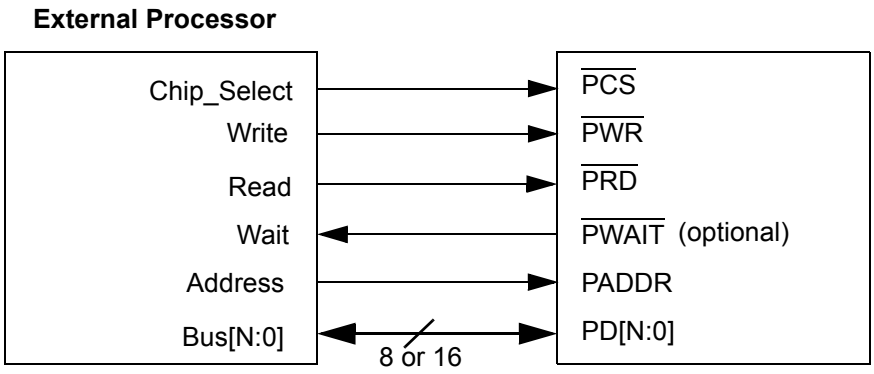
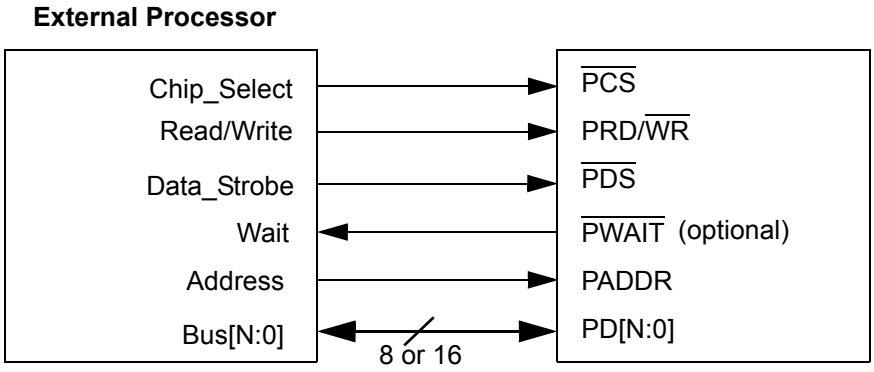


Figure 6. GPI Connections Using Combined Read/Write and Data Strobes



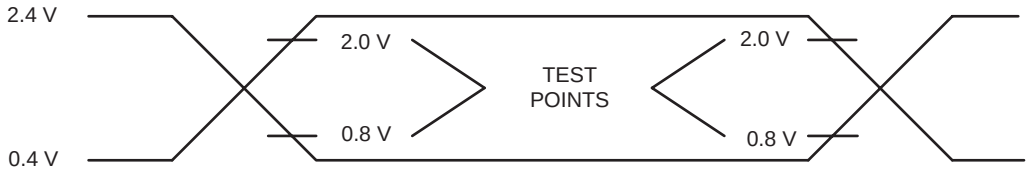
GPI Timing Requirements

The timing requirements for read and write accesses are shown in the following timing diagrams. The PWAIT waveform on the read diagrams is shown as a dotted line because the wait strobe feature is optional and would only go active if the read data was not yet valid following a read command. Also, although the wait strobe polarity is programmable, it is shown as active Low in several of the timing diagrams. Each write and read access is qualified by an active chip select signal. In some applications, the chip select pin could be tied Low. The 16-bit accesses using separate read and write strobes is shown in Figure 8 and Figure 9. The 8-bit accesses using separate read and write strobes are shown in Figure 10 and Figure 11. The timing information for the 8 and 16-bit figures using separate read and write strobes can be found in Table 10. The 8-bit accesses using a combined read/

write strobe and a data strobe is shown in Figure 12 and Figure 13. The timing information for the 8 and 16-bit figures using a combined read/write strobe and a data strobe can be found in Table 11. Refer to Figure 14 for an example of the read status register access (which applies to both 8 and 16-bit modes). It should be noted that if the host is using the wait pin feature and issues a read command, that performing a status read operation immediately after the writing of a read command and before the actual read of the first byte/word of data would cause the read status access to be extended. Refer to Figure 15 for an example of the byte swap operation on the data word (which also applies to 8 and 16-bit modes).

SWITCHING CHARACTERISTICS

Figure 7. Switching Characteristics



DVDD = PLL_VDD = 3.3 V ±5%, PLL_VSS = DVSS = 0 V.

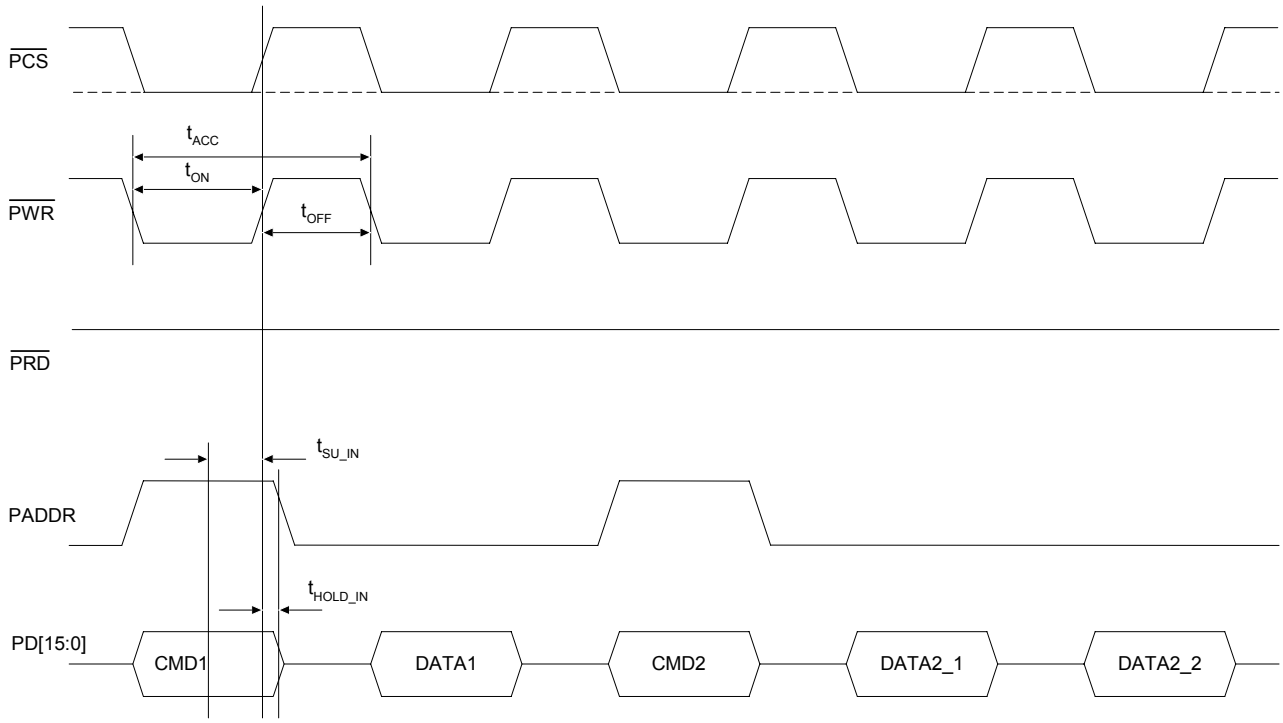
Table 10. GPI Bus Timing Parameters for Separate Read and Write Strobes.

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{ACC}	Access period (from Write to Write or Read to Read or Read to Write)	100	—	—	ns	
t_{ON}	Pulse width LOW ($\overline{PCS}$ or $\overline{PWR}$ or $\overline{PRD}$)	35	—	—		
t_{OFF}	Pulse width HIGH ($\overline{PCS}$ & $\overline{PWR}$ or $\overline{PCS}$ & $\overline{PRD}$)	10	—	—		
t_{WR_RDV}	Write to Read (rising $\overline{PWR}$ to Data output valid)	25	—	270		3
t_{RD_DV}	$\overline{PCS}$, PADDR, $\overline{PRD}$ active to Data output valid	—	—	25		3
t_{SU_IN}	Address, Data input setup time to rising $\overline{PCS}$ or $\overline{PWR}$	20	—	—		
t_{HOLD_IN}	Address, Data input hold time after rising $\overline{PWR}$ or $\overline{PCS}$	1	—	—		
t_{HOLD_OUT}	Data output hold time after rising $\overline{PRD}$ or $\overline{PCS}$	3	—	10		3
t_{CS_WAIT}	Chip Select active to Wait active	—	—	25		1,3
t_{WAIT}	Wait strobe width LOW when $\overline{PCS}$ is active	0	80	280		1,2,3
t_{WAIT_DV}	PWAIT deserted to Data valid	—	—	0		3

Notes:

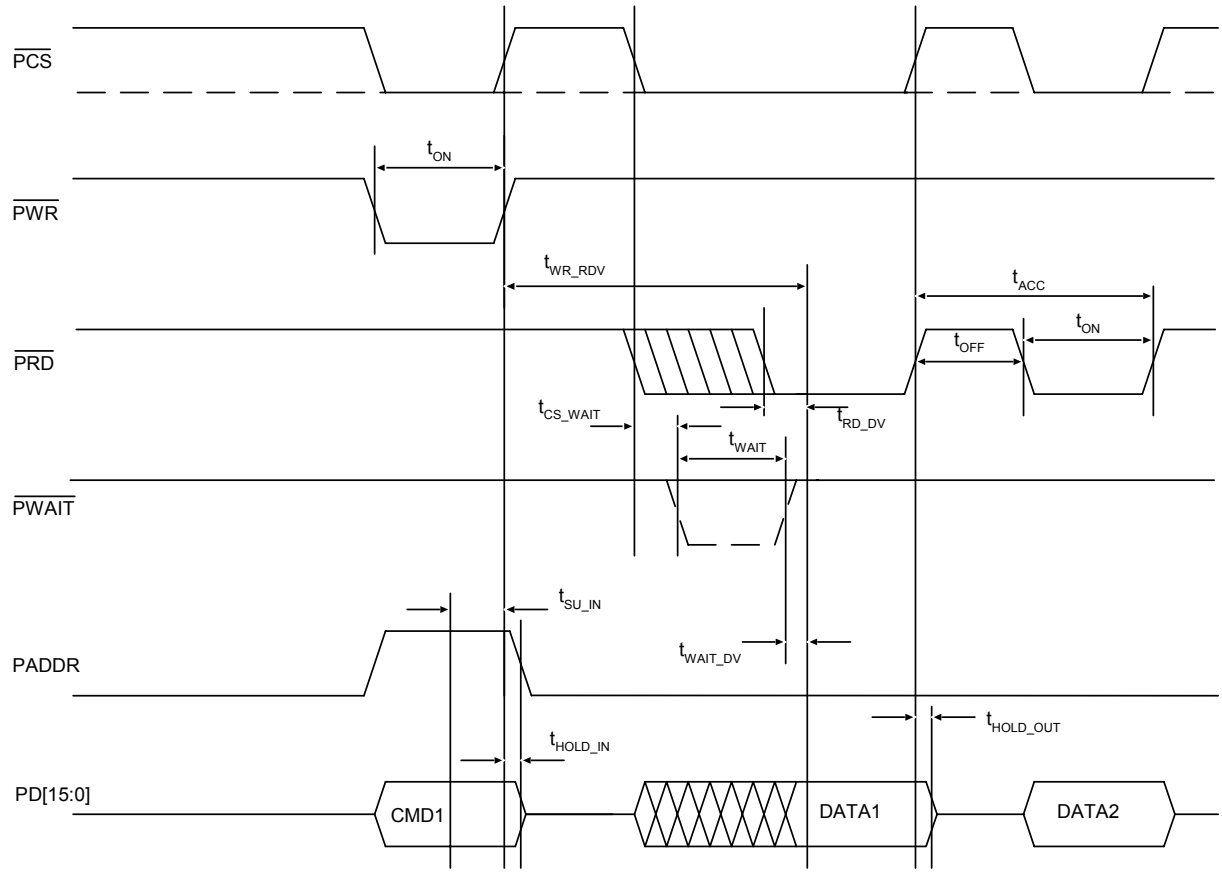
1. *The Wait Strobe active edge may occur as early as the rising Write Strobe signal if Chip Select is held active.*
2. *Before clocks are properly configured and stabilized, the maximum delay may be up to 400 ns.*
3. *C_{load} = 40 pF.*

Figure 8. GPI 16-Bit Write Access Using Separate Read and Write Strobes



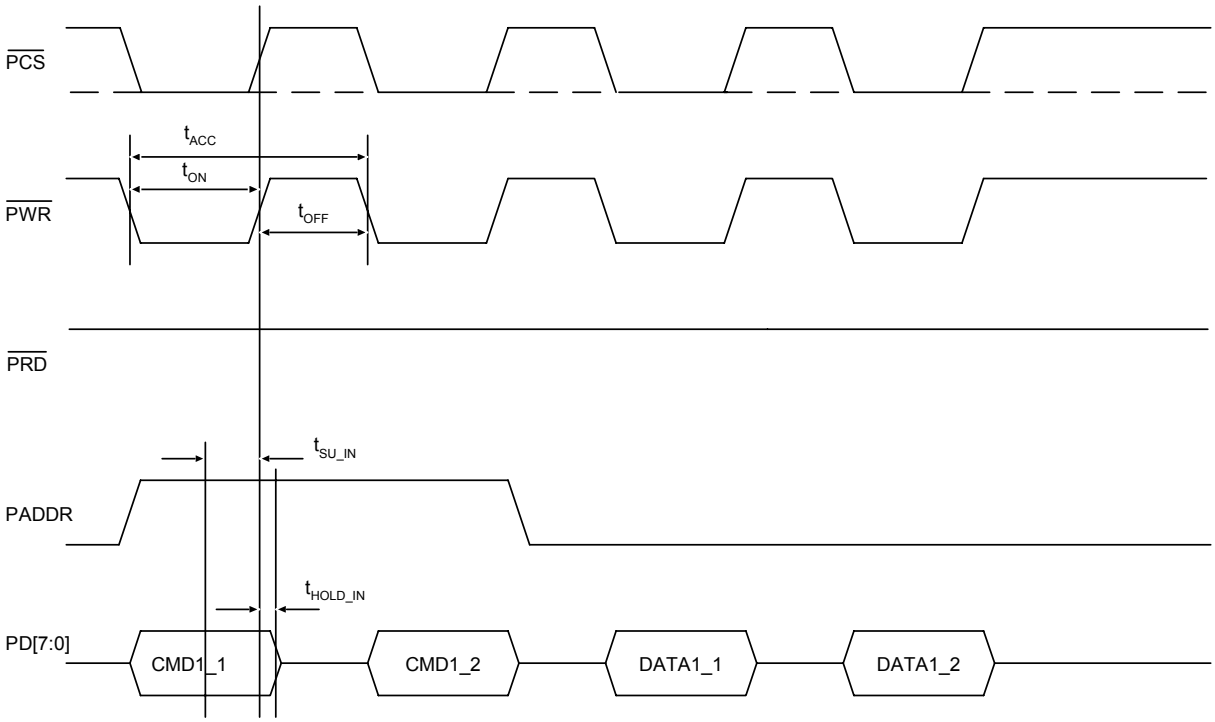
Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 9. GPI 16-Bit Read Access Using Separate Read and Write Strobes



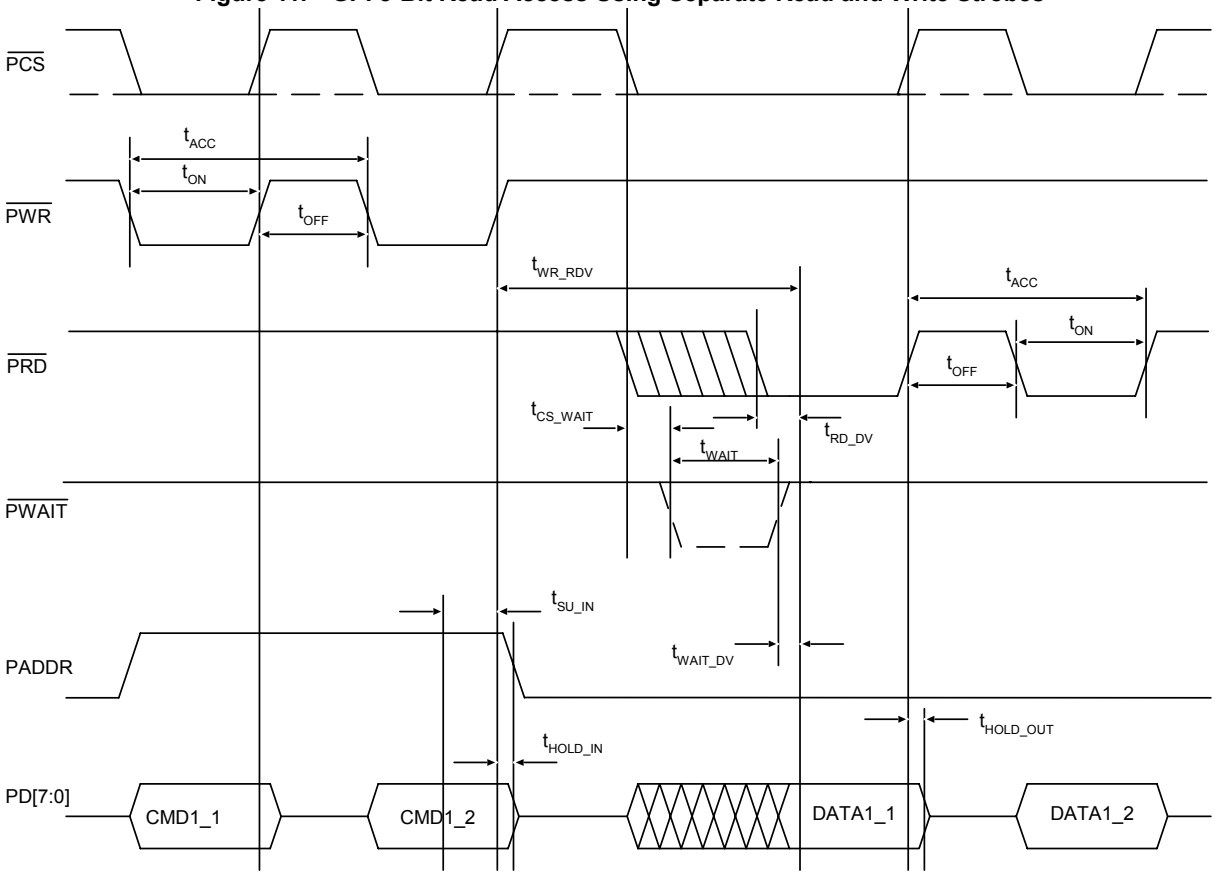
Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 10. GPI 8-Bit Write Access Using Separate Read and Write Strobes



Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 11. GPI 8-Bit Read Access Using Separate Read and Write Strobes



Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

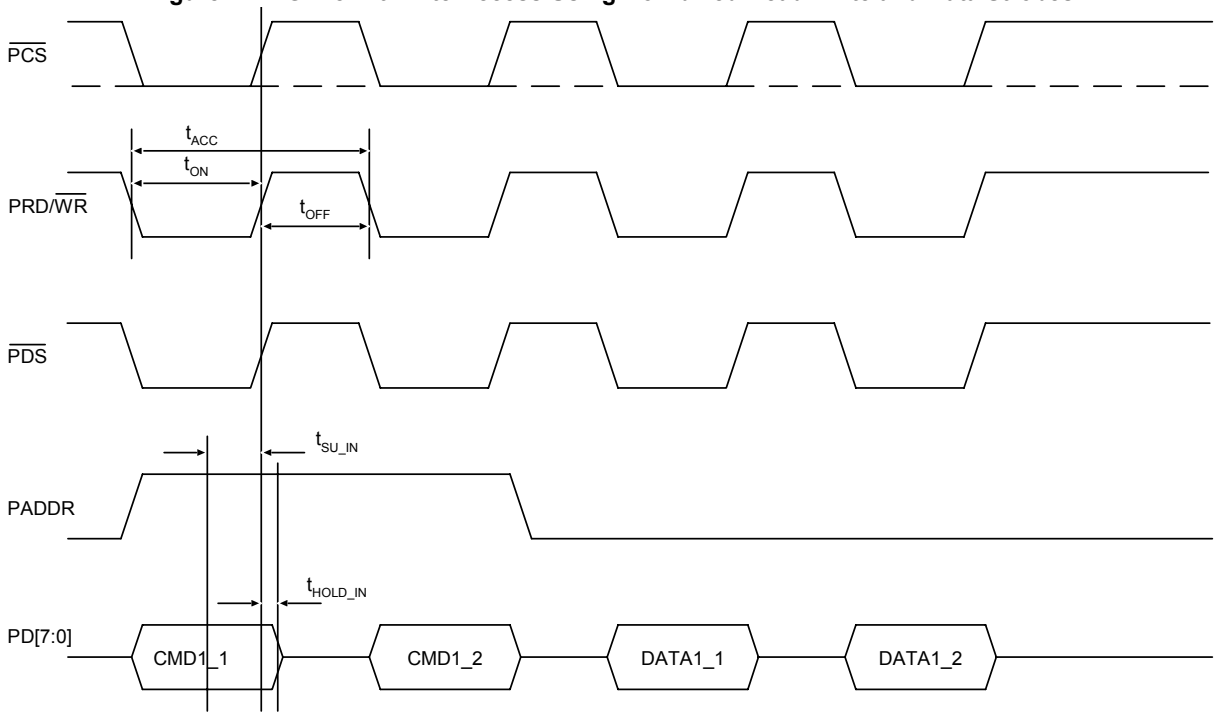
Table 11. GPI Bus Timing Parameters for Combined Read/Write and Data Strobes

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{ACC}	Access period (from Write to Write or Read to Read or Read to Write)	100	—	—	ns	
t_{ON}	Pulse width LOW ($\overline{PCS}$ or PRD/$\overline{WR}$ or $\overline{PDS}$)	35	—	—		
t_{OFF}	Pulse width HIGH ($\overline{PCS}$ & PRD/$\overline{WR}$ & $\overline{PDS}$ or $\overline{PCS}$ & $\overline{PDS}$)	10	—	—		
t_{WR_RDV}	Write to Read (rising PRD/$\overline{WR}$ to Data output valid)	25	—	270		3
t_{RD_DV}	$\overline{PCS}$, PADDR, PRD/$\overline{WR}$ active to Data output valid	—	—	25		3
t_{SU_IN}	Address, Data input setup time to rising $\overline{PCS}$ or PRD/$\overline{WR}$ or $\overline{PDS}$	20	—	—		
t_{HOLD_IN}	Address, Data input hold time after rising PRD/$\overline{WR}$ or $\overline{PDS}$ or $\overline{PCS}$	1	—	—		
t_{HOLD_OUT}	Data output hold time after rising $\overline{PDS}$ or $\overline{PCS}$	0	—	10		3
t_{CS_WAIT}	Chip Select active to Wait active	—	—	25		1,3
t_{WAIT}	Wait strobe width LOW when $\overline{PCS}$ is active	0	80	280		1,2,3
t_{WAIT_DV}	PWAIT deserted to Data valid	—	—	0		3

Note:

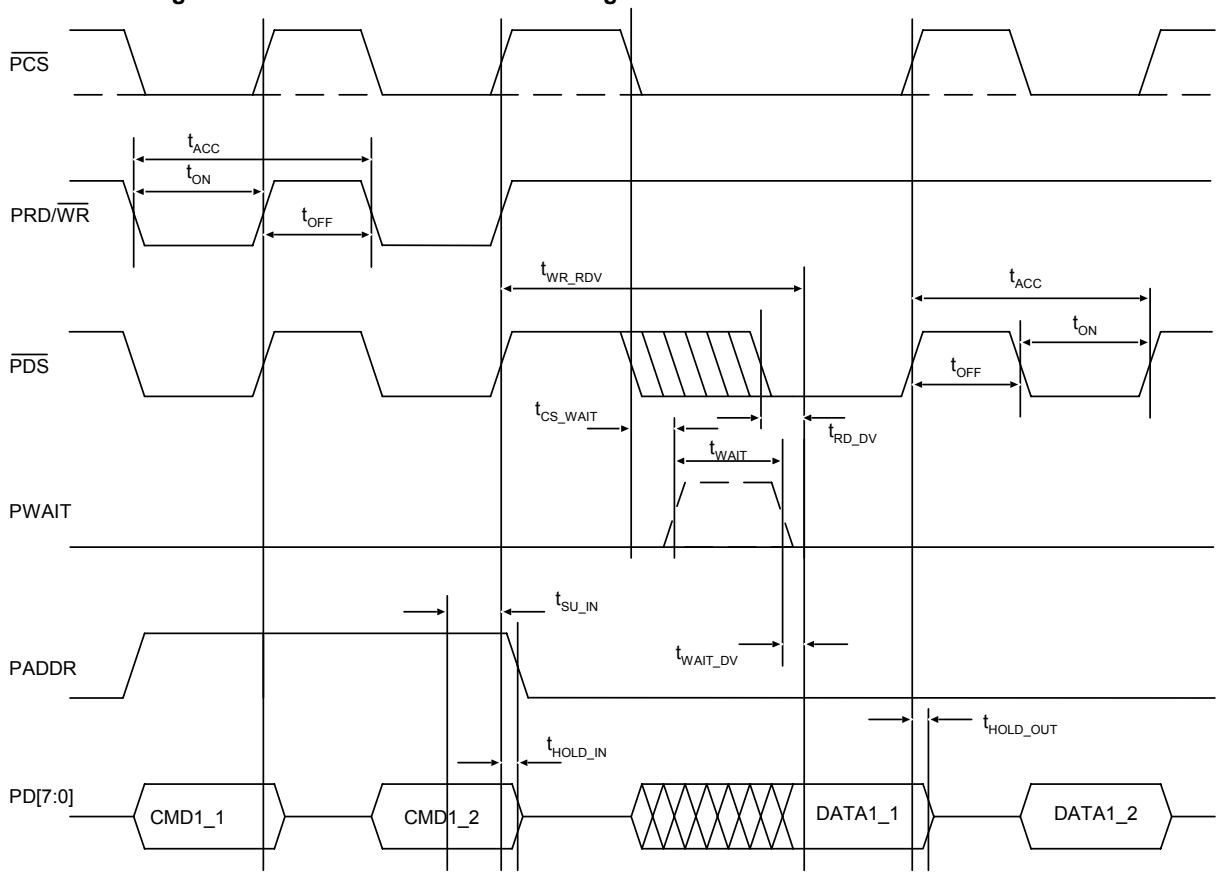
1. *The Wait Strobe active edge may occur as early as the rising Write Strobe signal if Chip Select is held active.*
2. *Before clocks are properly configured and stabilized, the maximum delay may be up to 400ns.*
3. *C_{load} = 40pF.*

Figure 12. GPI 8-Bit Write Access Using Combined Read/Write and Data Strobes



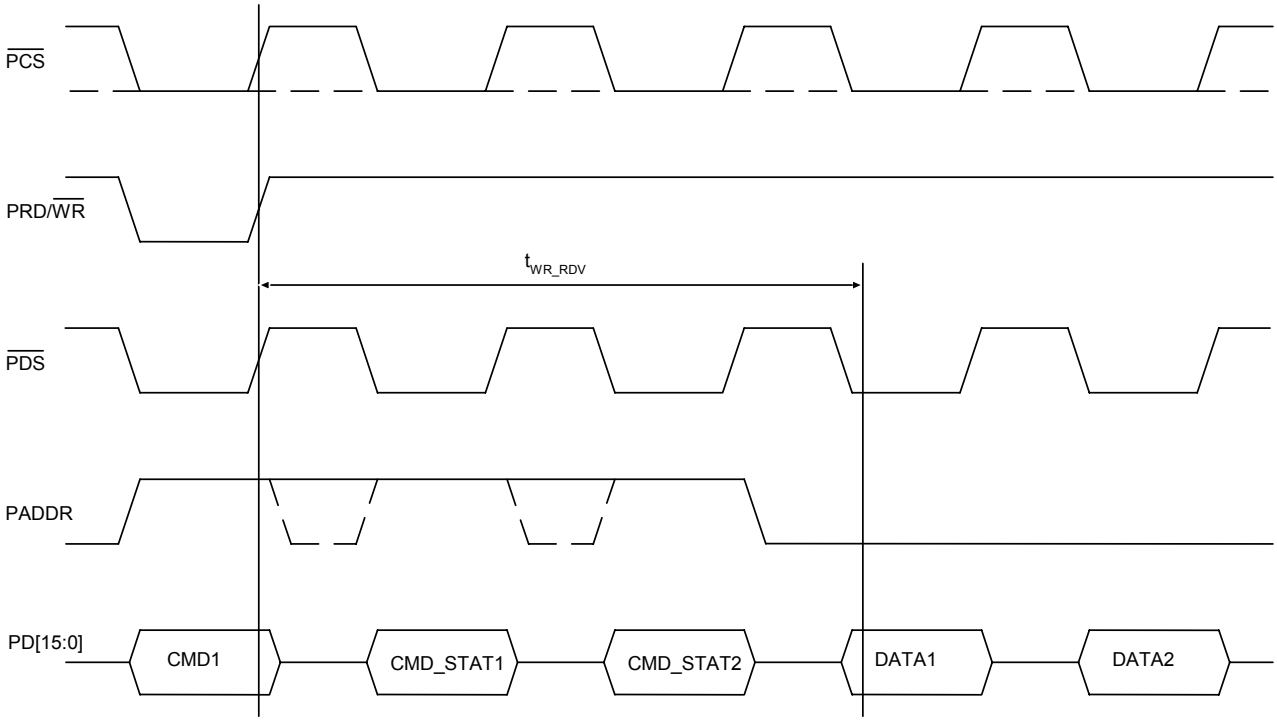
Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 13. GPI 8-Bit Read Access Using Combined Read/Write and Data Strobes



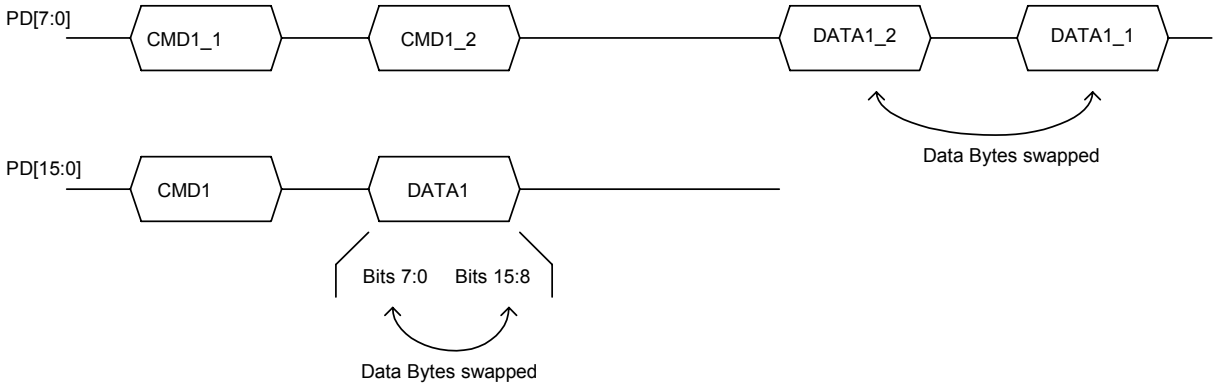
Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 14. GPI Read Status Register Access



Note: each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 15. GPI Data Byte Swap Access



SERIAL PERIPHERAL INTERFACE (SPI)

Serial Peripheral Interface (SPI) is an external interface of the VCP device used by the external host to communicate with the device. The SPI interface is compatible with the SPI interface used by general DSPs, so that those chips can interface with the VCP device without any glue logic. Because the SPI has the same logical view as the General Purpose Parallel Interface (GPI), the host can issue the same commands or data to the VCP device regardless of the physical interface.

SPI External Pins Connection

The SPI is a 3-wire or 4-wire synchronized serial interface used in many DSPs and micro controllers. The data is transferred bi-directionally from master to slave and from slave to master. The master provides clock SCK to synchronize the data transfer, and the signals SIMO and SOMI are for the data bit stream. SPI master can be a 3-wire or 4-wire SPI master, depending on if the master drives the $\overline{SS}$ signal. If the master is a 3-wire SPI master, the master does not drive $\overline{SS}$. Otherwise, the 4-wire SPI master pulls $\overline{SS}$ Low when transferring data. If the master is a 3-wire SPI master, the $\overline{SS}$ pin at the slave can be tied Low in the single master/slave pair or connected to the GPIO output of the master in the multiple slaves system.

Table 12. SPI Signals

Signal Name	Type	Description
SCK	I	SPI clock
SIMO	I	SPI slave input/master output
SOMI	O	SPI slave output/master input
$\overline{SS}$	I	SPI Slave select low

The VCP device will be the SPI slave, and the external host will be the SPI master. Signal SIMO will connect to the SI pin and signal SOMI will connect to the SO pin of the VCP device. Legerity VCP devices sample the input signal SI on the rising edge of the clock and change the output signal SO on the falling edge of the clock.

Figure 16 shows the SPI interface system with a 4-wire SPI master. One of the GPIO pins is needed to drive the $\overline{SS}$ pin of the VCP device. When the VCP device supports command framing on the $\overline{SS}$ pin, the GPIO pin of the master connecting to the $\overline{SS}$ pin of the slave is required, as shown in Figure 17, on page 30.

Figure 16. Four-Wire Master-Slave Connections

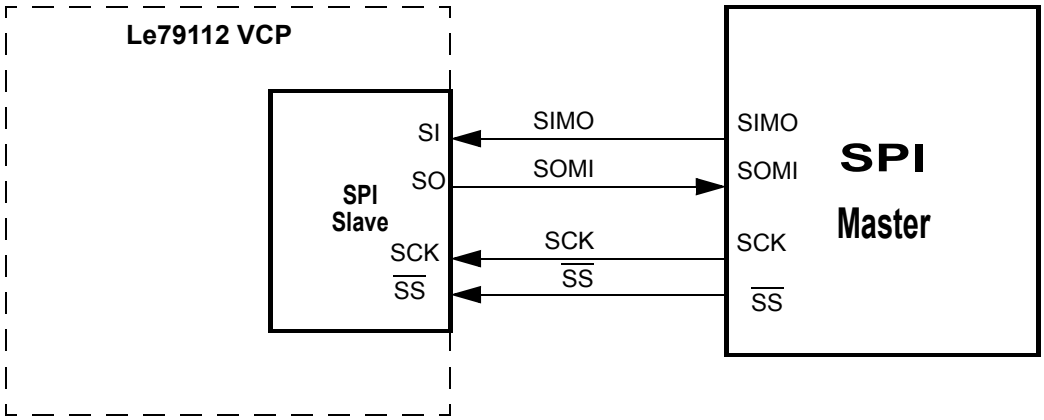
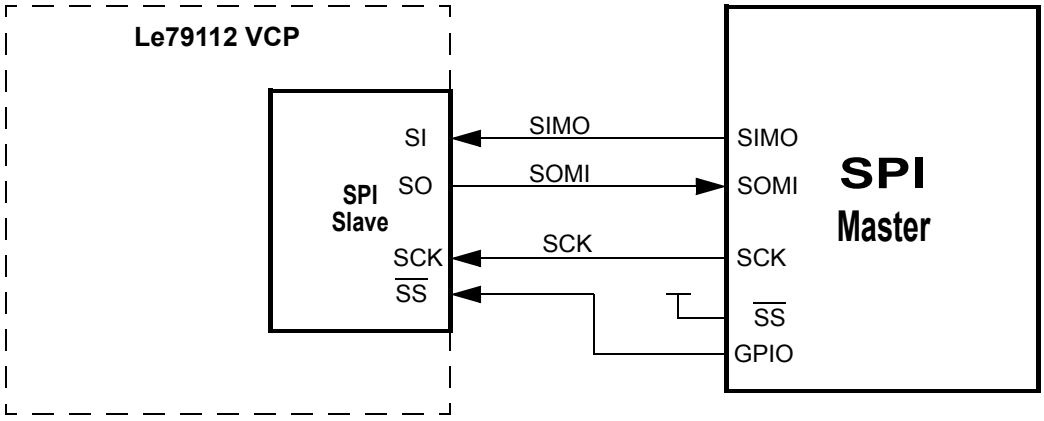


Figure 17. Three-Wire Master-Slave Connections



SPI Features

In order to connect to different SPI masters and share the same logic view with the GPI, the SPI slave of the VCP device has the following designs:

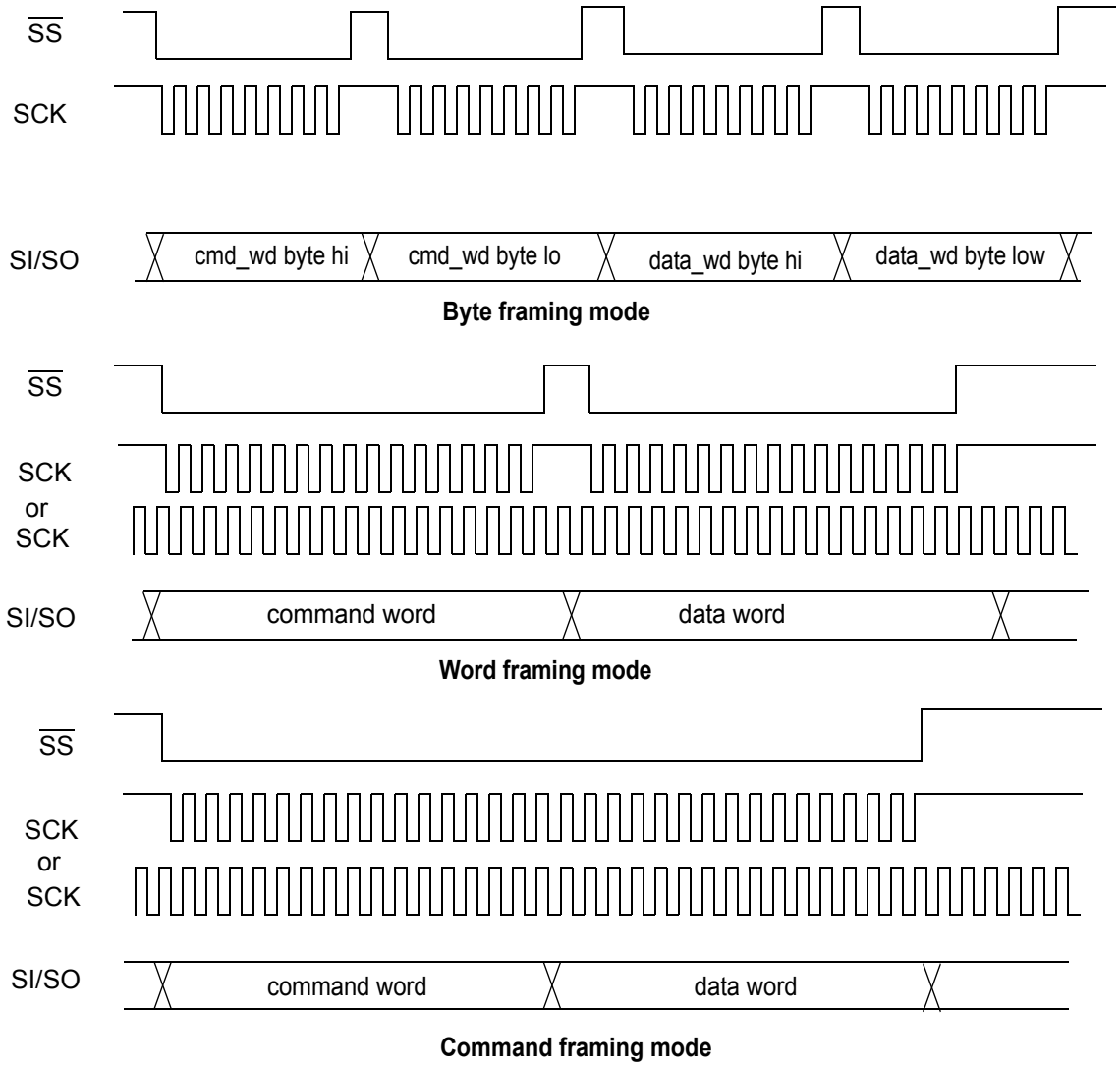
- Separate SI and SO pins.
- No daisy chain support.
- No read latency: no latency between the read command word and the first data word.
- Data byte swap is supported.
- $\overline{SS}$ pin supports byte/word framing, and command framing mode, as shown in Figure 18. The SPI slave state machine will reset if $\overline{SS}$ returns to High when the number of active SCK clocks is not equal to 8 or 16. If there is no clock, $\overline{SS}$ has to be Low for more than 125 ns (depending on the internal HCLK clock) to be recognized to reset SPI slave state machine. In command framing mode, the transition of $\overline{SS}$ to High means the command has ended. This event resets the SPI slave state machine, and the next falling edge of $\overline{SS}$ starts a new command.

Figure 18 shows three kinds of framing modes based on the behavior of $\overline{SS}$. In byte/word framing mode, $\overline{SS}$ is Low for 8/16 SCK clocks. For a two-word command, $\overline{SS}$ needs to toggle 4/2 times to complete the command transfer. In command framing mode, $\overline{SS}$ is Low for the whole duration of the command transfer. When the command is finished, $\overline{SS}$ will go back to High. If $\overline{SS}$ Low lasts shorter than the expected command length, the command is aborted and the SPI slave state machine resets. However if the user pulls $\overline{SS}$ Low longer than the expected command length, the extra words will start a new command sequence. In both word framing mode and command framing mode, SCK can be free-running or absent when $\overline{SS}$ is inactive High. In byte framing mode, SCK must be absent when $\overline{SS}$ is inactive High

Every time $\overline{SS}$ returns to High and the number of active SCK clocks is not equal to 8 or 16, the SPI slave state machine will reset. The next $\overline{SS}$ Low starts a new command sequence. In command framing mode, the transition back to High means the end of the command. If $\overline{SS}$ Low lasts less than 16 SCK clock cycles, no command byte is processed. If $\overline{SS}$ Low lasts more than 16 clock cycles, each 16-clock cycles triggers the SPI slave to process the word until $\overline{SS}$ returns back to High. The SPI slave will not reset

state machine when $\overline{SS}$ Low lasts exactly 8 or 16 SCK clock cycles to support byte/word framing mode. In byte/word framing mode, the user has to be aware of the command length, as there is no indication of command boundary.

Figure 18. $\overline{SS}$ Framing Modes



SPI Timing Requirements

The timing requirements for read and write accesses are shown in the following timing diagrams. The single data word read and write command is shown in Figure 19 and Figure 20. The data word can have data bytes swap like the single data word write command in Figure 21. Bits 7:0 of the data word comes out first and bits 15:8 of the data word come out second. The timing information for the read/write command is in Figure 22, Figure 23, and Table 13.

Figure 19. One Data Word Write in Byte Framing Mode

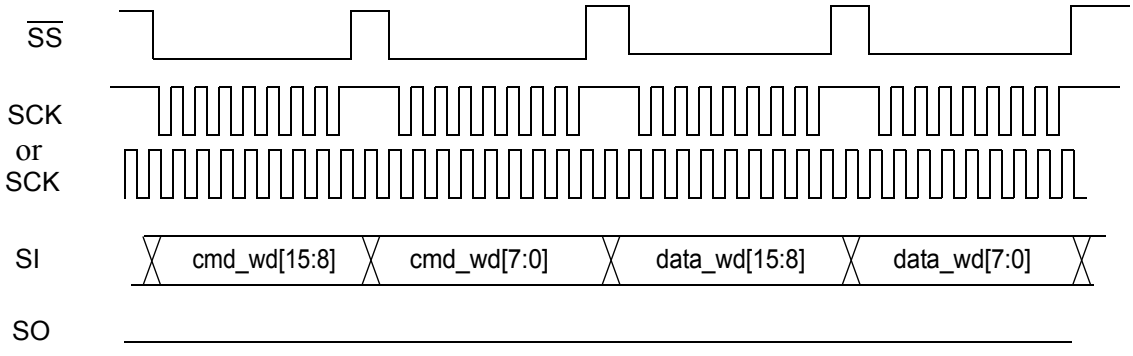


Figure 20. One Data Word Read in Word Framing Mode

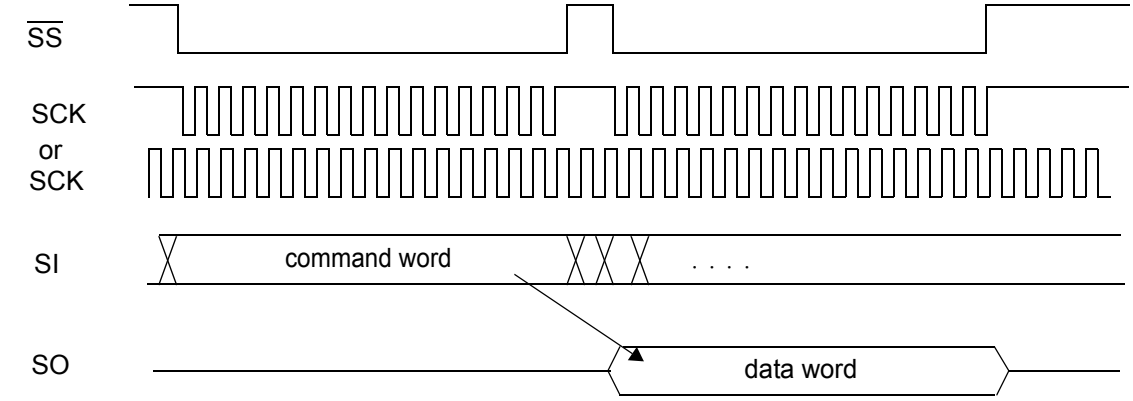


Figure 21. One Data Word Write in Byte Framing Mode with Byte Swap

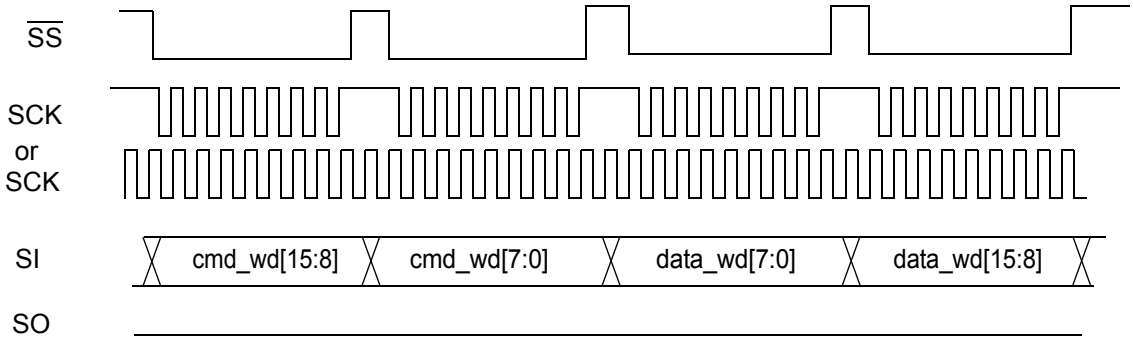


Table 13. SPI Timing Parameters

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Serial clock period	61	—	—	ns	
2	t_{DCH}	Serial clock HIGH pulse width	24	—	—		1
3	t_{DCL}	Serial clock LOW pulse width	24	—	—		1
4	t_{DCR}	Rise time of clock	—	—	8		
5	t_{DCF}	Fall time of clock	—	—	8		
6	t_{ICSS}	Slave select setup time, Input mode	15	—	t_{DCY}–18		
7	t_{ICSH}	Slave select hold time, Input mode	0	—	t_{DCY}–15		
8	t_{ICSL}	Slave select pulse width, Input mode	—	—	—		4
9	t_{ICSO}	Slave select off time, Input mode	61	—	—		1,3
10	t_{IDS}	Input data setup time	15	—	t_{DCY}–15		
11	t_{IDH}	Input data hold time	15	—	t_{DCY}–15		
13	t_{OCSS}	Slave select setup time, Output mode	15	—	t_{DCY}–18		
14	t_{OCSH}	Slave select hold time, Output mode	0	—	t_{DCY}–15		
15	t_{OCSL}	Slave select pulse width, Output mode	—	—	—		4
16	t_{OCSO}	Slave select off time, Output mode	61	—	—		1,3
17	t_{ODD}	Output data turn on delay	—	—	24		2, 5
18	t_{ODH}	Output data hold time	3	—	—		5
19	t_{ODOF}	Output data turn off delay	3	—	24		5
20	t_{ODC}	Output data valid	3	—	24		5

Notes:

1. *SCK may be stopped in the High or Low state indefinitely without loss of information. When $\overline{SS}$ is at Low state, every 16 SCK cycles the 16-bit received will be interpreted by the SPI interface logic.*
2. *The first data bit is enabled on the falling edge of $\overline{SS}$ or on the falling edge of SCK, whichever occurs last.*
3. *The SPI slave requires 61ns $\overline{SS}$ Off time just to make the transition of $\overline{SS}$ synchronized with SCK clock. In the command framing mode, there is no $\overline{SS}$ Off time between each 16-bit command/data and $\overline{SS}$ is held low until the end of command.*
4. *If $\overline{SS}$ is not held low for 16 or 8 SCK cycles exactly, the SPI slave will reset. During byte or word framing mode, $\overline{SS}$ is held low for 8 or 16 SCK cycles. During command framing mode, $\overline{SS}$ is held low for the whole duration of the command. Besides, multiple commands can be transferred with $\overline{SS}$ low for the whole duration of the multiple commands. The rising edge of the $\overline{SS}$ indicates the end of the command sequence and resets the SPI slave.*
5. *C_{load} = 40pF*

Figure 22. SPI Interface (Input Timing)

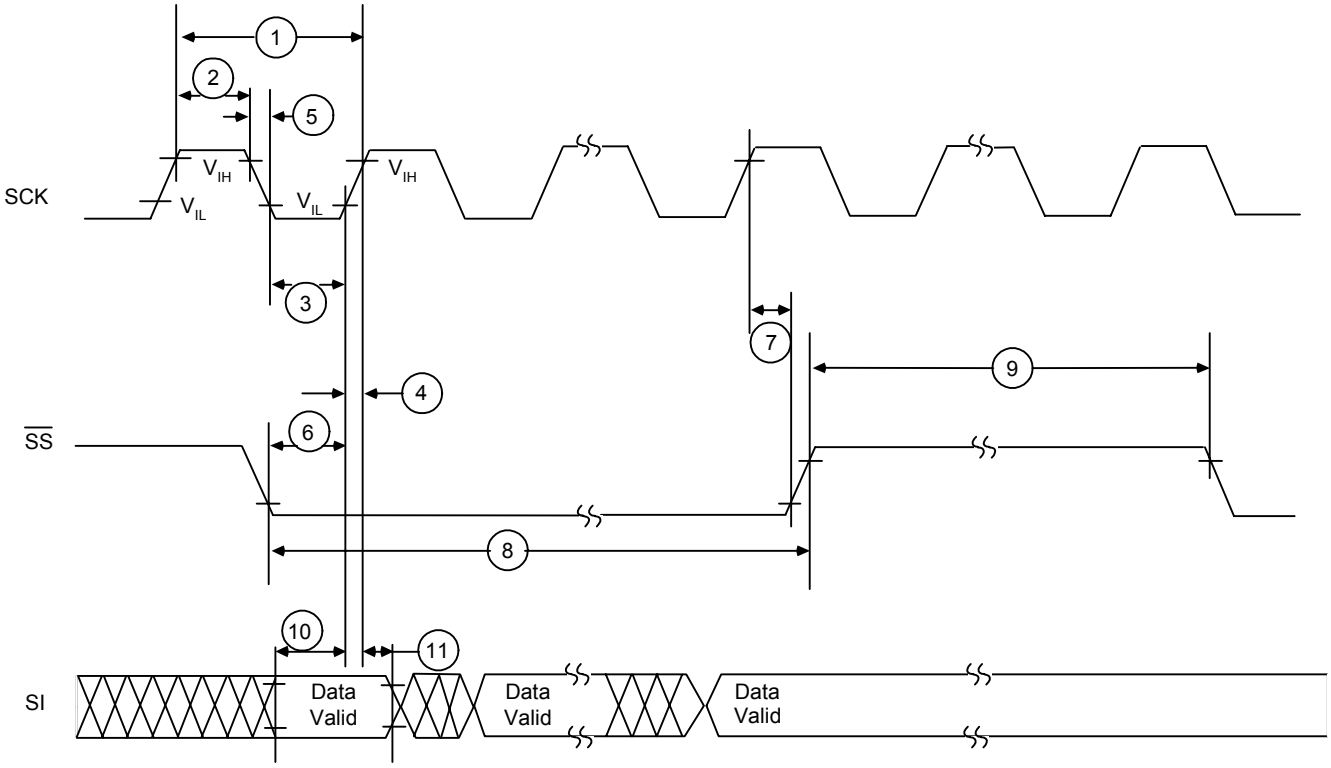
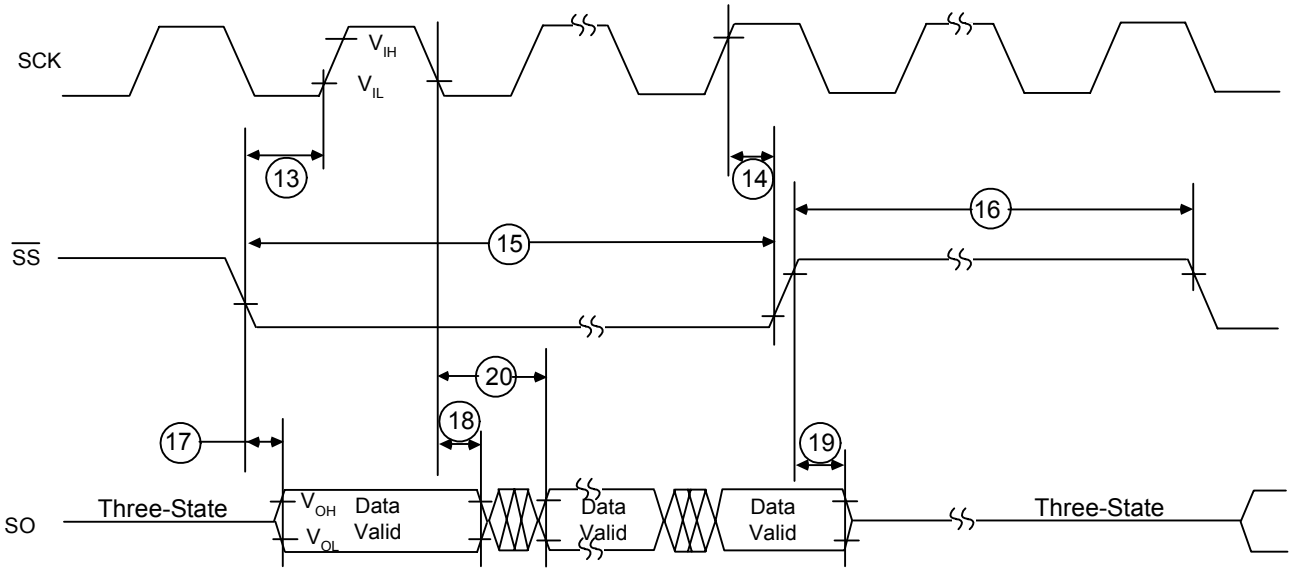


Figure 23. SPI Interface (Output Timing)

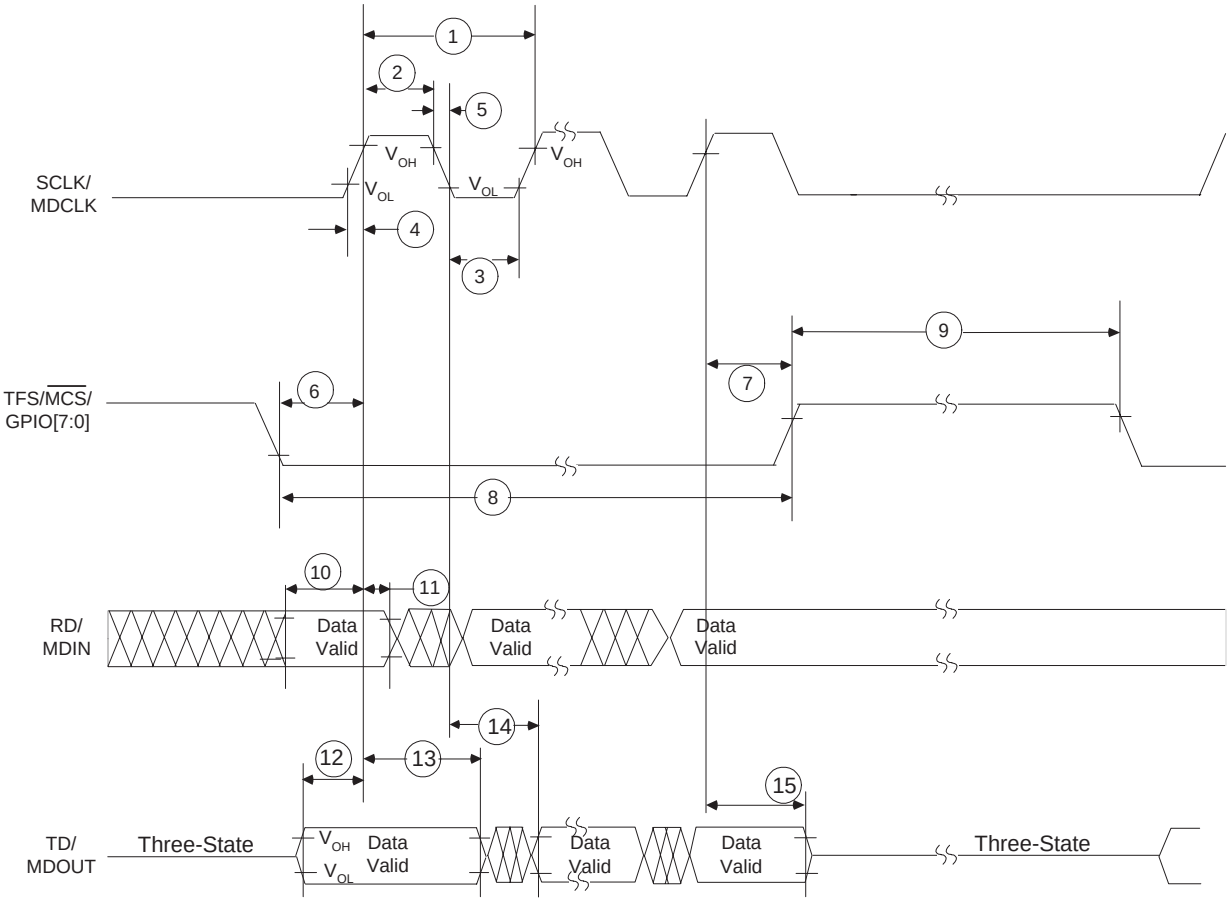


SPORT / MASTER MPI / GPIO[7:0] TIMING

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	135.6	140.2	—	ns	
2	t_{DCH}	Data clock HIGH pulse width	67.8	—	—		
3	t_{DCL}	Data clock LOW pulse width	67.8	—	—		
4	t_{DCR}	Rise time of clock	—	—	8		1
			—	—	24		2
5	t_{DCF}	Fall time of clock	—	—	8		1
			—	—	24		2
6	t_{CSS}	Chip select setup time	55	—	—		1
			66	—	—		2
7	t_{CSH}	Chip select hold time	50	—	—		
8	t_{CSL}	Chip select pulse width	—	1121	—		
9	t_{CSO}	Chip select off time	2000	—	—		
10	t_{RDS}	Input data setup time requirement	20	—	—		1
			30.3	—	—		2
11	t_{RDH}	Input data hold time requirement	0	—	—		
12	t_{TDS}	Output data setup time	55	—	—		
13	t_{TDH}	Output data hold time	50	—	—		
14	t_{TDD}	Output data delay	—	—	10		

1. *Assumes 40-pF load on SCLK, TD, and TFS or GPIO[7:0].*
2. *Assumes 150-pF load on SCLK and TD, but 40-pF load on TFS or GPIO[7:0].*

Figure 24. SPORT / MasterMPI Timing



PCM INTERFACE

PCLK accuracy = ± 100 PPM

Table 14. PCM Interface Timing Parameters

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	61	—	1953.1	ns	1,4, 6
			122	—	1953.1		1,5
23	t_{PCH}	PCM clock HIGH pulse width	24	—	—		4
			48	—	—		5
24	t_{PCL}	PCM clock LOW pulse width	24	—	—		4
			48	—	—		5
25	t_{PCF}	Fall time of clock	—	—	10		
26	t_{PCR}	Rise time of clock	—	—	10		
27	t_{FSS}	FS setup time	10	—	t_{PCY}–5		
28	t_{FSH}	FS hold time	5	—	125000-3t_{PCY}–10		
29	t_{TSD}	Delay to $\overline{TSC}$ valid	5	—	24		2,4
			5	—	35		2,5
30	t_{TSO}	Delay to $\overline{TSC}$ off	5	—	24		3,4
			5	—	35		3,5
31	t_{DXD}	PCM data output delay	5	—	24		4
			5	—	35		5
32	t_{DXH}	PCM data output hold time	5	—	24		4
			5	—	35		5
33	t_{DXZ}	PCM data output delay to high-Z	5	—	24		3,4
			5	—	35		3,5
34	t_{DRS}	PCM data input setup time	10	—	t_{PCY}–5		
35	t_{DRH}	PCM data input hold time	5	—	t_{PCY}–5		
36	t_{FST}	PCM or frame sync jitter time	–97	—	97		

Note:

1. *The PCM clock (PCLK) frequency must be an integer multiple of 512 kHz. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 MHz can be used for standard US transmission systems. The minimum clock frequency is 512 kHz.*
2. *$\overline{TSC}$ is delayed from FS by a typical value of* N • t_{PCY}*, where N is the value stored in the time/clock slot register.*
3. *$\overline{TSC}$ is an open drain driver. t_{TSO} is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The minimum pull-up resistance to VDD is 360 Ω.*
4. *C_{load} = 40pF*
5. *C_{load} = 150pF*
6. *PCLK must be present at all times to maintain proper internal operation. A total clock failure will result in a 60% reduction in internal MIPs within 125 µs. If the clock failure can be restored within 2 µs, a MIP drop of only 1% will result.*

Figure 25. PCM Highway Timing, SLAC XE = 0 (Transmit on Negative PCLK Edge)

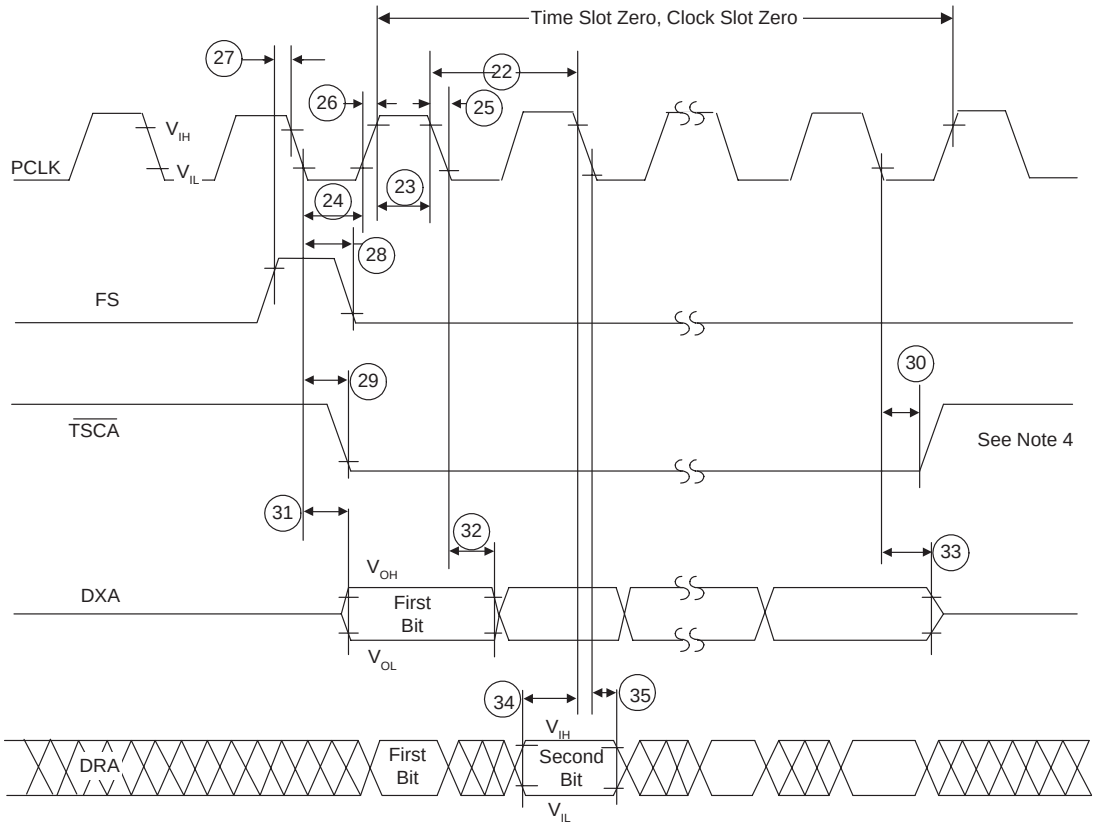
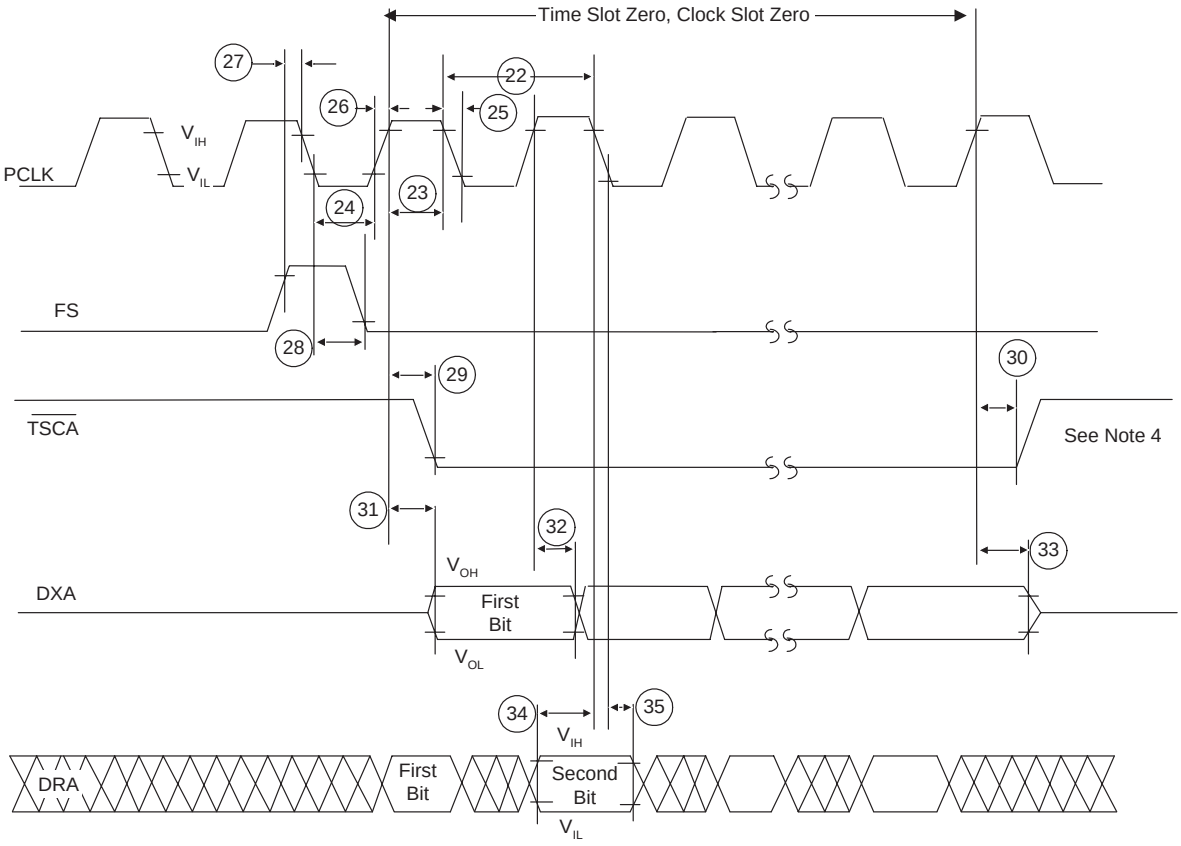


Figure 26. PCM Highway Timing, SLAC XE = 1 (Transmit on Positive PCLK Edge)



TROUBLESHOOTING AT INITIAL START-UP

First verify that the power supplies and the Configuration pins are appropriately set. Configuration pins must be set before releasing the Le79112 VCP from reset.

All four VDD25Ox pins must be wired together to distribute the on-board +2.5 V supply appropriately.

Secondly, perform the following steps to check that the VCP can be read and written through the HBI.

1. Probe the PWAIT pin. With reset inactive, perform a write of 0x04 to the Configure Interface register (CMD 0xFD04). This should result in the PWAIT pin going High; writing 0x06 (CMD 0xFD06) will make PWAIT go Low. This verifies the basic HAL function - VpHalHbiCmd().
2. With reset inactive, perform a read of the CMD register. This should return 0x0002 (the 2 bit is the interrupt pin status—it should be High, inactive). To read the CMD register in 8-bit mode, perform two back to back 8-bit reads of the CMD register location. For this step, no HAL function needed, simple address read.
3. Write to the Page register (CMD 0xFEzz - zz being any page number 0 - 0xFF). This write should be reflected in a subsequent read of the CMD register above. A CMD of 0xFEAA should result in a read from the CMD register of 0xAA02. This is writing the Page register which gets reflected in a read of the CMD register (again, the read is two 8-bit reads of the CMD register location—the same location read twice).
4. A read of the PCLK-Selection register (CMD 0x8700, followed by two 8-bit reads of the data register) with no PCLK or FS will result in a value of 0x32FB. If both PCLK and FS are present, then the value read will be PCLK/8 Khz. This step reads two bytes using HAL function - VpHalHbiRead().

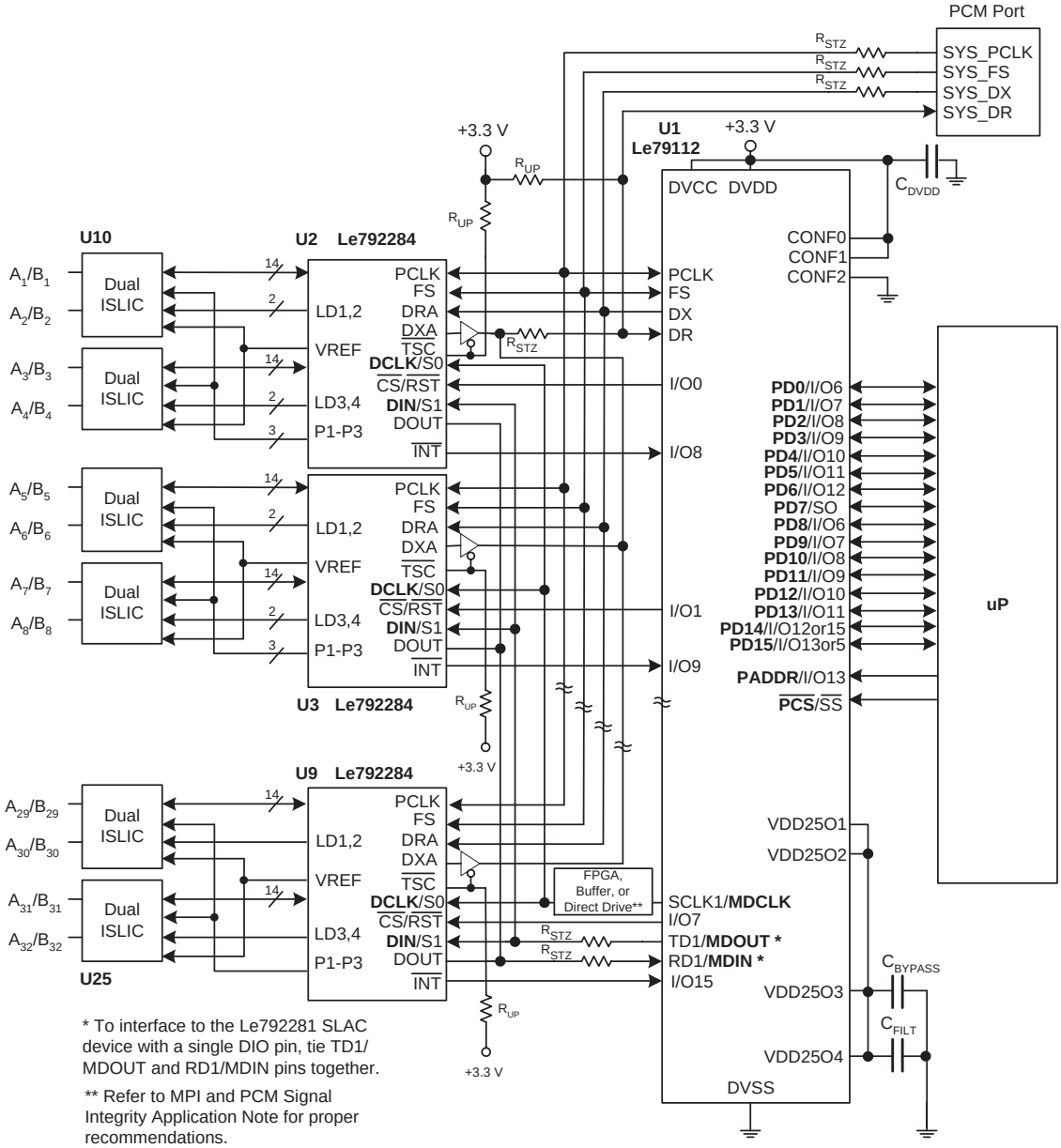
If the four steps above were completed successfully, the VCP device is now functional.

Thirdly, perform the memory test that is provided with the test application. The memory test will verify a proper HAL layer of C code, operation of the host processor, and operation of the VCP HBI interface (at speed). If these are working properly, there is a high probability of being able to successfully download and run code. The memory test is supplied in the C source code to be compiled for the host processor. It writes all the VCP mailboxes and reads them back. Code and documentation is located on the CD of the VCP release zip file.

Finally, run the quickstart application that is provided in the package and boot-load the API image. This provides verification of the VCP firmware image download and execution, the MPI to ISLAC interface, and the integrity of the PCM highway and the voice path. It also verifies basic call control, usage of profiles, DTMF decoding, Caller ID generation (VE880 series only), and line testing (VE790 series only). The boot-load is supplied as a binary firmware load to the VCP. It is to be boot-loaded into the VCP along with some C host code to boot-load and control the image. The code and documentation is located on the CD of the VCP release zip file or API_II code.

APPLICATION CIRCUIT

Figure 27. 32-Channel Line Card Schematic



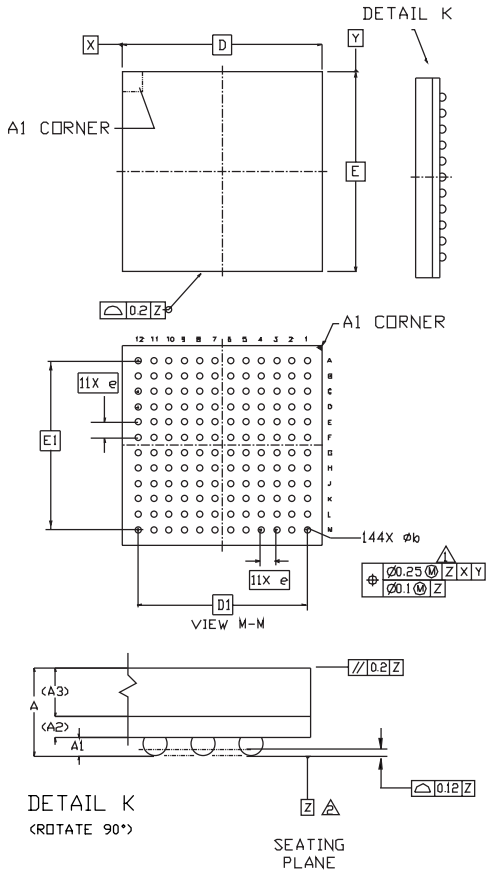
LINE CARD PARTS LIST

The following table lists the components required for a 32-channel Line Card circuit as shown in the preceding Application Circuit. External components required for VCP use are listed. Refer to the ISLIC and ISLAC data sheets for external components used with those devices.

Item	Qty	Type	Value	Tol.	Rating	Comments
U1	1	Le79112				VCP
U2 – U9	8	Le79Q2284 or other Le79228 ISLAC derivative				ISLAC device
U10 – U25	16	Le79232, Le79242, or Le79252				ISLIC device
R_{UP}	17	Resistor	10 kΩ	10%	1/16 W	
R_{STZ}	6	Resistor	40.2 Ω	10%	1/16 W	
C_{DVDD}	7	Capacitor	10 nF	20%	10 V	Ceramic
C_{BYPASS}	4	Capacitor	22 nF	20%	10 V	Ceramic
C_{FILT}	1	Capacitor	10 µF	20%	6.3 V	Ceramic or tantalum

PHYSICAL DIMENSIONS

144-Pin BGA



Symbol	144 BGA	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	0.32 REF	
A3	0.80 REF	
b	0.40	0.60
D	13 BSC	
E	13 BSC	
e	1 BSC	
D1	11 BSC	
E1	11 BSC	

NOTES:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
2. Datum Z is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

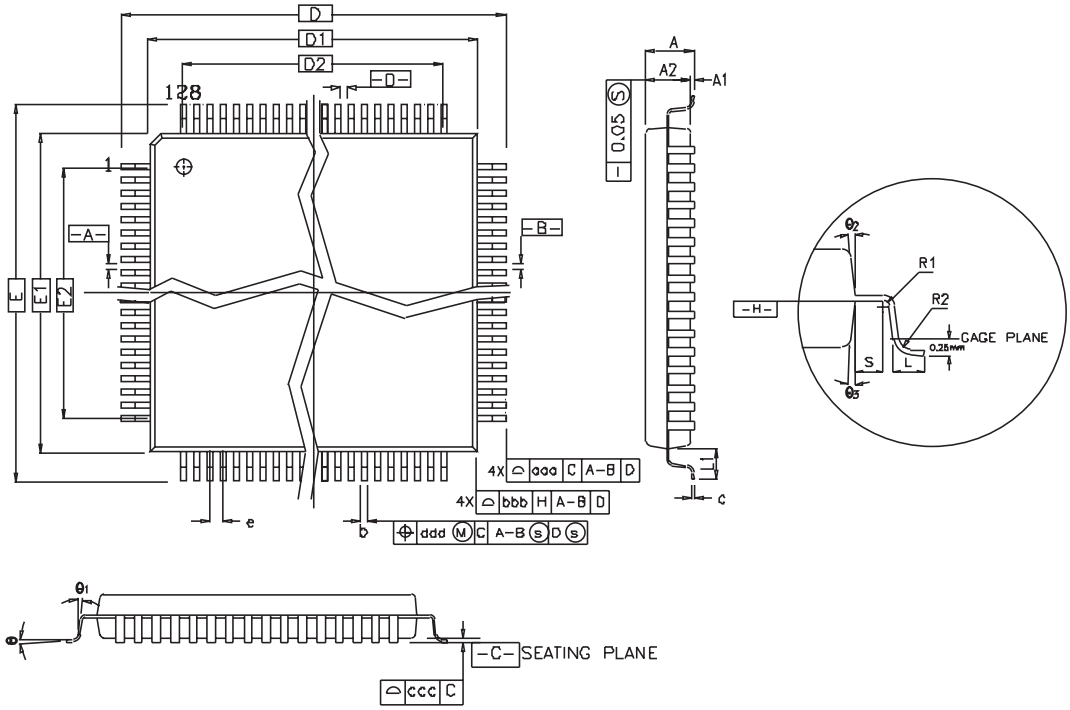
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME_Y14.5M	98ASH70694A-A

144-Lead LFBGA

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

128-Pin TQFP



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.08	-	-	0.003	-	-
θ	0º	3.5º	7º	0º	3.5º	7º
θ 1	0º	-	-	0º	-	-
θ 2	11º	12º	13º	11º	12º	13º
θ 3	11º	12º	13º	11º	12º	13º
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	-	-	0.008	-	-

Symbol	128L					
	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
b	-	0.16	-	-	0.006	-
e	0.40 BSC			0.016 BSC		
D2	12.40			0.488		
D3	12.40			0.488		
E2	8.00			0.315		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Notes:
1. Dimensions “D1” and “E1” do not include mold protrusion. Allowable protrusion is 0.25mm per side. “D1” and “E1” are maximum plastic body size dimensions including mold mismatch.
2. Dimension “b” does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.

128-Pin TQFP

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- Removed "Channel 1" reference from Page 0 of Figure 6.
- Removed Transparent mode references.
- Added power dissipation values.
- Added 128-pin TQFP package data.
- Removed Spare pins from Pin Descriptions.
- Added a new Internal Block Diagram.

Revision B1 to B2

- Updated product branding throughout document.

Revision B2 to C1

- Updated OPNs

Revision C1 to D1

- Added "Packing" column and Note 2 to *Ordering Information*, on page 1; added green package note
- Renamed Digital Voice Processor (DVP) to VoiceEdge Control Processor (VCP)
- Changed OPN for 128-pin TQFP package from Le79112A**T**C to Le79112A**V**C
- Block Diagrams modified.
- Pin Descriptions, made ICE interface reserved pins, made MCM and 100/64 DVDD pins, Master PCM pins renamed Master MPI2.
- In DC Specifications, changed Output Low Voltage Condition from IoI = 10 mA to 8 mA.
- System Register section overhauled, complete set of System Registers added.
- Modified drawings in Figures 13-16 and corresponding Tables 12 and 13. t_{RD_DV} Max increased from 20 to 25 ns.
- Table 13, *SPI Timing Parameters*, on page 33, t_{ICSS} and t_{OCSS} Max increased from t_{DCY-15} to t_{DCY-18} ns.
- Table 14, *PCM Interface Timing Parameters*, on page 36, Note 3, minimum pull-up resistance of 360 Ω to VDD added.
- Added Troubleshooting section.
- Added Application Circuit and Parts List.
- Major text enhancements and deletions.

Revision D1 to E1

- Page 5, Added TQFP cross reference to Table 1.
- Page 18, Added duplicate MMAP (bit D9) and HWRES (bit D8) commands to the Hardware Reset register.
- Page 20, Added CFAIL bit clearing delay at start-up.
- Page 35, SPORT/Master MPI/GPIO[7:0] Timing, No. 14, Output data delay, 10 ns Min changed to 10 ns Max.
- Page 39, Modified Application Circuit and Line Card Parts List.
- Minor edits.

Revision E1 to F1

- Pages 9 and 10, text deletions.
- Page 18, in Hardware Reset register, changed bit D2 from RSVD to CLKNOCLR.
- Page 39 and 40, updated Application Circuit and Line Card Parts List.
- Enhanced format of package drawing in *Physical Dimensions*, on page 41.
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007.