Le79114
VoiceEdge™ Control Processor II
VE790 Series
Data Sheet

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Applications

- Cost effective voice solution for long or short loops providing POTS and integrated test capabilities
- Applications include: IVD, DLC, CO, Voice-enabled DSLAM, PBX/KTS, MDU, MSAP, MSAN

Features

- Aggregated call control lowers demand on host micro-processor
- 64 channels of call control
- Provides expanded line and circuit testing in conjunction with Zarlink's Ve790 Series chipsets
  - Provides 32 channels of simultaneous DTMF
  - Provides 4 channels of simultaneous line testing
- Software interface using VoicePath™ API-II
- Software downloadable, field upgradeable, expandable
- Serial and parallel host controller interface options
- Complete control of up to 16 Quad ISLAC devices
  - Two master SPI ports
  - 32 General Purpose I/Os
  - 16 configured as chip selects
  - 16 configured for interrupts
- Two slave PCM highway ports
  - Single or dual PCM highways capable of operating up to 16.384 MHz
  - Separate test highway option
- Internal PLL and hardware network timing recovery for creating analog sampling clocks
- 3.3 V compliant I/O; Internal 3.3 V to 1.8 V linear regulator for the core logic

Description

The Le79114 VoiceEdge™ Control Processor II (VCP II) is a second generation platform that delivers enhanced call control, self-test and line test capabilities. This latest processor works with Zarlink Ve790 devices using its SPI interface(s), PCM port(s), and GPIO. The Le79114 VCP II device provides the same integrated line-testing and feature-set as the Le79112 VCP device, plus additional capabilities such as 32 channels of simultaneous DTMF detection and 64 channels of improved POTS control.

This product enables the design of a low-cost, high-performance, fully software programmable line interface for multiple country applications. All AC, DC, signaling parameters and data are fully programmable. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost-effective.

The Le79114 device is provided with extensive software and support, through the LineCare™ software suite, enabling the designer to develop a fully programmable solution in the least amount of time.

Ordering Information

Device	Package (Green)[1]	Packing[2]
Le79114KVC	128 Pin TQFP	Tray

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

Related Literature

- 081130 Le79232 SLIC Device Data Sheet
- 081185 Le79252 SLIC Device Data Sheet
- 081256 Le79228 Quad ISLAC™ Device Data Sheet
- 081190 Le792288 Octal ISLAC™ Device Data Sheet
- 081507 MPI and PCM Signal Integrity Application Note
- 081572 Le79114-SW VCP Software Package Data Sheet
- VoicePath™ API II Reference Guide

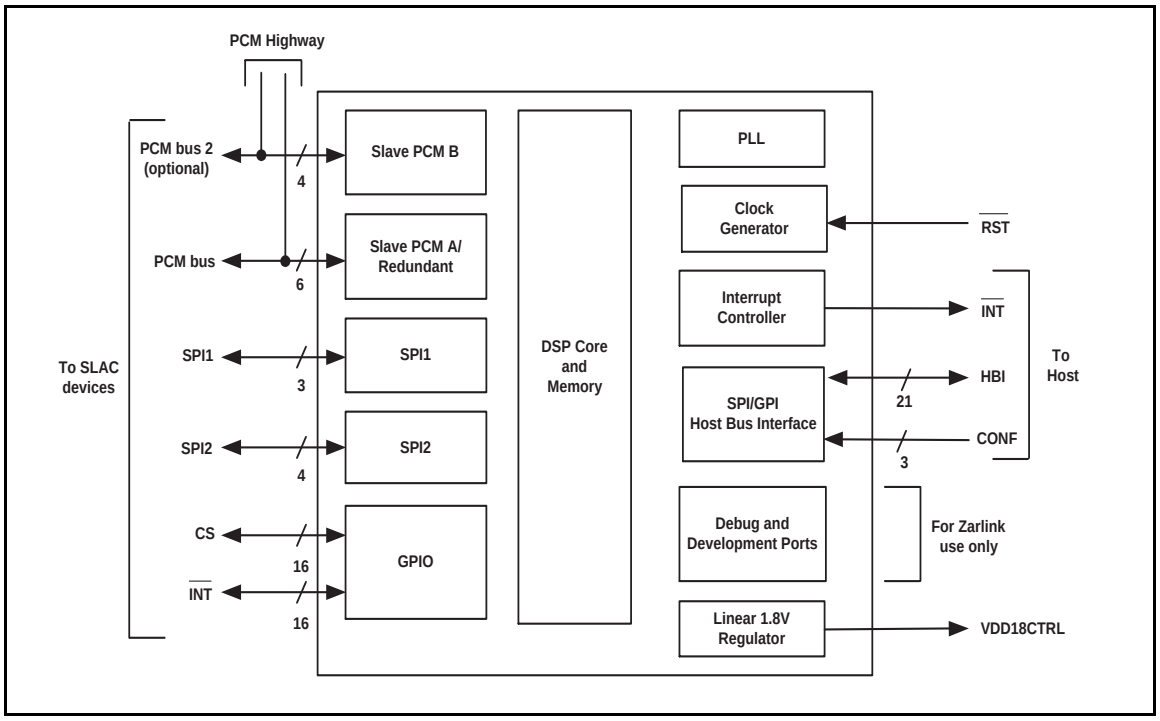

Figure 1 - Block Diagram

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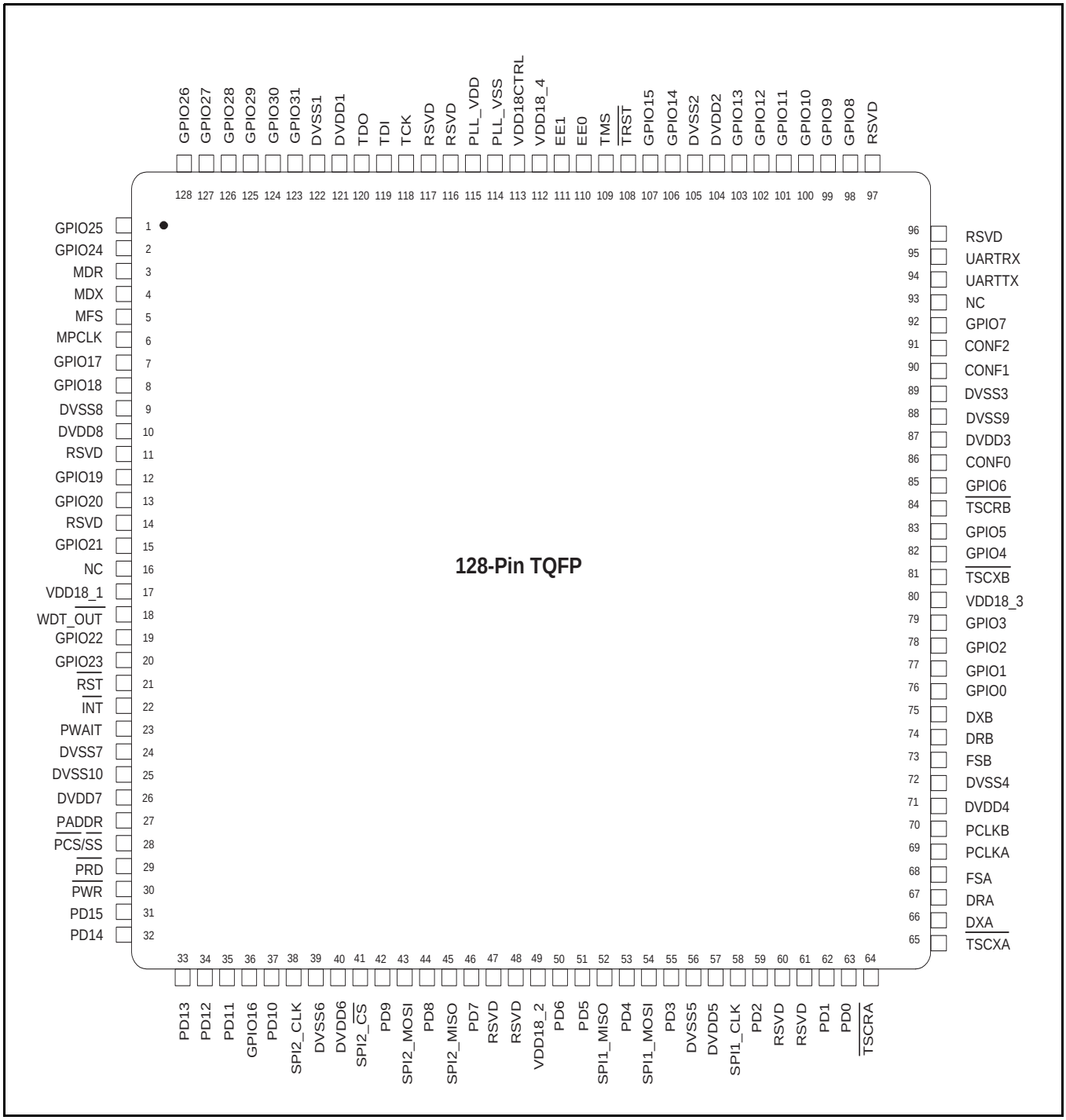


Figure 2 - Le79114KVC 128-Pin TQFP Package

Pin Descriptions

All signals are CMOS levels unless otherwise stated.

The VCP II device has 128 pins.

Pin Name (Alternate)	Pin#	Type	Reset[1]	Description
$CONF_2$	91	Input	Z	VCP II configuration pins that determine serial or parallel modes (8-bit, 16-bit, separate read and write strobes, data strobe and combined read/write strobe). **See Table for configuration summary.**
$CONF_1$	90	Input	Z	
$CONF_0$	86	Input	Z	
$\overline{PCS}/\overline{SS}$	28	Input	Z	$\overline{PCS}$: Parallel interface: active-low chip select. $\overline{SS}$: Serial interface: active-low slave select.
$\overline{PRD}$ (PRD/$\overline{WR}$ or SI)	29	Input	Z	$\overline{PRD}$: Parallel Separate Rd/Wr strobe: active-low read strobe. PRD/$\overline{WR}$: Parallel Combined Rd/Wr strobe: active-high read control/active-low write control. SI: Serial interface: data input.
$\overline{PWR}$ ($\overline{PDS}$ or SCK)	30	Input	Z	$\overline{PWR}$: Parallel Separate Rd/Wr strobe: active-low write strobe $\overline{PDS}$: Parallel Combined Rd/Wr strobe: active-low data strobe. SCK: Serial interface: data clock.
PD_{15}	31	Input/ Output	Z/Keeper	16-bit parallel interface: bi-directional data bits 15-8. Serial interface: reserved.
PD_{14}	32			
PD_{13}	33			
PD_{12}	34			
PD_{11}	35			
PD_{10}	37			
PD_9	42			
PD_8	44			
PD_7 (SO)	46	Input/ Output	Z/Pull-down (Parallel) Z (Serial)	PD_7: Parallel interface: bi-directional data bit 7. SO: Serial interface: data output.
PD_6	50	Input/ Output	Z/Keeper	Parallel interface: bi-directional data bits 6 through 0. Serial interface: reserved.
PD_5	51			
PD_4	53			
PD_3	55			
PD_2	59			
PD_1	62			
PD_0	63			
PWAIT	23	Output	Z	Parallel interface: programmable active-low or active-high signal to extend the current access cycle. PWAIT should be connected to a resistor pulled to the inactive state. If unused, let pin float. Serial interface: reserved.
PADDR	27	Input	Z	Parallel interface: signal to indicate the start of a command sequence. Serial interface: reserved.
$\overline{INT}$	22	Output	Z/Pull-up	Host Interrupt indicator(active low).

Table 1 - Le79114 VCP II Device Pin Description (Host Interface Pins)

Pin Name	Pin#	Type	Reset[1]	Description		
PCLKA	69	Input	Z	Slave PCM Highway A	Clock input.	Mutually exclusive with PCLKB operation.
FSA	68	Input[2]	Z		Framing input.	Mutually exclusive with FSB operation.
DXA	66	Output[3]	Z		PCM data output.	Mutually exclusive with DXB operation.
DRA	67	Input[2]	Z		PCM data input.	Mutually exclusive with DRB operation.
$\overline{\text{TSCXA}}$	65	Output	Z		PCM data output tristate control.	Mutually exclusive with $\overline{\text{TSCXB}}$ operation. This output is active low when DXA is transmitting. The output is open-drain and is normally inactive (high impedance). A pull-up load should be connected to DVDD. If output not used, leave node float.
$\overline{\text{TSCRA}}$	64	Output	Z		PCM data input tristate control.	Mutually exclusive with $\overline{\text{TSCRB}}$ operation. This output is active low when DRA is transmitting. The output is open-drain and is normally inactive (high impedance). A pull-up load should be connected to DVDD. If output not used, leave node float.
PCLKB	70	Input	Z	Redundant Slave PCM Highway	Clock input.	Mutually exclusive with PCLKA operation. If not used, tie pin to DVSS.
FSB	73	Input[2]	Z		Framing input.	Mutually exclusive with FSA operation. If not used, tie pin to DVSS.
DXB	75	Output[3]	Z		PCM data output.	Mutually exclusive with DXA operation. If not used, tie pin to DVSS.
DRB	74	Input[2]	Z		PCM data input.	Mutually exclusive with DRA operation. If not used, tie pin to DVSS.
$\overline{\text{TSCXB}}$	81	Output	Z		PCM data output tristate control.	Mutually exclusive with $\overline{\text{TSCXA}}$ operation. This output is active low when DXB is transmitting. The output is open-drain and is normally inactive (high impedance). A pull-up load should be connected to DVDD. If output not used, leave node float.
$\overline{\text{TSCRB}}$	84	Output	Z		PCM data input tristate control.	Mutually exclusive with $\overline{\text{TSCRA}}$ operation. This output is active low when DRB is transmitting. The output is open-drain and is normally inactive (high impedance). A pull-up load should be connected to DVDD. If output not used, leave node float.
MPCLK	6	Input[2]	Z	Slave PCM Highway B (Optional)	Clock input.	If not used, tie pin to DVSS.
MFS	5	Input[2]	Z		Framing input.	
MDX	4	Output[3]	Z		PCM data output.	
MDR	3	Input[2]	Z		PCM data input.	

Table 2 - Le79114 VCP II Device Pin Description (PCM Interface Pins)

Slave PCM Highway A has a Redundant Slave PCM Highway which can be used in parallel to PCM Highway A. When enabled, the VCP II will automatically switch between Highway A and Redundant when either highway suffers a system failure. Slave PCM Highway A, or the Redundant Slave PCM Highway, is programmed by selecting VP_OPTION_HWY_A from the API.

Slave PCM Highway B use is optional. It can be used as a second PCM Highway or as a Test Highway. Slave PCM Highway B is programmed by selecting VP_OPTION_HWY_B from the API.

Pin Name (Alternate)	Pin#	Type	Reset[1]	Description	
$\overline{\text{TRST}}$	108	Input	Pull-up	Debug reset input. Tie to DVSS through 1 KΩ resistor.	These pins are for Zarlink debug use only. Refer to the Debug Interface section for more information.
TCK	118	Input	Pull-up	Debug clock input.	
TMS	109	Input	Pull-up	Debug mode select input.	
TDI	119	Input	Pull-up	Debug data input.	
TDO	120	Output	Z	Debug data output.	
EE0	110	Input/Output	Z/Pull-down	Emulator control pin.	For Zarlink development use only, leave pins float.
EE1	111	Input/Output	Z/Pull-down	Emulator debug output pin.	
UARTTX	94	Output	1	Transmit pin.	For Zarlink development use only, leave pins float.
UARTRX	95	Input	Z/Pullup	Receive pin.	

Table 3 - Le79114 VCP II Device Pin Description (Debug and Development Ports)

Pin Name	Pin#	Type	Reset[1]	Description
SPI1_CLK	58	Output	0	SPI1 clock output.
SPI1_MOSI	54	Input/ Output	Z	SPI1 Master output, Slave input.
SPI1_MISO	52	Input	Z	SPI1 Master input, Slave output.
SPI2_$\overline{CS}$	41	Output	1	SPI2 alternate chip select output.
SPI2_CLK	38	Output	0	SPI2 clock output.
SPI2_MOSI	43	Input/ Output	Z	SPI2 Master output, Slave input. If unused, tie to DVSS through 10 KΩ resistor.
SPI2_MISO	45	Input	Z	SPI2 Master input, Slave output. If unused, tie to DVSS through 10 KΩ resistor.
GPIO0 ($\overline{MINT0}$/TIMER0)	76	Input/ Output	Z/Pullup	General Purpose I/O. Can function as an Interrupt input when connected to an ISLAC. Also has timer input/output functionality.
GPIO1 ($\overline{MINT1}$/TIMER1)	77			
GPIO2 ($\overline{MINT2}$)	78	Input/ Output	Z/Pullup	General Purpose I/O. Can function as an Interrupt input when connected to an ISLAC.
GPIO3 ($\overline{MINT3}$)	79			
GPIO4 ($\overline{MINT4}$)	82			
GPIO5 ($\overline{MINT5}$)	83			
GPIO6 ($\overline{MINT6}$)	85			
GPIO7 ($\overline{MINT7}$)	92			
GPIO8 ($\overline{MINT8}$)	98			
GPIO9 ($\overline{MINT9}$)	99			
GPIO10 ($\overline{MINT10}$)	100			
GPIO11 ($\overline{MINT11}$)	101			
GPIO12 ($\overline{MINT12}$)	102			
GPIO13 ($\overline{MINT13}$)	103			
GPIO14 ($\overline{MINT14}$)	106			
GPIO15 ($\overline{MINT15}$)	107			

Table 4 - Le79114 VCP II Device Pin Description (Peripheral Logic Pins)

Pin Name	Pin#	Type	Reset[1]	Description
GPIO16 ($\overline{MCS0}$)	36	Input/ Output	Z/Pull-down (Note, this pull-down is present only during reset)	General Purpose I/O. Can function as a gated Chip Select for a Serial slave device.
GPIO17 ($\overline{MCS1}$)	7			
GPIO18 ($\overline{MCS2}$)	8			
GPIO19 ($\overline{MCS3}$)	12			
GPIO20 ($\overline{MCS4}$)	13			
GPIO21 ($\overline{MCS5}$)	15			
GPIO22 ($\overline{MCS6}$)	19			
GPIO23 ($\overline{MCS7}$)	20			
GPIO24 ($\overline{MCS8}$)	2			General Purpose I/O. Can function as a gated Chip Select for a Serial slave device. These pins serve a dual purpose, they provide boot up options for Zarlink use. Do not use pull-up devices on these nodes. Refer to Table 11 for more information.
GPIO25 ($\overline{MCS9}$)	1			
GPIO26 ($\overline{MCS10}$)	128			
GPIO27 ($\overline{MCS11}$)	127			
GPIO28 ($\overline{MCS12}$)	126			
GPIO29 ($\overline{MCS13}$)	125			
GPIO30 ($\overline{MCS14}$)	124			
GPIO31 ($\overline{MCS15}$)	123			
RSVD	11, 14, 47, 48, 60, 61, 96, 97			Reserved. These pins are internally connected. Pins must be left floating.

Table 4 - Le79114 VCP II Device Pin Description (Peripheral Logic Pins) (continued)

Pin Name	Pin#	Type	Description
PLL_VDD	115	Supply	Analog power supply, which must be connected to the digital power supply externally. It is important to provide a decoupling capacitor of 0.1 µF from PLL_VDD to PLL_VSS.
PLL_VSS	114	Ground	Analog ground. Analog and digital grounds must be connected externally to the same ground plane.
DVDD1	121	Supply	+3.3 V Digital power supply. This supply handles the 3.3 V external digital I/O devices. It is important to provide local decoupling capacitors of 0.1 µF to the ground plane on each pin in addition to a parallel 10 µF capacitor on the ground plane.
DVDD2	104		
DVDD3	87		
DVDD4	71		
DVDD5	57		
DVDD6	40		
DVDD7	26		
DVDD8	10		
VDD18_1	17	Supply	+1.8 V Digital power supply. It is important to provide local decoupling capacitors of 0.1 µF to the ground plane on each pin in addition to a parallel 10 µF or 100 µF capacitor on this supply node to the ground plane.
VDD18_2	49		
VDD18_3	80		
VDD18_4	112		

Table 5 - Le79114 VCP II Device Pin Description (Power Supply Pins)

Pin Name	Pin#	Type	Description
DVSS1	122	Ground	Digital ground. Digital and analog grounds must be connected.
DVSS2	105		
DVSS3	89		
DVSS4	72		
DVSS5	56		
DVSS6	39		
DVSS7	24		
DVSS8	9		
DVSS9	88		
DVSS10	25		
VDD18CTRL	113	Output	+1.8 V linear regulator gate drive output. If used, connect to the gate of an external transistor to form the +1.8 V core voltage.

Table 5 - Le79114 VCP II Device Pin Description (Power Supply Pins)

Pin Name	Pin#	Type	Reset[1]	Description
$\overline{RST}$	21	Input	Z	Active Low reset input returns chip to default state. $\overline{RST}$ pulse width must be a minimum of 100 ns. The pin must be externally pulled up.
WDT_$\overline{OUT}$	18	Output	Z	Active Low, open-drain output from Watchdog timer function. Triggers on watchdog timer expiration and power on reset. The minimum pulse width for WDT_$\overline{OUT}$ is 1 ms. This pin must be shorted to $\overline{RST}$ if the watchdog function is desired to reset the VCP II or system.
RSVD	116, 117			Reserved. These pins are internally connected. Pins must be left floating.
NC	16, 93			No connect. These pins are not internally connected. Pins can be used as tie points.

Table 6 - Le79114 VCP II Device Pin Description (Control Pins)

Note:

1. *Logic state after reset.*

   Z = No state driven, high impedance.
   1 = Logic high.
   0 = Logic low.
   Keeper = Kept in current state, not allowed to float.
   Pull-up = Internal pull-up provided.
   Pull-down = Internal pull-down provided.

2. *Used as an input, but pin has I/O capability.*
3. *Used as an output, but pin has I/O capability.*

Configuration Assignments ($CONF_2$ - $CONF_0$)

$CONF_2$ - $CONF_0$	Host Interface	Parallel Data Width	Parallel Read/Write Strobes
000	Parallel	8	Combined
001	Parallel	8	Separate
010	Parallel	16	Combined
011	Parallel	16	Separate
100	Serial	NA	NA
101	Reserved		
110			
111			

1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–60 ºC ≤ T_A ≤ +125 ºC
Ambient Temperature, under Bias	–40 ºC ≤ T_A ≤ +85 ºC
Maximum Junction Temperature	+125 ºC
Ambient relative humidity (non condensing)	5 % to 95 %
PLL_VDD with respect to PLL_VSS or DVSS	–0.4 V to +4.0 V
DVDD with respect to PLL_VSS or DVSS	–0.4 V to +4.0 V
VDD18 with respect to DVSS or PLL_VSS	–0.4 V to +1.98 V
Latch up immunity (any pin)	±100 mA
Any other pin with respect to DVSS or PLL_VSS	–0.4 V to (DVDD + 0.4 V)
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

Thermal Resistances

Thermal resistances for the 128-pin TQFP.

Theta-JA	33.7 ºC/W
Psi-JT	0.1 ºC/W
Theta-JB	28.5 ºC/W
Theta-JC	4.3 ºC/W

1.2 Operating Ranges

Zarlink guarantees the performance of this device over commercial (0 ºC to 70 ºC) and industrial (-40 ºC to 85 ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40 ºC to +85 ºC
Ambient Relative Humidity	15 % to 85 %

Electrical Ranges

DVDD	+3.3 V ± 5% (see note)
PLL_VDD	+3.3 V ± 5%, DVDD ± 50 mV (see note)
VDD18	+1.8 V ± 5% (see note)
DVSS	0 V
PLL_VSS	DVSS ±10 mV
Digital pins with respect to DVSS	DVSS to +3.465 V

Note: *+3.3 V supply should ramp and reach a steady final value before +1.8 V supply ramps. $\overline{RST}$ should be held low until both supplies have reached final values. If +3.3 V supply and +1.8 V supply ramps and sequence can not be guaranteed, both $\overline{RST}$ and $\overline{TRST}$ should be held low until both supplies have reached final values. In the case where +3.3 V supply and +1.8 V supply ramps and sequence can not be guaranteed, $\overline{TRST}$ is typically tied low via a 1 KΩ resistor to ground.*

1.3 DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Input Low Voltage		– 0.5	—	0.8	V	1
2	Input High Voltage		2.0	—	3.465	V	1
3	$\overline{RST}$ Input Low Voltage		– 0.5		0.5	V	
4	$\overline{RST}$ Input High Voltage		1.1		3.465	V	
5a	Input Leakage Current	0 to DVDD, outputs in high-Z state.	–10	—	+10	µA	3
5b			–100	—	+100	µA	4
6	Input hysteresis		0.15	0.225	0.3	V	2
7	Output Low Voltage	Iol = 10 mA	—	—	0.4	V	5
8	Output High Voltage	Ioh = 400 µA	DVDD –0.4	—	—		5
9	DVDD / PLL_VDD Power Dissipation	DSP in peak operation.	—		50	mW	6
10	VDD18 Power Dissipation	DSP in peak operation.	—		800	mW	6

Notes:

1. *Applies to all digital input pins except $\overline{RST}$.*
2. *Applies to all digital input pins.*
3. *Pins with no pull-up, pull-down or keeper.*
4. *Pins with pull-up, pull-down or keeper.*
5. *Applies to all digital output pins.*
6. *No external DC loads present.*

2.0 Host Bus Interface (HBI) Overview

The Host Bus Interface provides a means for exchanging control, configuration, and status information with an external host processor. The HBI is able to sustain 16-bit transactions up to 10 MHz rate with minimal latency.

This interface is implemented through a combination of hardware and firmware. The design is layered as shown in Figure 3. Hardware provides a generic means for transporting data between the host and internal memory. The interpretation of the data is provided by firmware running on the VCP II. This layered architecture allows the definition of the application level interface to change by modifying the firmware.

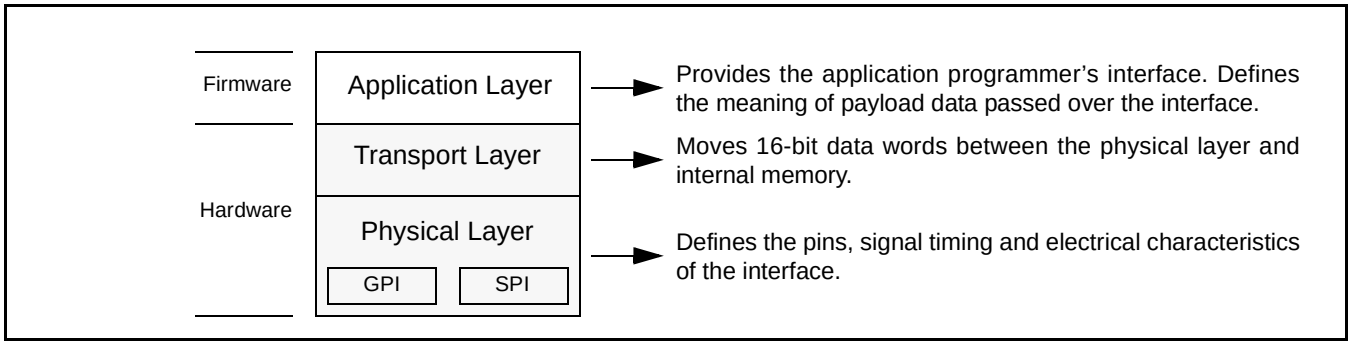


Figure 3 - Host Bus Interface Layers

2.1 Transport Layer

The transport layer moves 16-bit data words between the physical interface and internal memory or registers on an internal bus. It defines the structure of a transport frame, which consists of a 16-bit command word followed by 0 or more 16-bit payload data words. It also defines the interface address model, and provides mapping between interface and internal addresses.

2.2 Application Layer

The application layer defines the programmer's interface, and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the programmer's interface can change by providing new software.

2.3 Physical Layer

The physical layer provides the functionality needed to electrically interface with a host processor. It defines the pins, signal timing and electrical characteristics of the interface. Two physical interfaces are provided. The General Purpose Parallel Interface (GPI) implements an 8-bit or 16-bit wide parallel interface. Options are selected via the configuration pins, refer to <Cross-Reference>Table . The Serial Peripheral Interface (SPI) implements a 4-wire synchronous serial slave interface.

3.0 Transport Layer

The primary responsibility of the transport layer is to move 16-bit data words between the physical interface and the device's internal memory. Data is organized into transport frames, which consist of a 16-bit command word followed by 0 or more data words. The command word provides address and length information to the transport hardware. In a sense, this hardware provides an internal DMA-like function, moving data over the internal bus under host control. Both the GPI and SPI physical layers share a common transport layer.

3.1 Interface Addressing

The transport command word provides address information to the interface hardware.

The host interface address model is based on a paged memory scheme as shown in Figure 4. The command design permits up to 257 pages, with up to 128 offset-addressable 16-bit wide register locations. Therefore, an interface address is composed of an 8-bit page number and a 7-bit register offset. Pages are selected by using a command to write the page register. All data access commands operate on the selected page. One exception is the direct page, which can be accessed at any time without changing the page register.

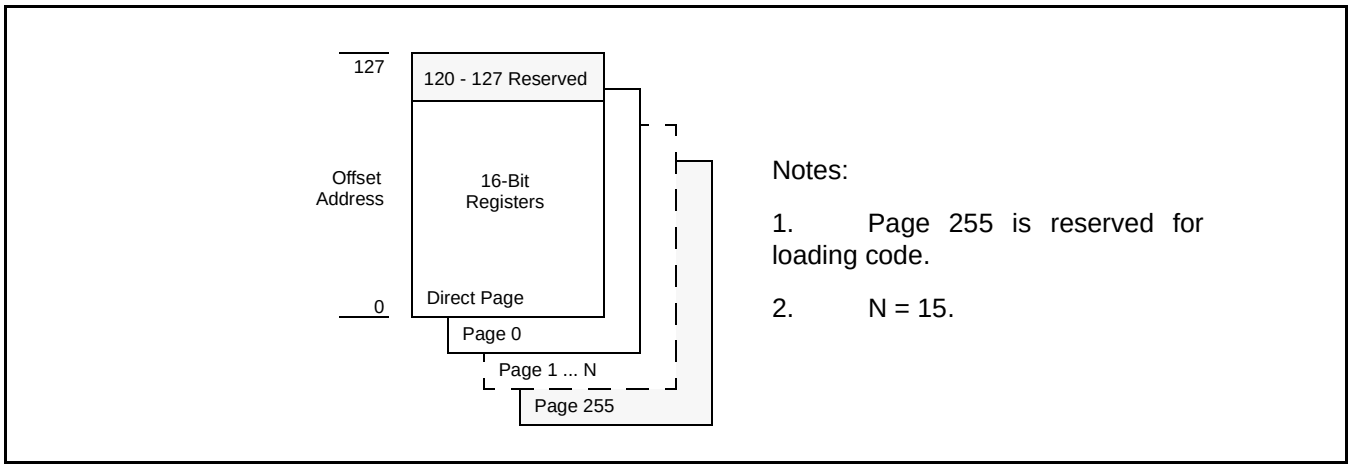


Figure 4 - Host Bus Interface Address Model

3.2 Command Structure

All transport frames start with a 16-bit command word followed by 0 or more 16-bit data words. The same command format is used for both the GPI and the SPI. Table 7 provides a list of transport commands followed by a short description of each command.

Transport Command	Command Bit Position								Number of 16-bit Data Words
	15	14	13	12	11	10	9	8	
	7	6	5	4	3	2	1	0	
Paged Offset Access	0	Offset Address (0 - 127)							Length + 1
	r/w[1]	Length (0 - 127)							
Direct Offset Access	1	Offset Address[2] (0 - 119)							Length + 1
	r/w[1]	Length[2](0 - 119)							
Start Paged Access	1	1	1	1	1	0	0	r/w[1].	Length + 1
	Length (0 - 255)								
Continue Paged Access	1	1	1	1	1	0	1	r/w[1].	Length + 1
	Length (0 - 255)								
Configure Interface	1	1	1	1	1	1	0	1	0
	Interface Option Bits								
Select Page	1	1	1	1	1	1	1	0	0
	Page Number (0 - 255)								
NOP	1	1	1	1	1	1	1	1	0
	1	1	1	1	1	1	1	1	

Table 7 - Host Bus Interface Transport Commands

1. Read/Write select bit. 0 = Read. 1 = Write.
2. Addresses 120 - 127 on the Direct Page are reserved

3.2.1 Paged Offset Access

This command accesses one or more contiguous 16-bit registers on the currently selected page. The 7-bit offset specifies the starting address on the page. The command is followed by (Length + 1) 16-bit data words. The 7-bit Length field allows accessing between 1 and 128 locations with a single transport frame. For nonzero Lengths, the address automatically increments, and consecutive locations are accessed.

3.2.2 Direct Offset Access

Direct Offset Access is the same as Paged Offset Access, except that the direct page is the target. By using this command, the direct page can be accessed at any time without modifying the page register.

3.2.3 Start Paged Access

This command accesses a contiguous stream of 16-bit data words starting from offset 0 on the currently selected page. The command is followed by (Length + 1) 16-bit data words. The 8-bit Length field allows accessing between 1 and 256 locations (i.e. up to 512 bytes) with a single transport frame. Access always begins from offset 0, and the address automatically increments.

3.2.4 Continue Paged Access

Continue Paged Access is the same as the Start Paged Access, except that access starts from where the last paged access left off. By using this command, packets of arbitrary length can be supported. This gives the host the flexibility to split packets transfer into smaller sizes if desired.

3.2.5 Select Page

This command selects the active interface page. It is a write only command and is followed by 0 data words. The 8-bit page field allows up to 256 selectable pages to be defined.

HBI Page Selection (PGSEL) **Command 0xFE (W)**

D7	D6	D5	D4	D3	D2	D1	D0
PG_SEL [7:0]							

PG_SEL: Page addressed by any non-direct HBI access.

3.2.6 Configure Interface

This command is used to configure various physical interface options. It is a write-only command and is followed by 0 data words. The Interface Option Bits field allows the following features to be programmed by the host: Wait Pin Polarity (active High or active Low), Wait Pin Enable (default is tri-state), Wait Pin Drive Mode (open-source/open-drain or TTL), Interrupt Pin Drive Mode (open-drain or TTL), and Endian Control (Big or Little). If this register is not programmed correctly, it is possible that the host may not be able to communicate with the VCP II device properly. This should be part of the HAL (Hardware Abstraction Layer) function used to initialize the device.

HBI User Interface Pin Configuration (PINCONFIG) **Command 0xFD (W)**

D7	D6	D5	D4	D3	D2	D1	D0
RSVD	RSVD	RSVD	INT_DRV	PWAIT_DRV	PWAIT_EN	PWAIT_POL	END_SEL

RSVD: Should be written as 0.

INT_DRV: $\overline{\text{INT}}$ pin drive mode.

0: Open drain (default).
1: TTL.

PWAIT_DRV: PWAIT pin drive mode.

0: CMOS-drive (default). Pin is actively driven to both polarities. When $\overline{\text{PCS}}$ is deasserted (High), the PWAIT pin is driven inactive.
1: Open source or drain depending on polarity. Pin is actively driven to its active polarity as specified by the PWAIT_POL setting. When $\overline{\text{PCS}}$ is deasserted(High), the PWAIT pin is tri-stated.

PWAIT_EN: PWAIT pin enable.

0: Disabled (default).
1: Enabled.

PWAIT_POL: PWAIT pin polarity.

0: Active Low (default).
1: Active High.

END_SEL: Endian select.

0: Big endian (default).

1: Little endian.

Note:

The commands are not affected by endianness; their order must be maintained per documentation. Hence, little-endian systems will need to reverse the command structure.

3.2.7 NOP

A command is reserved to serve as a NOP. Note that all commands except for the Offset Access commands are implemented by reserving an address from the direct page.

3.3 VCP II Direct Page Hardware Register Summary

<Cross-Reference>Table 8 provides an overview listing of the hardware derived registers. These registers reside on the Direct Page.

Register Name	Mnemonic	Register Description	Offset	Notes
Interrupt Indication	INTIND	Used by **`VpGetEvent()`** to get the next event from the queue.	0x00	
Interrupt Parameter	INTPARAM	Used by **`VpGetEvent()`** to get the next event's parameter.	0x01	
Page Offset	PGOFFSET	Allows for interleaved page accesses. Not used by the VP-API.	0x02	
Mailbox Flag	MBFLAG	Used by the VCP II firmware and VP-API to provide page handshaking.	0x03	
Page 255 Checksum (High)	CHKSUM	Checksum of Boot Load data.	0x04	
Page 255 Checksum (Low)			0x05	
Page 255 Base Address (High)	BASE_ADDR	Used for Boot Load.	0x06	
Page 255 Base Address (Low)			0x07	
PCLKB Select	PCLKB_SEL	PCLK A and B Select Register: VCP II defaults to autodetect the PCLK rate.	0x08	
PCLKA Select	PCLKA_SEL		0x09	
Clock Status	CLKSTAT	System Clock status	0x0A	
MCLK Configuration	MCLKCONFIG	Reference Clock configuration	0x0B	
System Real Time Status	SYSSTAT	System Interrupt (fault) status.	0x0C	
System Interrupt Mask	SYSMASK	System Interrupt (fault) mask.	0x0D	
Boot Sense (High)		Boot sense value. It contains the steady state (pulled up or down) values of each GPIO pin as sensed by the Boot Loader.	0x14	These registers are updated by firmware some time after reset
Boot Sense (Low)			0x15	
Reset Type		A 4-bit value indicating the cause of the last System Reset event.	0x16	
Entry Address (High)	ENT_ADDR	Program entry address for an HBI-loaded application. The host application image will write this register before writing the Software Flags register to launch the application correctly.	0x18	
Entry Address (Low)			0x19	

Table 8 - VoiceEdge™ VCP II Hardware Derived Register Space

3.4 Direct Page (Hardware) Registers

This section details each of the VoiceEdge VCP II device registers provided by the hardware or boot firmware. These registers are provided for debugging purposes only. The VP-API has corresponding definitions for their addresses (and bit definitions) and knows how to read/write these registers.

Note:

In all registers, "RSVD" should be written 0 and reads as indeterminate, unless otherwise indicated.

Interrupt Indication (INTIND) **Direct page address 0x00 (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT_SRC	INT_IND[14:8]						
INT_IND[7:0]							

This register reports the source information for the current interrupt. It returns 0x0000 if there is no active interrupt. Reading this register clears the associated interrupt and loads the INTPARAM register with the associated parameter. In most cases the host should read the INTPARAM register after reading this register. This can be accomplished with one multi-word read, since the INTPARAM register immediately follows the INTIND register.

INT_SRC Interrupt source bit.

0: Event queue.
1: System interrupt register.

INT_IND[14:0] Interrupt indication field. The contents of this field depend on the interrupt source bit. If the INT_SRC indicates a system interrupt, each subsequent bit indicates a transition on the corresponding system interrupt status register bit (refer to the SYSINTSTAT register for details). Only unmasked system interrupts will appear in this manner. If INT_SRC is 0, an application specific interrupt is present.

Interrupt Parameter (INTPARAM) **Direct page address 0x01 (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT_PARAM[15:8]							
INT_PARAM[7:0]							

This register returns the parameter for the last interrupt read from the INTIND register. It is updated whenever the INTIND register is read. Reading this register does not change the state of the interrupt hardware.

INT_PARAM[15:0] Interrupt parameter field. The meaning of this field depends on the associated interrupt. System interrupts will mirror the system interrupt status (SYSINTSTAT) register at the time the INTIND read occurred.

Page Offset (PGOFFSET) **Direct page address 0x02 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD						PG_OFFSET[9:8]	
PG_OFFSET[7:0]							

Page Offset contains a pointer to the address of the next transaction into the current mailbox. This register allows interleaved access to a given page. To implement interleaved access, the host must read this register prior to changing the active page. After restoring the active page the host must restore the Page Offset to continue accesses from the previous position with a Continue Page access command. Alternatively, a paged offset access may be used, immediately.

PG_OFFSET[9:0] Address offset of the next access to the currently selected mailbox.

Mailbox Flag (MBFLAG) **Direct page address 0x03 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSP_FLAG	CMD_FLG

This register indicates access rights to the VCP II device's command and response mailboxes corresponding to page 0 and 1 respectively. The VCP II device transfers mailbox control to the host by writing a 0 to the respective bit indicating that the host has access to the corresponding mailbox. The host transfers mailbox control to the VCP II device by writing a 1 to the bit which corresponds to the mailbox to which the host is relinquishing control. Note that the host and the VCP II device can only relinquish control of a mailbox. Neither can request control and it is therefore important that both relinquish control in a reasonably expedient manner.

CMD_FLAG The host sets the Command Mailbox flag by writing a 1 to the associated bit. Writing a 0 to any bit has no affect.

0: Host owns associated mailbox.
1: DSP owns associated mailbox.

RSP_FLAG The host sets the Response Mailbox flag by writing a 1 to the associated bit. Writing a 0 to any bit has no affect.

0: Host owns associated mailbox.
1: DSP owns associated mailbox.

Page 255 Checksum High Register **Direct page address 0x04 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CHKSUM[31:24]							
CHKSUM[23:16]							

Page 255 Checksum Low Register **Direct page address 0x05 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CHKSUM[15:8]							
CHKSUM[7:0]							

This double-word register holds the checksum for any boot operation. The code load integrity is guaranteed by the checksum hardware which resides in this register. This register is used by the VP-API to verify the integrity of a boot load operation.

Page 255 Base Address High Register (BASE255) **Direct page address 0x06 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD	RSVD	BASE_ADDR[29:24]					
BASE_ADDR[23:16]							

Page 255 Base Address Low Register (BASE255) **Direct page address 0x07 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BASE_ADDR[15:8]							
RSVD							

This double-word register is used for code loading. The API uses this register accordingly. The host software needs no further manipulation of this register.

BASE_ADDR[31:8] Upper address bits of Page 255 accesses.

PCLKB Select (PCLKB_SEL) **Direct page address 0x08 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AUTO-DETECTB	AUTO HIWAYBA	FSB_GEN	PCLKB_FREQ[12:8]				
PCLKB_FREQ[7:0]							

PCLKB_SEL is used to configure the PCLKB input to the VCP II, depending on the relationship between FSB (frame sync) and PCLKB.

AUTODETECTB Auto-detected Redundant Highway.

0: Autodetect disabled. PCLKB_FREQ[12:0] should be set by the user.
1: Autodetect the frequency of PCLKB based on the FSB period and store result in PCLKB_FREQ[12:0]. When high the auto detection is restarted and the PCLKB_FREQ field is initialized (default)

AUTO_HIWAYBA Redundant Highway to Highway A Switch.

0: Disable highway automatic switching option.
1: Automatically switch from Redundant Highway to Highway A if CFAIL_PCLKB=1 and CFAIL_PCLKA=0 *(See CLKGEN_STATUS for definition of CFAIL_PCLK)*

FSB_GEN FSB Generation.

0: FSB is provided externally.
1: FSB is generated by the VCP II device at the specified frequency. Whenever this bit is set to High, the AUTODETECTB bit should be set to low by the host software.

PCLKB_FREQ[12:0]: Indicates the set frequency of PCLKB as a multiple of 8KHz -1. When writing AUTODETECTB = 1, the default is restored to these bits 1001011111011 until the auto-detection is complete. PCLKB can be any frequency that is a multiple of 512KHz +/- 6000ppm.

0000000111111:	PCLKB = 512 kHz.
0000010111111:	PCLKB = 1.536 MHz
0000011111111:	PCLKB = 2.048 MHz.
0000111111111:	PCLKB = 4.096 MHz.
0001111111111:	PCLKB = 8.192 MHz.
0011111111111:	PCLKB = 16.384 MHz.
1000100111111:	PCLKB = 35.328 MHz ADSL clock
1001011111011:	PCLKB = 38.880 MHz (default)

Using FSB as an 8-kHz reference, the device will automatically select the correct PCLKB_FREQ value. The initial PCLKB_FREQ[12:0] setting will be 1001011111011 (PCLKB=38.880 MHz). If the FSB or PCLKB pulses are absent, the device will maintain CSEL[12:0] = 1001011111011 until it detects transitions on both the FSB and PCLKB inputs. Automatic frequency detection will occur after 9 consistent FSB periods. Meaning, reading this register before the mentioned 1.125 ms will report the default (0x92FB) PCLKB, not the actual PCLKB frequency.

If FSB is to be generated internally, set FSB_GEN bit to internal generation, set the AUTODETECTB bit to 0 and write the appropriate clock frequency register PCLKB_FREQ[12:0] with the desired value. This can be done in the Hardware Abstraction Layer (HAL) function used to initialize the chip and configure the HBI interface. This should be done before booting the device.

PCLKA Select (PCLKA_SEL) **Direct page address 0x09 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AUTO-DETECTA	AUTO_ HIWAYAB	FSA_GEN	PCLKA_FREQ[12:8]				
PCLKA_FREQ[7:0]							

PCLKA_SEL is used to configure the PCLKA input to the VCP II, depending on the relationship between FSA (frame sync) and PCLKA.

AUTODETECTA Highway A Auto Detect.

0: Autodetect disabled. PCLKA_FREQ[12:0] should be set by the user.
1: Autodetect the frequency of PCLKA based on the FSA period and store result in PCLKA_FREQ[12:0]. When High, the auto detection is restarted and the PCLKA_FREQ field is initialized (default).

AUTO_HIWAYAB Highway A to Redundant Highway Switch.

0: Disable highway automatic switching option.
1: Automatically switch from Highway A to Redundant Highway if CFAIL_PCLKA=1 and CFAIL_PCLKB=0 *(See CLKGEN_STATUS for definition of CFAIL_PCLK)*

FSA_GEN FSA Generation.

0: FSA is provided externally.
1: FSA is generated by the VCP II device at the specified frequency. When ever this bit is set to High. the AUTODETECTA bit should be set to Low.

PCLKA_FREQ[12:0]: Indicates the set frequency of PCLKA as a multiple of 8KHz -1. When writing AUTODETECTA = 1, the default is restored to these bits 1001011111011 until the auto-detection is complete. PCLKA can be any frequency that is a multiple of 512KHz +/- 6000ppm.

0000000111111: PCLKA = 512 kHz.
0000010111111: PCLKA = 1.536 MHz
0000011111111: PCLKA = 2.048 MHz.
0000111111111: PCLKA = 4.096 MHz.
0001111111111: PCLKA = 8.192 MHz.
0011111111111: PCLKA = 16.384 MHz.
1000100111111: PCLKA = 35.328 MHz ADSL clock
1001011111011: PCLKA = 38.880 MHz (default)

Using FSA as an 8-kHz reference, the device will automatically select the correct PCLKA_FREQ value. The initial PCLKA_FREQ[12:0] setting will be 1001011111011 (PCLKA=38.880 MHz). If the FSA or PCLKA pulses are absent, the device will maintain CSEL[12:0] = 1001011111011 until it detects transitions on both the FSA and PCLKA inputs. Automatic frequency detection will occur after 9 consistent FSA periods. Meaning, reading this register before the mentioned 1.125ms will report the default (0x92FB) PCLKA, not the actual PCLKA frequency.

If FSA is to be generated internally, set FSA_GEN bit to internal generation, set the AUTODETECTA bit to 0 and write the appropriate clock frequency register PCLKA_FREQ[12:0] with the desired value. This can be done in the Hardware Abstraction Layer (HAL) function used to initialize the chip and configure the HBI interface. This should be done before booting the device.

Clock Status (CLKSTAT) **Direct page address 0x0A (R/W)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD					CFAIL GLOBAL	CFAIL PCLKB	CFAIL PCLKA
RSVD				POR	RST	WDT	HWRES

CFAIL_GLOBAL:(RO) PLL failure indicator.

0: No Failure
1: PLL failure detected

CFAIL_PCLKA:(RO) PCLKA clock failure indicator.

0: No Failure
1: Clock failure detected

CFAIL_PCLKB:(RO) PCLKB clock failure indicator.

0: No Failure
1: Clock failure detected

POR:(RW) Power up reset indication. This bit is set by a POR event. It can be cleared by writing 0 to it. This bit is cleared by firmware during the boot sequence so that subsequent POR events can be detected. See Table 9.

RST:(R/W) $\overline{\text{RST}}$ reset indication. This bit is cleared by a POR event and set by the $\overline{\text{RST}}$ pin. It can be written by firmware. The $\overline{\text{RST}}$ bit is cleared by firmware during the boot sequence so that subsequent $\overline{\text{RST}}$ events can be detected. See Table 9.

WDT (R/W) WDT_$\overline{\text{OUT}}$ reset indication. This bit is cleared by a POR event and set by the (!RST_N &&!WDT_OUT_N) asserted. The WDT bit is cleared by firmware during the boot sequence so that subsequent WDT events can be detected. See Table 9.

HWRES:(R/W) Hardware reset. Setting this bit causes a full system reset to occur immediately. After the reset sequence, this bit will still hold the last written value. See Table 9.

POR	RST	WDT	HW_ RESET	Notes
x	x	x	0	Hardware induced reset. Follow pin strap options.
0	0	0	1	Host induced reset. Evaluate pin straps and perform full system startup sequence.
0	0	1	1	Reserved
0	1	0	1	Host induced reset. Start previously loaded application without MBIST or Code Loading.
0	1	1	1	Host induced reset. Reserved.
1	x	x	1	

Table 9 - CLKGEN Status Hardware Reset Controls

Note: CLKSTAT should only be written to cause a hardware reset. Any other write is illegal.

MCLK Configuration (MCLKCONFIG) **Direct page address 0x0B (R/W)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD		CURRENT _HIWAY	REFCLK_FREQ[12:8]				
REFCLK_FREQ[7:0]							

CURRENT_HIWAY:(RW) Currently active PCM highway. This bit is writable but may be modified by hardware if either AUTO_HIWAY bit (*in PCLKA_SEL, address 0x09*) is asserted and a clock failure is present on the appropriate PCLK/FS pair.

0: Highway A. (Default)
1: Highway B.

REFCLK_FREQ:(RO) Indicates the frequency of the selected PLL source clock. The field is read only and the frequency should be programmed in the appropriate PCLKx_SEL register (x =A or B). The frequency is specified as a: (multiple of 8000) - 1.

Note: The power-up default for the 16-bit portion of this register is 0x12FB.

System Real Time Status (SYSSTAT) **Direct page address 0x0C (RO)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	EV_OV	WDT	CFAIL_ GLOBAL	CFAIL_ PCLKA	CFAIL_ PCLKB	SYS_FLAG[9:8]	
SYS_FLAG[7:0]							

This read only register allows the host to determine the present status of the system faults. It differs from the INTPARAM register in that no interrupt is required to determine the system fault status.

EV_OV Event queue overflow detected. This bit indicates that an event was lost due to event queue overflow. If events are being serviced and generated at the same time it is possible that this flag will be set multiple times. This bit must be cleared by reading INTIND, if the bit is unmasked, or by reading SYSSTAT if it is masked.

WDT Watchdog timer timeout occurred. (default =0) This bit is asserted when the WDT_OUT pin is driven low if a system reset is not induced by that action.This bit must be cleared by reading INTIND, if the bit is unmasked, or by reading SYSSTAT if it is masked.

CFAIL_GLOBAL PLL or selected source Clock Fail status. (default =1)

CFAIL_PCLKA PCLKA/FSA Clock Fail status. (default =1)

CFAIL_PCLKB PCLKB/FSB Clock Fail status. (default =1)

SYS_FLAG[9:0] Software configurable system interrupt real time status bit.

0: The status of the bit is not set (default).
1: When asserted, each bit masks the interrupt caused by a transition on the respective SYS_FLAG bit of the SYSSTAT register. The application software will define the meaning of these bits as needed.

System Interrupt Mask (SYSMASK) **Direct page address 0x0D (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EVENT_ DELAY	MOVL	MWDT	MCFAIL_ GLOBAL	MCFAIL_ PCLKA	MCFAIL_ PCLKB	MSYS_FLAG[9:8]	
MSYS_FLAG[7:0]							

This register is used to mask system interrupt sources. There is a one to one correspondence between the bit definitions in SYSMASK and INTIND when INTIND represents a system interrupt.

EVENT_DELAY: Event delay bit

0: Low priority event queue (two, three) interrupts are reported to the host by asserting the $\overline{INT}$ pin whenever an event is present in those queues. (default)
1: Low priority event queue (two, three) interrupts cannot pull the $\overline{INT}$ pin low or output events unless a system interrupt or high priority event queue one interrupt was first present to assert the $\overline{INT}$ pin. This feature allows fewer host interruption from the lower priority events.

MOVL: Interrupt Queue Overflow mask. When asserted the interrupt is masked. (Default = 1). If this bit is asserted (masked), the SYSSTAT must be read to clear the OVL status. Otherwise, if the OVL is unmasked, a read of the INTIND clears the OVL status bit.

MWDT: Watch Dog Timer mask. When asserted the interrupt is masked (default = 1). If this bit is asserted (masked), the SYSSTAT must be read to clear the WDT status. Otherwise, if the WDT is unmasked, a read of INTIND clears the WDT status bit.

MCFAIL GLOBAL: PLL or selected source Clock Fail mask. When asserted the interrupt is masked. (default = 1)

MCFAIL PCLKA: PCLKA/FSA Clock Fail mask. When asserted the interrupt is masked. (default = 1)

MCFAIL PCLKB: PCLKB/FSB Clock Fail mask. When asserted the interrupt is masked. (default = 1)

MSYS_FLAG[9:0]: Software configurable system interrupt mask bit. When asserted the interrupt is masked. (default = 1)

Boot Sense [GPIO31:16] **Direct page address 0x14 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
GPIO[31]	GPIO[30]	GPIO[29]	GPIO[28]	GPIO[27]	GPIO[26]	GPIO[25]	GPIO[24]
GPIO[23]	GPIO[22]	GPIO[21]	GPIO[20]	GPIO[19]	GPIO[18]	GPIO[17]	GPIO[16]

GPIO[31:16]: Reset GPIO input value.

Boot Sense [GPIO15:0] **Direct page address 0x15 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
GPIO[15]	GPIO[14]	GPIO[13]	GPIO[12]	GPIO[11]	GPIO[10]	GPIO[9]	GPIO[8]
GPIO[7]	GPIO[6]	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]

GPIO[15:0]: Reset GPIO input value.

Reset Type **Direct page address 0x16 (R)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSVD							
RSVD				POR	RST	WDT	HWRES

A four-bit value indicating the cause of the last System Reset event. The Boot Loader copies CLKSTAT [19:16] into the low nibble of this register. See Table 12 for interpretation of these bits.

Entry Address High Register **Direct page address 0x18 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENT_ADDR [31:24]							
ENT_ADDR [23:16]							

Entry Address Low Register **Direct page address 0x19 (RW)**

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENT_ADDR [15:8]							
ENT_ADDR [7:0]							

Program entry address for an HBI-loaded application. The host application image will write this double-word register before writing the Software Flags register to launch the application correctly.

3.5 Code Loading

The VCP II device will always come up in Boot mode following a power-on reset or when the reset pin of the chip is deasserted. The DSP will delay program execution until the boot sequence is completed as defined by the pin strapping. The VCP II device contains an on-chip ROM with initial startup code, a simple ROM monitor, and a boot loader. Before the ROM monitor runs, initial startup code is run to perform system diagnostics. The diagnostics consist of evaluating the GPIO[31:24] boot strap pins, testing for a stable system clock and testing/repairing the device's internal RAM if so configured. The evaluation of the GPIO[31:24] is accomplished by a crude software delay of at least 200 µs, and then polling the state of those pins. The clock failure may take significant time to disappear due to waiting for autodetection or a host write.

Pin	Boot Sense Function	Description
GPIO31 ($\overline{\text{MCS15}}$)	SLOW_SPEED	0: Write the PLL to the maximum frequency(140 MHz). 1: Do not adjust the PLLDIV field(98.304 MHz).
GPIO30 ($\overline{\text{MCS14}}$)	CFAIL_SKIP	0: Wait for CFAIL before proceeding with BOOT routine. 1: Do not wait for CFAIL before proceeding.
GPIO29 ($\overline{\text{MCS13}}$)	BIST_DISABLE	0: Enable Memory BIST/Repair in BOOT routine. 1: Disable Memory BIST/Repair in BOOT routine.
GPIO28 ($\overline{\text{MCS12}}$)	BOOT_DEBUG	0: Do not enter debug mode. 1: Enter debug mode after Memory BIST if enabled.
GPIO27 ($\overline{\text{MCS11}}$)	UART_ENABLE	0: Disable UART CLI during booting. 1: Enable UART CLI during booting.
GPIO26 ($\overline{\text{MCS10}}$)	GPIO_MESSAGES	0: Disable GPIO messages during booting. 1: Enable GPIO messages during booting.
GPIO25 ($\overline{\text{MCS9}}$)	RSVD	
GPIO24 ($\overline{\text{MCS8}}$)	RSVD	

Table 10 - Boot Sense Pin Definitions

3.6 Host Boot Procedure

The download code will be composed of a sequence of words that must be presented to the device via the GPI/SPI. These images can be broken up at 128-byte boundaries if needed. The first byte of the sequence (or after a break in the sequence of 128 blocks) must have the PADDR signal asserted. Any Zarlink provided image will conclude with the Page 255 Checksum register returning the value AA55 AA55. This register should be verified by the Host before proceeding.

4.0 Application Layer

The application layer defines the programmer's interface and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the programmer's interface can change by providing new software. The primary elements of the model are system registers, mailbox buffers and an event queue. The following sections describe these elements in more detail.

4.1 Software (Application Derived) Registers

The remainder of the registers defined in the HBI register space are application defined registers. For detailed information on these registers, refer to the *VoicePath API II Reference Guide for VCP II Devices*.

4.1.1 Mailboxes Buffers

Mailbox buffers are composed of a dedicated interface page and an associated hardware semaphore flag to control ownership. Mailbox buffers pass information in one direction only. The host writes to a downstream mailbox and reads from an upstream mailbox. The reverse is true for the DSP. The flag indicates mailbox status and guards against race conditions.

All mailbox flags are located in the 16-bit software flag register implemented on the direct page. They exhibit the following characteristics. Only the host can set a mailbox flag. Likewise, only the DSP can clear a mailbox flag. High-to-low transitions generate a maskable interrupt towards the host. Low-to-high transitions generate a maskable interrupt towards the DSP.

The following steps illustrate how a mailbox is used to pass information in the downstream (i.e. host-to-DSP) direction. For an upstream exchange, roles are simply reversed.

1. The host waits for the appropriate mailbox flag to go low, indicating that the mailbox is now empty. To do this, the host can either poll the mailbox flag register, or unmask the associated interrupt and wait for an interrupt to be generated.
2. The host selects the mailbox by issuing a Select Page command.
3. The host writes data into the mailbox using either the Paged Offset or Paged Access commands. Data can be written with one command or with several. The first location of the mailbox is used to indicate the length of the data being passed to the DSP. The host is responsible for writing this length value.
4. When the host is finished writing data to the mailbox, it then sets the associated mailbox flag by writing a one to the appropriate bit in the mailbox flag register. This indicates to the DSP that data is waiting in the mailbox, and ownership has passed to the DSP.
5. The DSP either polls the mailbox flag register, or receives an interrupt indicating data is available.
6. The DSP reads and processes the contents of the mailbox taking any required actions. It reads the first location in the mailbox to determine the length of the data.
7. The DSP clears the associated mailbox flag, indicating to the host that it is finished processing and passing ownership back to the host.

4.1.2 Command/Response Mailboxes

This mailbox pair provides a channel for exchanging command and status messages with the host. Refer to the VP-API code for commands. The command mailbox is for the host to write commands. The response mailbox is for the DSP to report the results of read commands or confirmation of write commands.

4.1.3 Event Queue

A key element of the host interface is an event queue. Events relay asynchronous information back to the host. Buffering events in a queue gives the host flexibility on when to read them, and ensures that no events are lost if the host is unable to service them immediately.

The host reads the event queue through the interrupt indication and parameter registers. Events are composed of a 16-bit indication value that includes channel and event type fields, and an optional 16-bit parameter. Several of the Le79114 VCP II events require a 32-bit timestamp. The timestamp can be reduced to 16-bits by creating a timestamp rollover event, and letting the host maintain the upper 16-bits. An event reports the lower 16-bits of the timestamp in the parameter register. (See the *VP-API II User's Guide* for information on an event associated with a timestamp).

5.0 Physical Layer

The physical layer provides both parallel and synchronous serial interfaces. These are described in the following sections.

5.1 General Purpose Parallel Interface (GPI)

The General Purpose Parallel Interface (GPI) is an external interface of the VCP II device that is used to communicate command information and data to/from an external host processor. The GPI has several configuration options and has been architected to connect gluelessly to a variety of external processors. Options are selected via the configuration pins, refer to Table 11. The GPI interface uses a combination of write, read, data, address, and wait strobes; thus, a dedicated clock is not needed to synchronize the transfers. The structure of the commands and data both take the form of a command word followed by data in order to preserve the same logical view as the Serial Peripheral Interface (SPI). This allows the host to issue the same commands to a VCP II device regardless of the physical interface.

5.1.1 GPI External Pin List

The pins related to the GPI are described below. Pins associated with clocks, reset, or interrupts are described in another section

Pin Name	Type	Reset	Description
$\overline{\text{PCS}}$	Input		GPI Chip Select (active Low)
PADDR	Input		GPI Address Pin (Command or Data Indicator)
PWAIT	Output/Z	Z	GPI Wait (Programmable polarity and drive mode, external pull-inactive required)
PD[15:0] (PD[7:0])	Input/Output/ Z	Z	GPI Data Bus. Alternate configuration as 8-bit Data Bus.
$\overline{\text{PWR}}$ (PDS)	Input		GPI Write Strobe (active Low). Alternate configuration as GPI Data Strobe (active Low)
$\overline{\text{PRD}}$ (PRD/$\overline{\text{WR}}$)	Input		GPI Read Strobe (active Low). Alternate configuration as GPI Read/Write Strobe (Read=High, Write=Low)

Table 11 - GPI Pins

Note:

Z = No state driven, high impedance.

5.1.2 GPI Features

The GPI has been designed to connect to a variety of external host processors. The capabilities of the GPI are enumerated below.

1. Commands and data can be transferred across the parallel interface using either separate read and write strobes or using a combined read/write strobe and a data strobe.
2. The GPI can be configured for either 8-bit or 16-bit data bus transfers.
3. A wait strobe can be used to indicate to the external processor that the interface is available for a transfer. When the wait strobe goes active, the interface is busy. The transfer will complete after the wait signal deasserts. The wait strobe pin polarity is programmable and defaults to tri-state. Note: an external pull-up or pull-down (depending on the programmed active state) is required.
4. Data byte swap allows the GPI to support big and little endian systems. (Note that the command is always evaluated as big endian, so little endian systems should byte swap the command word accordingly).

5. A read status register is available to the external processor by performing a read while the address pin is High. The contents of this register contains a wait status indication, which can be used by external processors that do not support the wait pin.

Parallel Interface Status (GPISTATUS) (RO)

D15	D14	D13	D12	D11	D10	D9	D8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PAGENUM							
RSVD	RSVD	RSVD	RSVD	RSVD	CMD_PROG	INT	PWAIT

Read GPISTATUS with PADDR High.

PAGENUM: Current active page

CMDPROG: Command in progress.

INT: $\overline{\text{INT}}$ logic state.

PWAIT: PWAIT logic state.

6. The address pin is used as a command word demarcation. The command interface is reset during a write operation when the address pin is High. (Note that the command interface is not reset during a read operation when the address pin is High.) This ensures that the command and data sequences between the external processor and the VCP II device will be interpreted properly. If a previous command has completed, the next word will be interpreted as a command regardless of PADDR. Refer to Table 12 for a list of the GPI access modes.

Address	Read or $\overline{\text{Write}}$	Access Type
0	0	write data
0	1	read data
1	0	write command
1	1	read status

Table 12 - GPI Interface Access Types

5.1.3 GPI Connections to an External Host

The GPI has several configuration options and has been architected to connect gluelessly to a variety of external processors. The GPI interface uses a combination of write, read, data, address, and wait strobes; thus, a dedicated clock is not needed to synchronize the transfers.

The GPI can be configured for either 8-bit or 16-bit data bus transfers. Commands and data can be transferred across the parallel interface using either separate read and write strobes or using a combined read/write strobe and a data strobe.

A wait strobe can be used to indicate to the external processor that the interface is available for a transfer. When the wait strobe goes active, the interface is busy. The transfer will complete after the wait signal deasserts. The wait strobe pin polarity is programmable and defaults to tri-state. Note: an external pull-up or pull-down (depending on the programmed active state) is required.

The external interface connection diagrams for the four different GPI configurations are shown in Figure 5 through Figure 8.

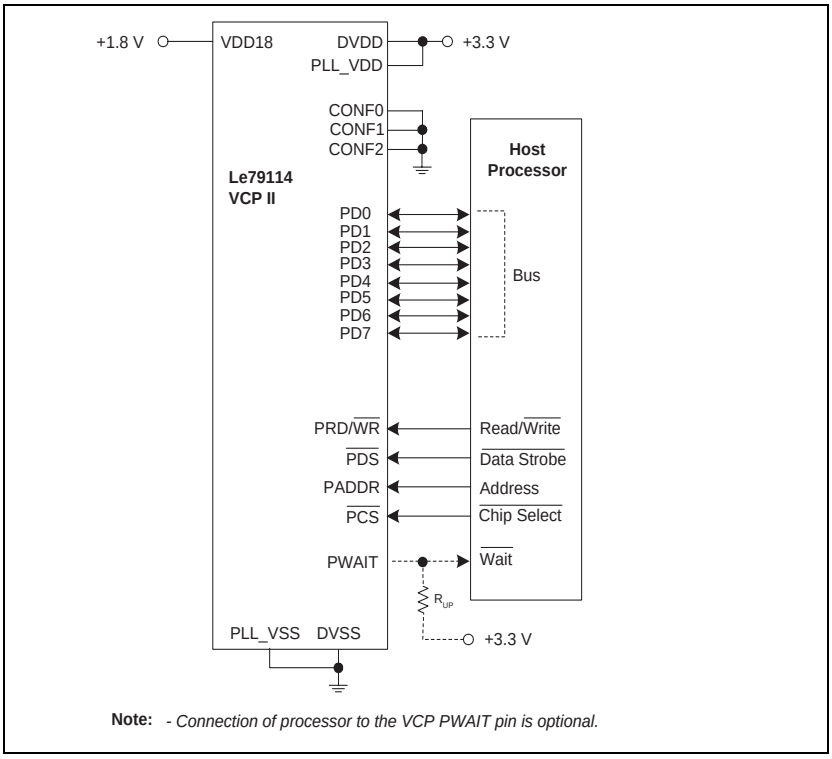


Figure 5 - GPI - 8-bit Parallel Control, Combined Read/Write and Data Strobe

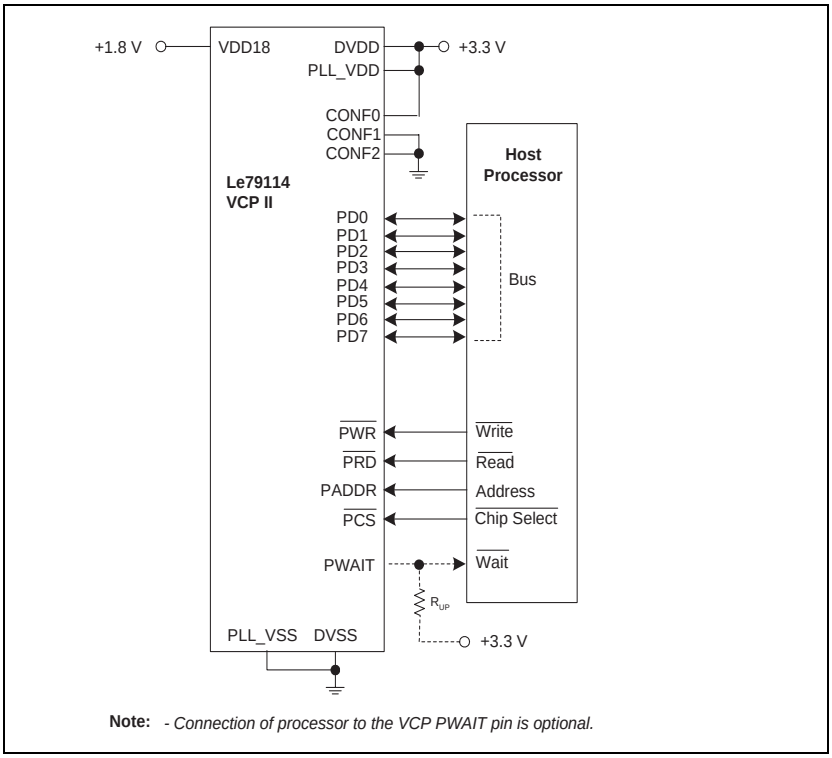


Figure 6 - GPI - 8-bit Parallel Control, Separate Read and Write Strobes

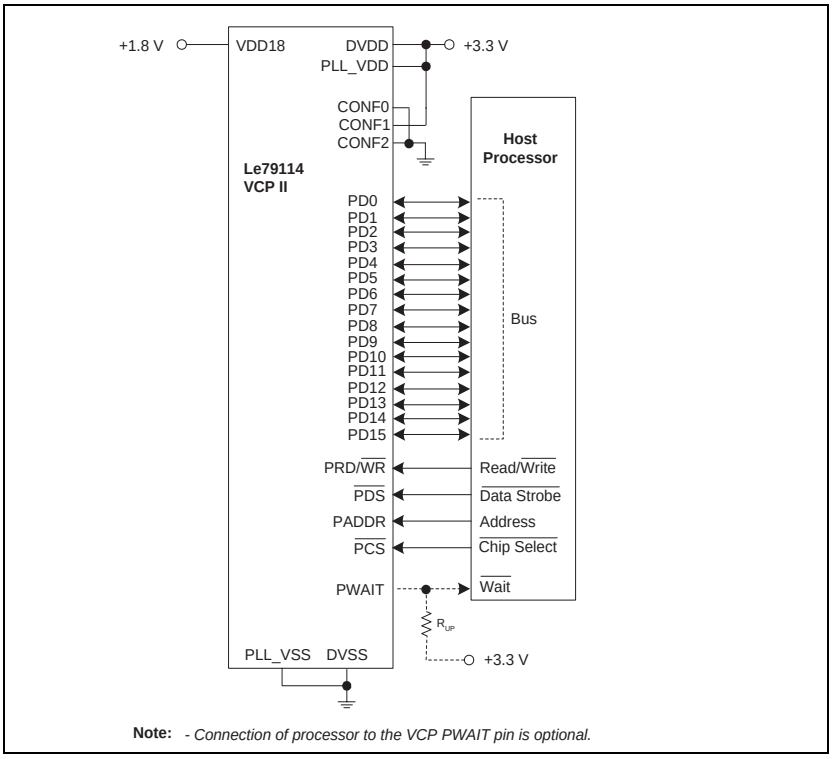


Figure 7 - GPI - 16-bit Parallel Control, Combined Read/Write and Data Strobe

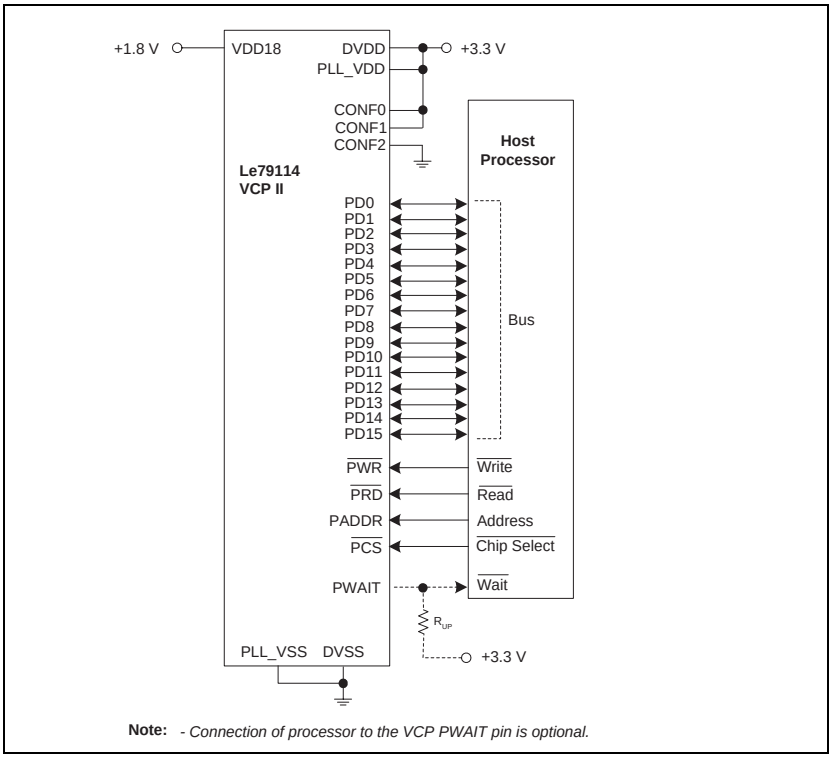


Figure 8 - GPI - 16-bit Parallel Control, Separate Read and Write Strobes

5.1.4 GPI Timing Requirements

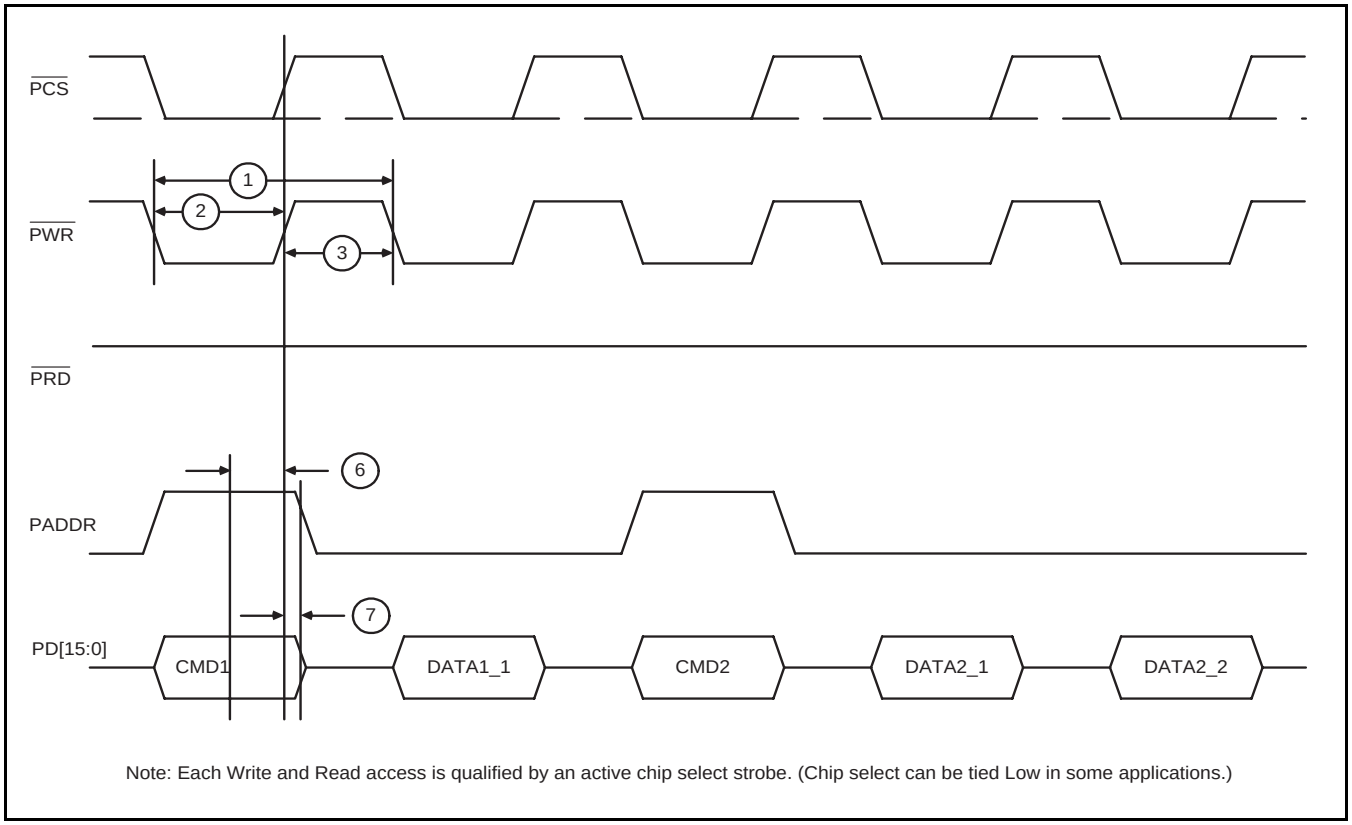
The timing requirements for read and write accesses are shown in the following timing diagrams. The PWAIT waveform on the read diagrams is shown as a dotted line because the wait strobe feature is optional and would only go active if the read data was not yet valid following a read command. Also, although the wait strobe polarity is programmable, it is shown as active Low in several of the timing diagrams. Each write and read access is qualified by an active chip select signal. In some applications, the chip select pin could be tied Low. The 16-bit accesses using separate read and write strobes is shown in Figure 9 and Figure 10. The 8-bit accesses using separate read and write strobes are shown in Figure 11 and Figure 12. The timing information for the 8 and 16-bit figures using separate read and write strobes can be found in <Cross-Reference>Table . The 8-bit accesses using a combined read/write strobe and a data strobe is shown in Figure 13 and Figure 14. The timing information for the 8 and 16-bit figures using a combined read/write strobe and a data strobe can be found in Table 13. Refer to Figure 15 for an example of the read status register access (which applies to both 8 and 16-bit modes). It should be noted that if the host is using the wait strobe feature and issues a read command, that performing a status read operation immediately after the writing of a read command and before the actual read of the first byte/word of data would cause the read status access to be extended. Refer to Figure 16 for an example of the byte swap operation on the data word (which also applies to 8 and 16-bit modes).

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{ACC}	Access period (from Write to Write or Read to Read or Read to Write)	100	—	—	ns	
2	t_{ON}	Pulse width LOW ($\overline{PCS}$ or $\overline{PWR}$ or $\overline{PRD}$)	35	—	—		
3	t_{OFF}	Pulse width HIGH ($\overline{PCS}$ & $\overline{PWR}$ or $\overline{PCS}$ & $\overline{PRD}$)	10	—	—		
4	t_{WR_RDV}	Write to Read (rising $\overline{PWR}$ to Data output valid)	25	—	270		3,4
5	t_{RD_DV}	$\overline{PCS}$, PADDR, $\overline{PRD}$ active to Data output valid	—	—	25		3
6	t_{SU_IN}	Address, Data input setup time to rising $\overline{PCS}$ or $\overline{PWR}$	15	—	—		
7	t_{HOLD_IN}	Address, Data input hold time after rising $\overline{PWR}$ or $\overline{PCS}$	0	—	—		
8	t_{HOLD_OUT}	Data output hold time after rising $\overline{PRD}$ or $\overline{PCS}$	0	—	10		3
9	t_{CS_WAIT}	Chip Select active to Wait active	—	—	25		2,3
10	t_{WAIT}	Wait strobe width LOW when $\overline{PCS}$ is active	0	80	280		2,3
11	t_{WAIT_DV}	PWAIT deserted to Data valid	—	—	0		2

Table 13 - GPI Bus Timing Parameters for Separate Read and Write Strobes[1]

Notes:

1. *Refer to Figure for timing diagram test points.*
2. *The Wait Strobe active edge may occur as early as the rising Write Strobe signal if Chip Select is held active.*
3. *The pin load is assumed to be C_{load} = 75pF.*
4. *This is the time between the read command and the first data word. If PWAIT is not used, then the maximum value must be met by the host. If PWAIT is used, faster transactions can occur.*



Note: Each Write and Read access is qualified by an active chip select strobe. (Chip select can be tied Low in some applications.)

Figure 9 - GPI 16-Bit Write Access Using Separate Read and Write Strobes

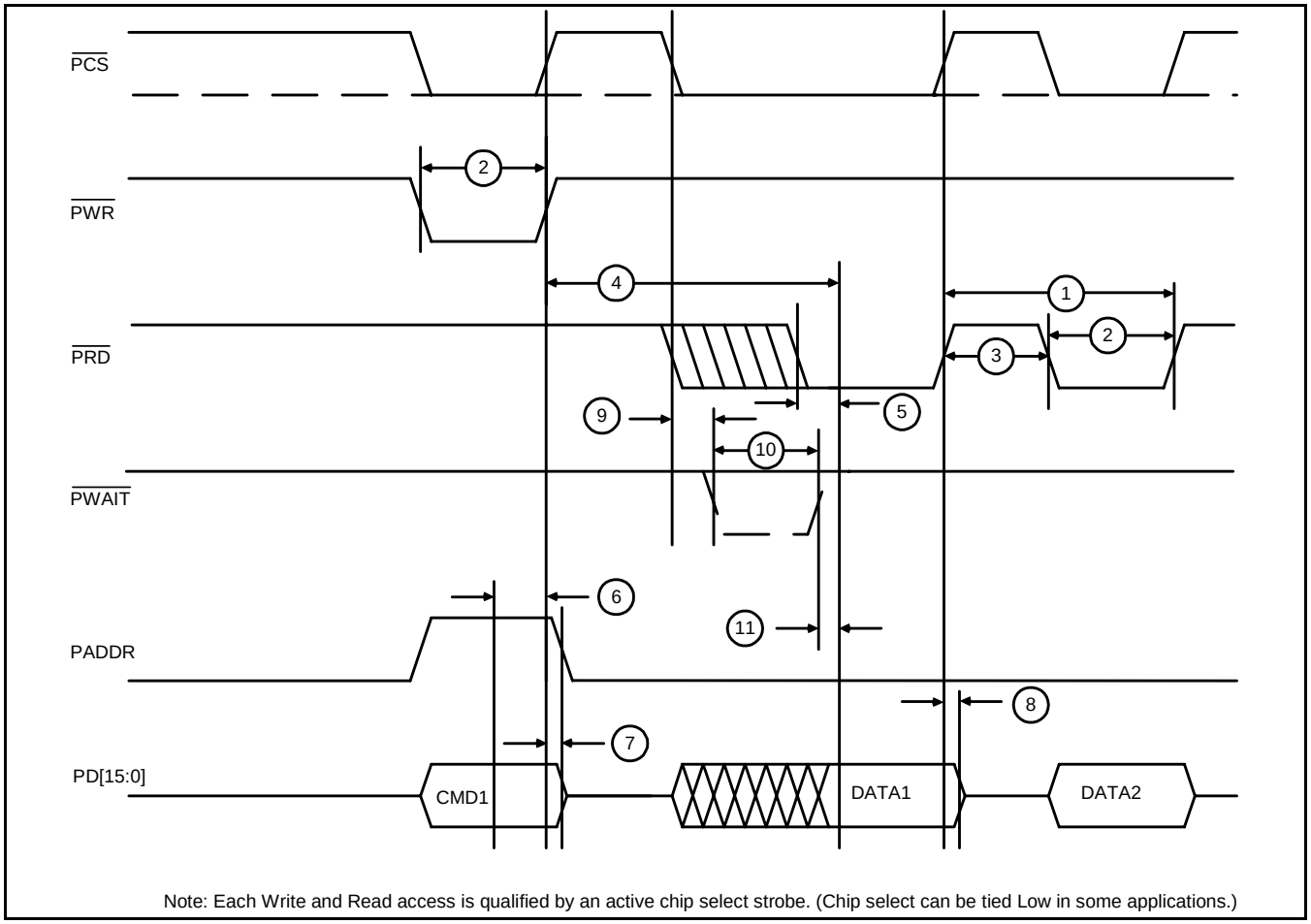


Figure 10 - GPI 16-Bit Read Access Using Separate Read and Write Strobes

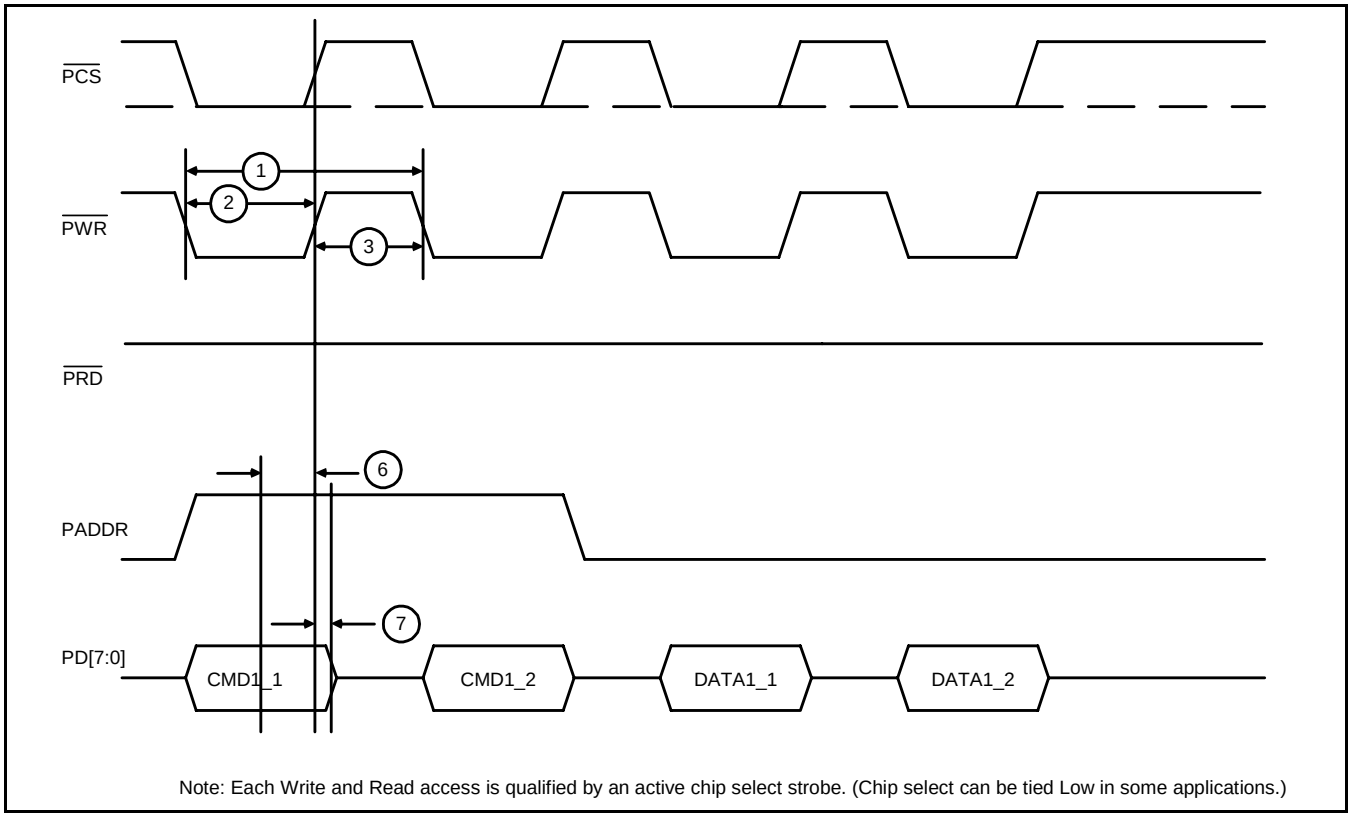


Figure 11 - GPI 8-Bit Write Access Using Separate Read and Write Strobes

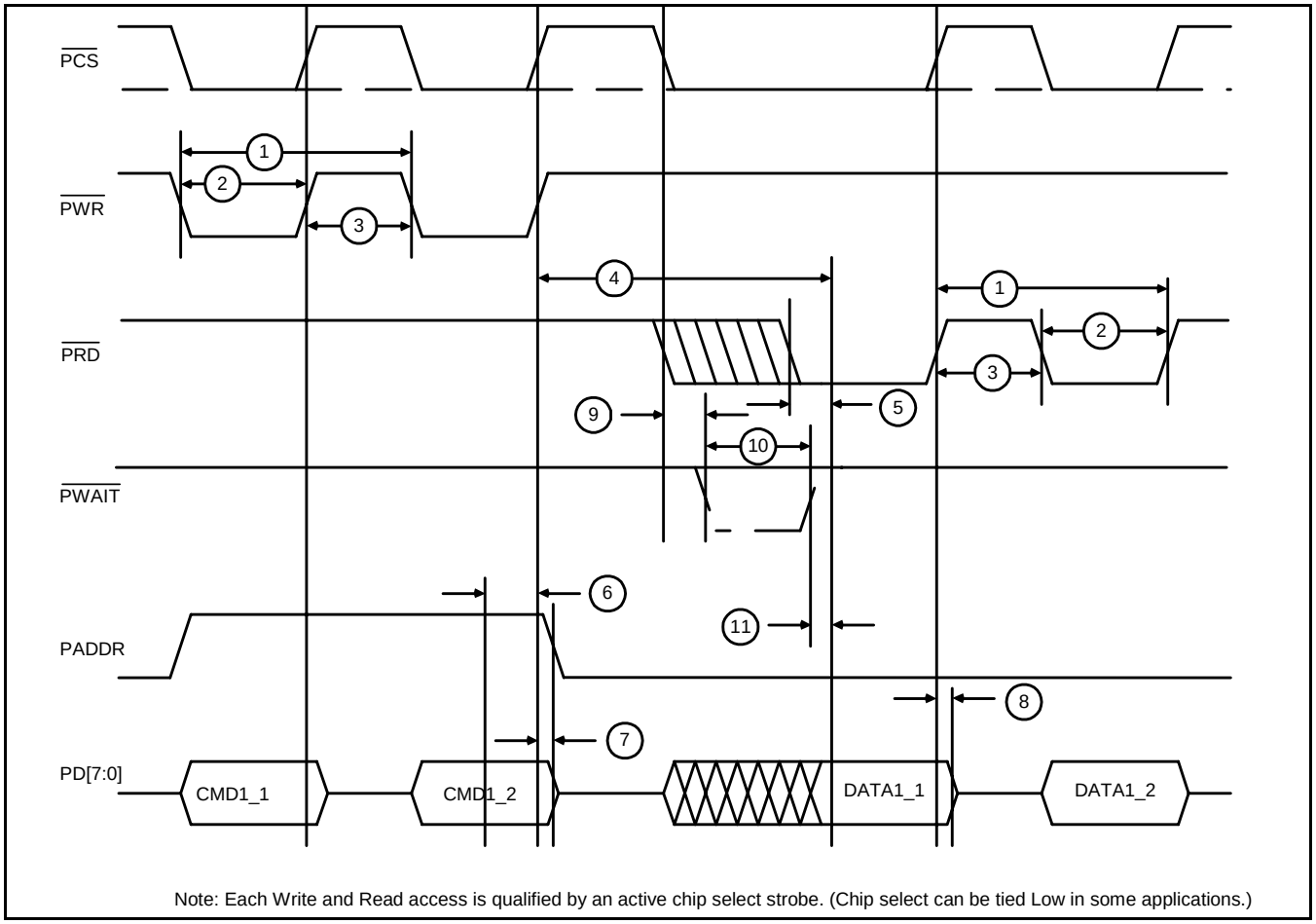


Figure 12 - GPI 8-Bit Read Access Using Separate Read and Write Strobes

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{ACC}	Access period (from Write to Write or Read to Read or Read to Write)	100	—	—	ns	
2	t_{ON}	Pulse width LOW ($\overline{PCS}$ or PRD/$\overline{WR}$ or $\overline{PDS}$)	35	—	—		
3	t_{OFF}	Pulse width HIGH ($\overline{PCS}$ & PRD/$\overline{WR}$ & $\overline{PDS}$ or $\overline{PCS}$ & $\overline{PDS}$)	10	—	—		
4	t_{WR_RDV}	Write to Read (rising PRD/$\overline{WR}$ to Data output valid)	25	—	270		3,4
5	t_{RD_DV}	$\overline{PCS}$, PADDR, PRD/$\overline{WR}$ active to Data output valid	—	—	25		3
6	t_{SU_IN}	Address, Data input setup time to rising $\overline{PCS}$ or PRD/$\overline{WR}$ or $\overline{PDS}$	15	—	—		
7	t_{HOLD_IN}	Address, Data input hold time after rising PRD/$\overline{WR}$ or $\overline{PDS}$ or $\overline{PCS}$	0	—	—		
8	t_{HOLD_OUT}	Data output hold time after rising $\overline{PDS}$ or $\overline{PCS}$	0	—	10		3
9	t_{CS_WAIT}	Chip Select active to Wait active	—	—	25		2,3
10	t_{WAIT}	Wait strobe active width when $\overline{PCS}$ is active	0	80	280		2,3
11	t_{WAIT_DV}	PWAIT deserted to Data valid	—	—	0		2

Table 14 - GPI Bus Timing Parameters for Combined Read/Write and Data Strobes[1]

Note:

1. *Refer to Figure for timing diagram test points.*
2. *The Wait Strobe active edge may occur as early as the rising Write Strobe signal if Chip Select is held active.*
3. *The pin load is assumed to be C_{load} = 75pF.*
4. *This is the time between the read command and the first data word. If PWAIT is not used, then the maximum value must be met by the host. If PWAIT is used, faster transactions can occur.*

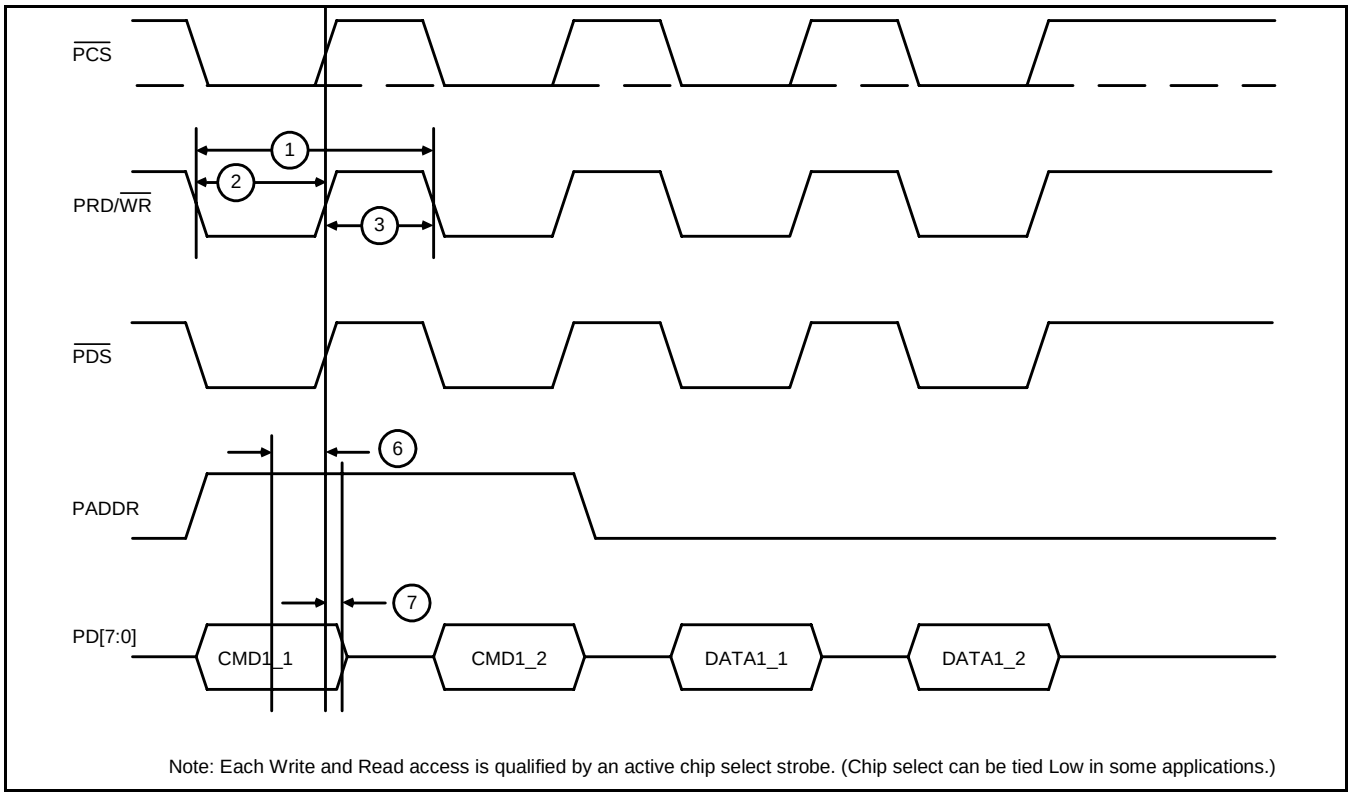


Figure 13 - GPI 8-Bit Write Access Using Combined Read/Write and Data Strobes

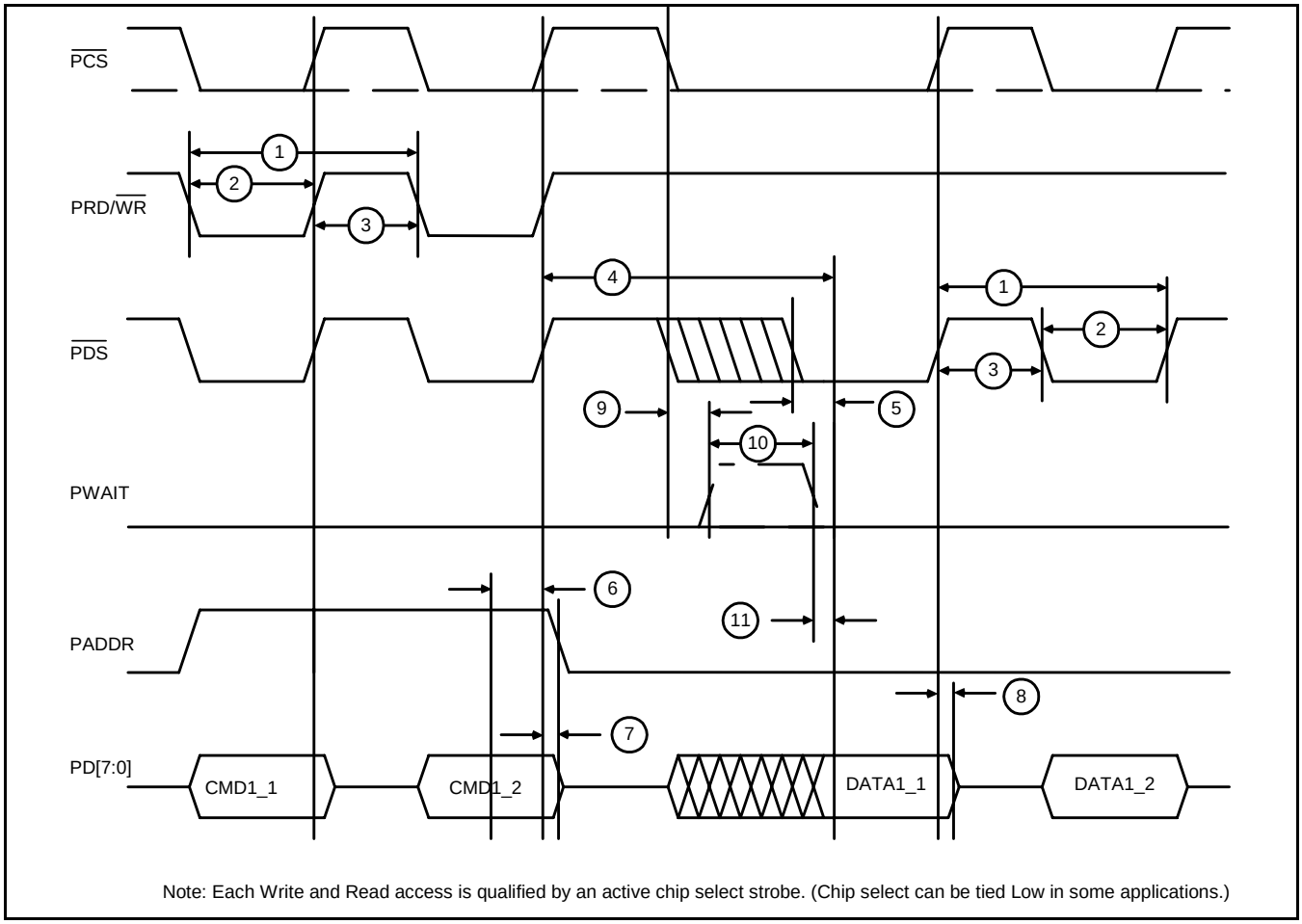


Figure 14 - GPI 8-Bit Read Access Using Combined Read/Write and Data Strobes

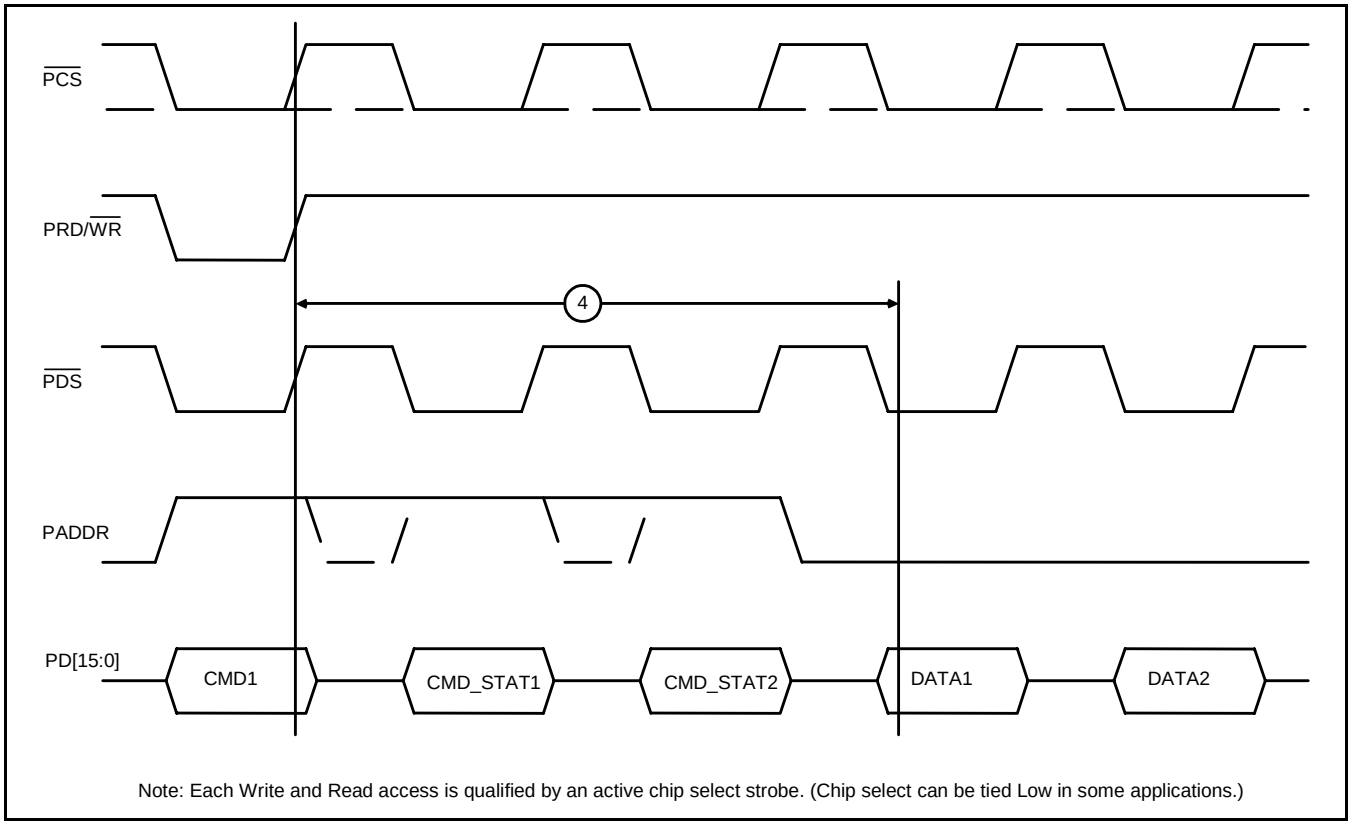


Figure 15 - GPI Read Status Register Access

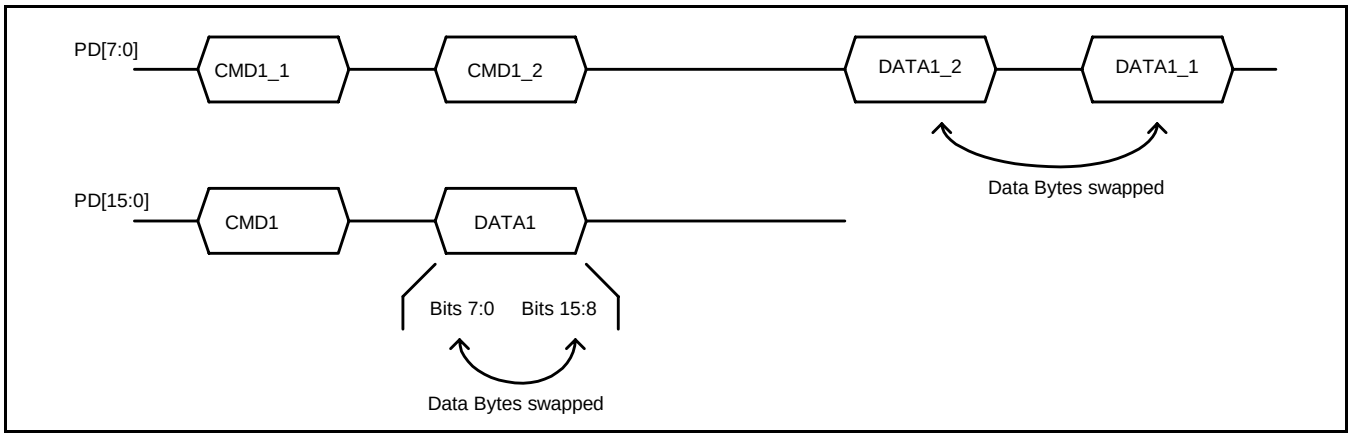


Figure 16 - GPI Data Byte Swap Access

5.2 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) is a physical interface of the VCP II device used by the external host to communicate with the device. The SPI interface is compatible with the SPI interface used by general DSPs, so that those chips can interface with the VCP II device without any glue logic. Because the SPI has the same logical view as the General Purpose Parallel Interface (GPI), the host can issue the same commands or data to the VCP II device regardless of the physical interface.

The most important factor with regards to the ability to use the SPI interface is not the clock speed or number of lines, but the host architecture. Required is a queued SPI with task resume capability and the host application broken into enough threads to allow for the SPI to not bottleneck or stall the network processor. Zarlink strongly recommends the GPI 16-bit architecture. If the SPI architecture is chosen, it is the responsibility of the software designer to correctly architect the host firmware.

5.2.1 SPI External Pins Connection

The SPI is a 4-wire synchronized serial interface used in many DSPs and microcontrollers. The data is transferred bi-directional from master to slave and from slave to master. The master provides clock SCK to synchronize the data transfer, and the signals MOSI and MISO are for the data bit stream. SPI master can be a 3-wire or 4-wire SPI master, depending on if the master drives the $\overline{SS}$ signal. A 4-wire SPI master pulls $\overline{SS}$ Low when transferring data. In a single master/slave pair the master can be a 3-wire interface, with the $\overline{SS}$ pin at the slave tied Low.

Signal Name	Type	Description
SCK	Input	SPI clock
MOSI	Input	SPI slave input/master output
MISO	Output	SPI slave output/master input
$\overline{SS}$	Input	SPI Slave select low

Table 15 - SPI Signals

The VCP II device will be the SPI slave, and the external host will be the SPI master. Signal MOSI will connect to the SI pin and signal MISO will connect to the SO pin of the VCP II device. Zarlink VCP II devices sample the input signal SI on the rising edge of the clock and change the output signal SO on the falling edge of the clock.

A 4-wire serial interface is shown in Figure 17. If the host processor does not provide a slave select and only one VCP II device is used, simply tie VCP II $\overline{SS}$ to ground.

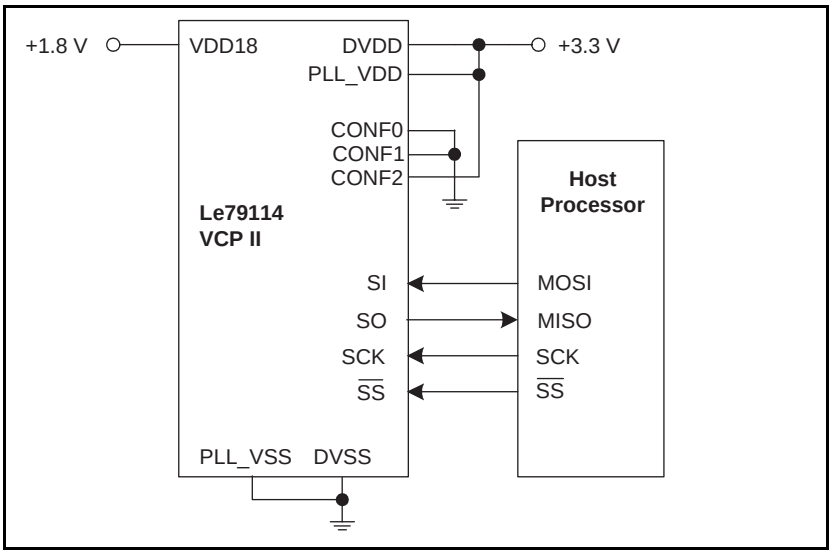


Figure 17 - SPI - 4-Wire Master-Slave Connections

5.2.2 SPI Features

- In order to connect to different SPI masters and share the same logic view with the General Purpose Parallel Interface, the SPI slave of the VCP II device has the following designs:
- Separate SI and SO pins.
- No read latency: no latency between the read command word and the first data word.
- Data byte swap is supported.
- $\overline{SS}$ pin supports byte/word framing, and command framing mode, as shown in Figure . The SPI slave state machine will reset if $\overline{SS}$ returns to High when the number of active SCK clocks is not equal to 8 or 16. If there is no clock, $\overline{SS}$ has to be Low for more than 125 ns to be recognized to reset SPI slave state machine. In command framing mode, the transition of $\overline{SS}$ to High means the command has ended. This event resets the SPI slave state machine, and the next falling edge of $\overline{SS}$ starts a new command.

Figure 18 shows three kinds of framing modes based on the behavior of $\overline{SS}$. In byte/word framing mode, $\overline{SS}$ is Low for 8/16 SCK clocks. For a two-word command, $\overline{SS}$ needs to toggle 4/2 times to complete the command transfer. In command framing mode, $\overline{SS}$ is Low for the whole duration of the command transfer. When the command is finished, $\overline{SS}$ will go back to High. If $\overline{SS}$ Low lasts shorter than the expected command length, the command is aborted and the SPI slave state machine resets. However, if the user pulls $\overline{SS}$ Low longer than the expected command length, the extra words will start a new command sequence. In both word framing mode and command framing mode, SCK can be free-running or absent when $\overline{SS}$ is inactive High.

Every time $\overline{SS}$ returns to High and the number of active SCK clocks is not equal to 8 or 16, the SPI slave state machine will reset. The next $\overline{SS}$ Low starts a new command sequence. In command framing mode, the transition back to High means the end of the command. If $\overline{SS}$ Low lasts less than 16 SCK clock cycles, no command byte is processed. If $\overline{SS}$ Low lasts more than 16 clock cycles, each 16-clock cycles triggers the SPI slave to process the word until $\overline{SS}$ returns back to High. The SPI slave will not reset the state machine when $\overline{SS}$ Low lasts exactly 8 or 16 SCK clock cycles to support byte/word framing mode. In byte/word framing mode, the user has to be aware of the command length, as there is no indication of command boundary. For this reason, command framing is recommended.

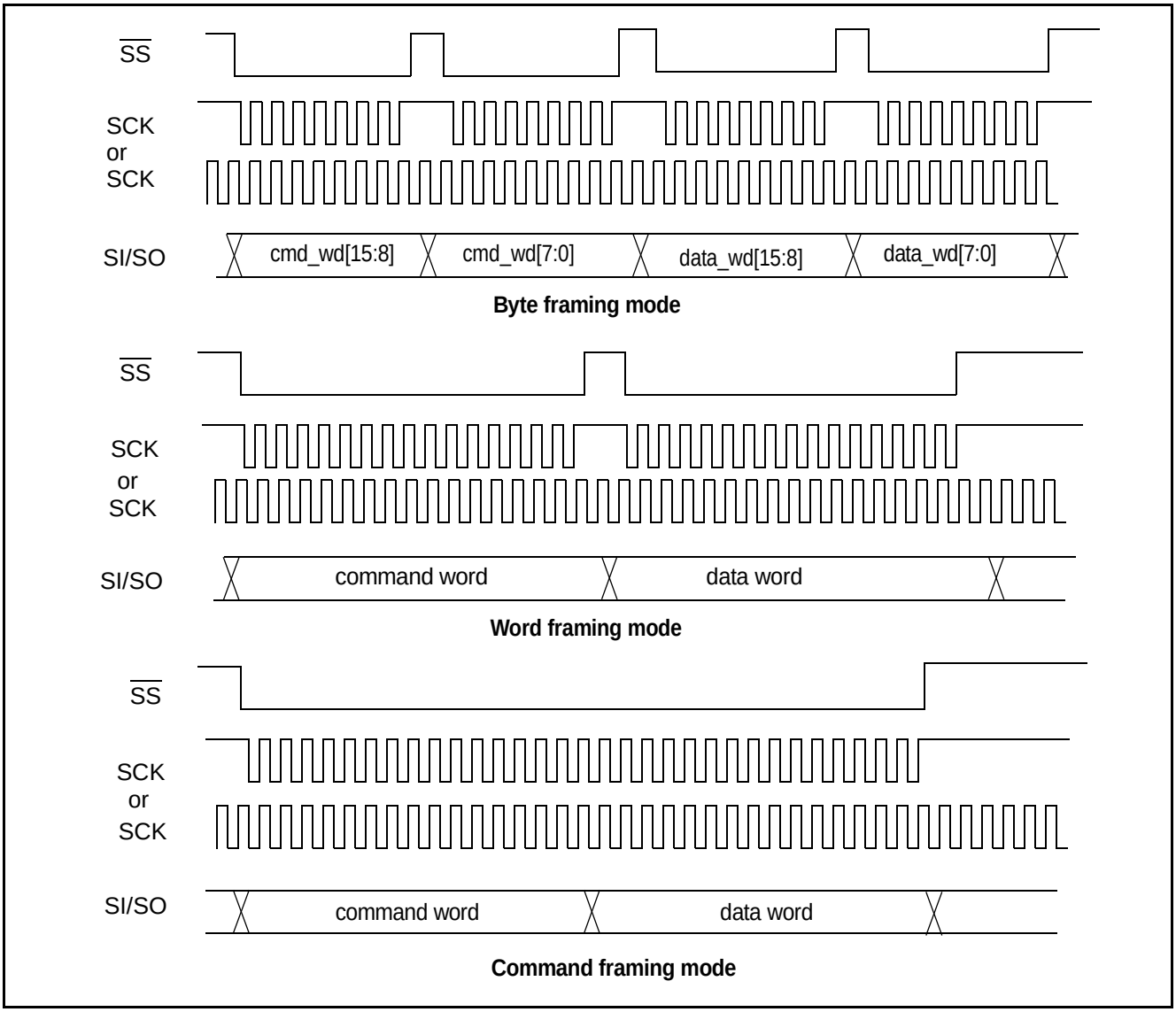


Figure 18 - $\overline{SS}$ Framing Modes

5.2.3 SPI Timing Requirements

The timing requirements for read and write accesses are shown in the following timing diagrams. The single data word read and write command is shown in Figure 19 and Figure 20. The data word can have data bytes swapped like the single data word write command in Figure 21. Bits 7:0 of the data word comes out first and bits 15:8 of the data word come out second. The timing information for the read/write command is in Figure 22, Figure 22, and Table 16.

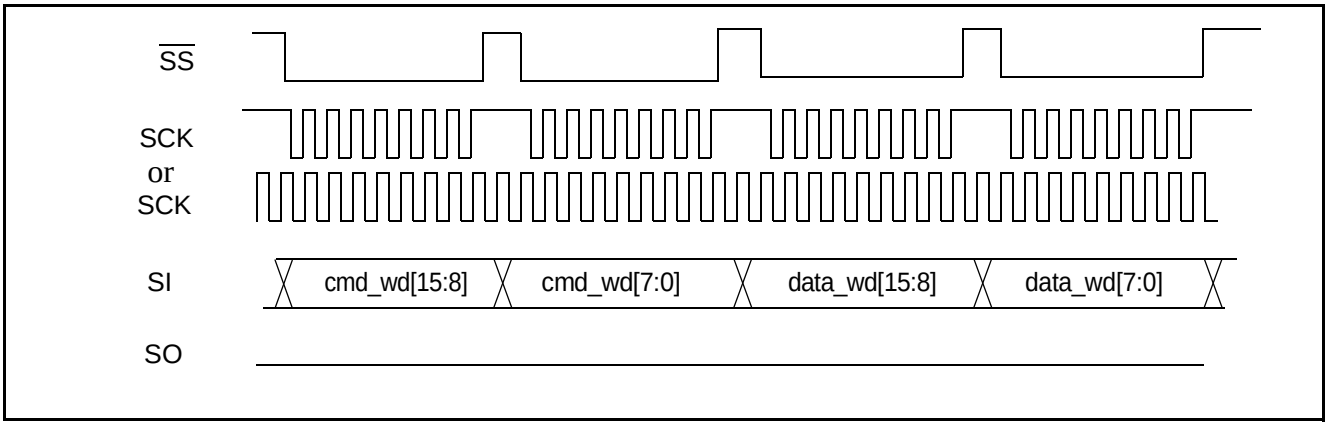


Figure 19 - One Data Word Write in Byte Framing Mode

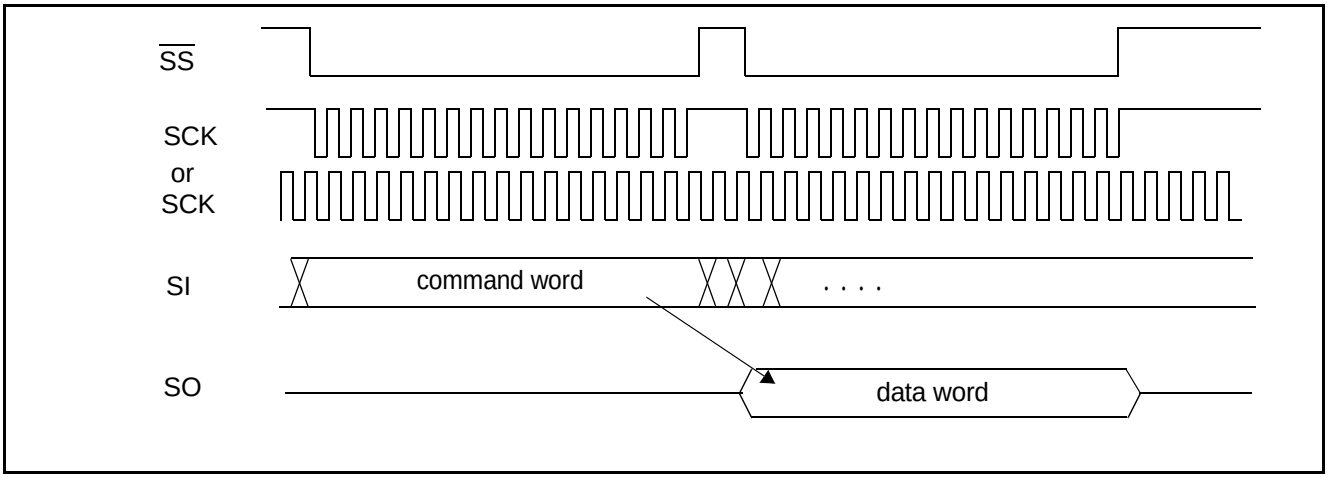


Figure 20 - One Data Word Read in Word Framing Mode

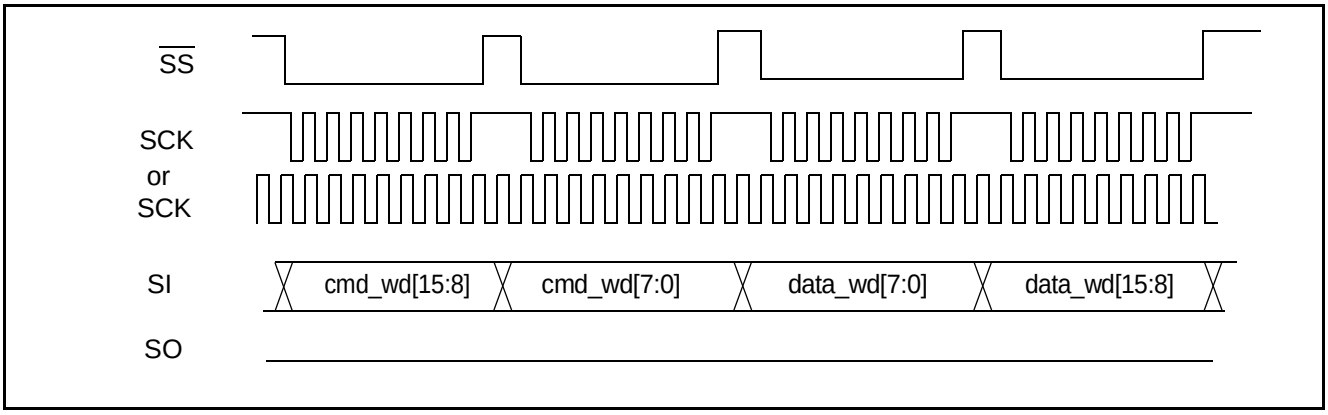


Figure 21 - One Data Word Write in Byte Framing Mode with Byte Swap

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Serial clock period	61	—	—	ns	
2	t_{DCH}	Serial clock HIGH pulse width	10	—	—		2
3	t_{DCL}	Serial clock LOW pulse width	24	—	—		2
4	t_{DCR}	Rise time of clock	—	—	8		
5	t_{DCF}	Fall time of clock	—	—	8		
6	t_{ICSS}	Slave select setup time	11	—	t_{DCY}–15		
7	t_{ICSH}	Slave select hold time	2	—	t_{DCY}–15		
8	t_{ICSL}	Slave select pulse width	—	—	—		5
9	t_{ICSO}	Slave select off time	61	—	—		2,4
10	t_{IDS}	Input data setup time	14	—	t_{DCY}–15		
11	t_{IDH}	Input data hold time	2	—	t_{DCY}–15		
12	t_{ODD}	Output data turn on delay	—	—	15		3, 6
13	t_{ODH}	Output data hold time	2	—	—		6
14	t_{ODOF}	Output data turn off delay	0	—	10		6
15	t_{ODC}	Output data valid	2	—	15		6

Table 16 - SPI Timing Parameters[1]

Notes:

1. *Refer to Figure for timing diagram test points.*
2. *SCK may be stopped in the High or Low state indefinitely without loss of information. When $\overline{SS}$ is at Low state, every 16 SCK cycles the 16-bit received data will be interpreted by the SPI interface logic.*
3. *The first data bit is enabled on the falling edge of $\overline{SS}$ or on the falling edge of SCK, whichever occurs last.*
4. *The SPI slave requires 61ns $\overline{SS}$ Off time just to make the transition of $\overline{SS}$ synchronized with SCK clock. In the command framing mode, there is no $\overline{SS}$ Off time between each 16-bit command/data and $\overline{SS}$ is held low until the end of command.*
5. *If $\overline{SS}$ is not held Low for 16 or 8 SCK cycles exactly, the SPI slave will reset. During byte or word framing mode, $\overline{SS}$ is held Low for 8 or 16 SCK cycles. During command framing mode, $\overline{SS}$ is held Low for the whole duration of the command. Besides, multiple commands can be transferred with $\overline{SS}$ low for the whole duration of the multiple commands. The rising edge of the $\overline{SS}$ indicates the end of the command sequence and resets the SPI slave.*
6. *Pin loading is assumed to be C_{load} = 75pF*

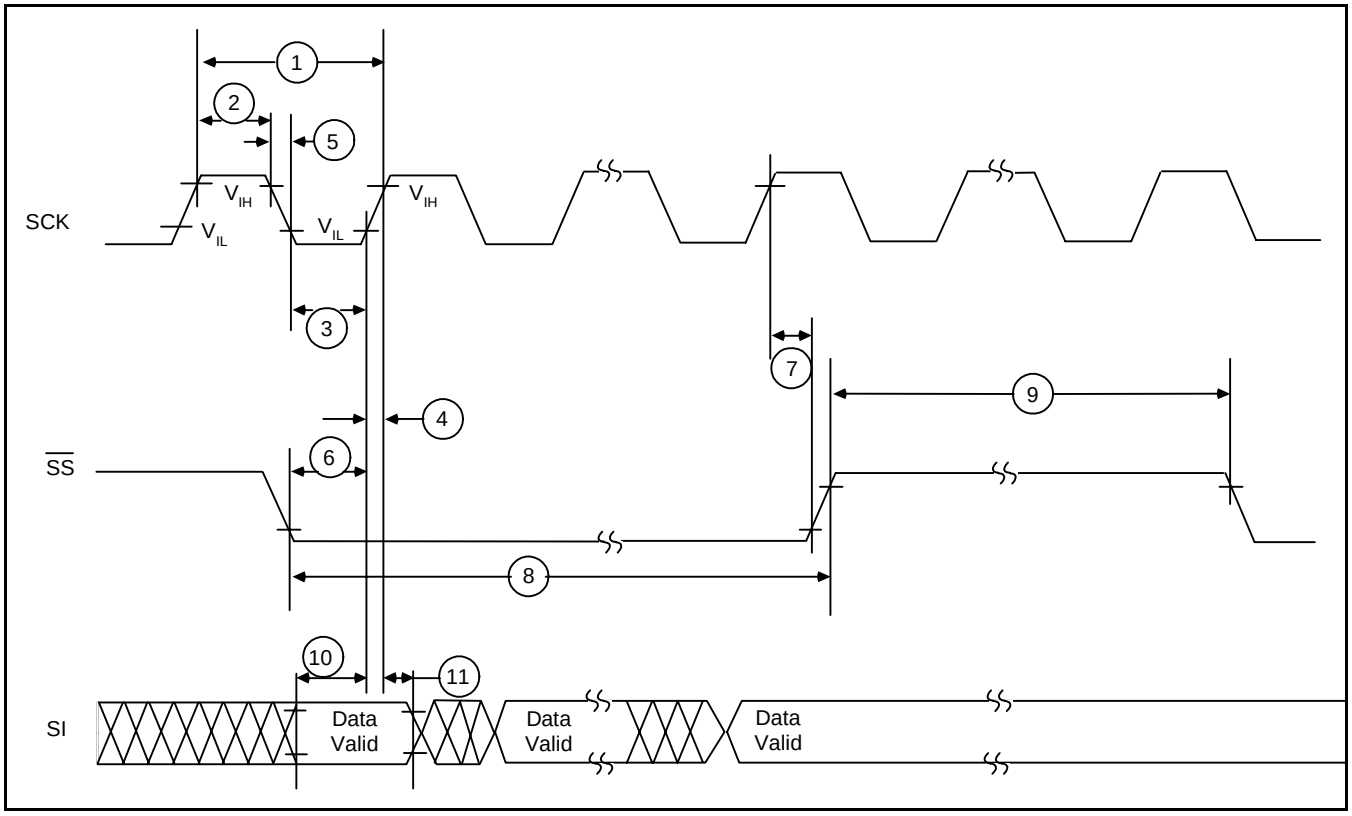


Figure 22 - SPI Interface (Input Timing)

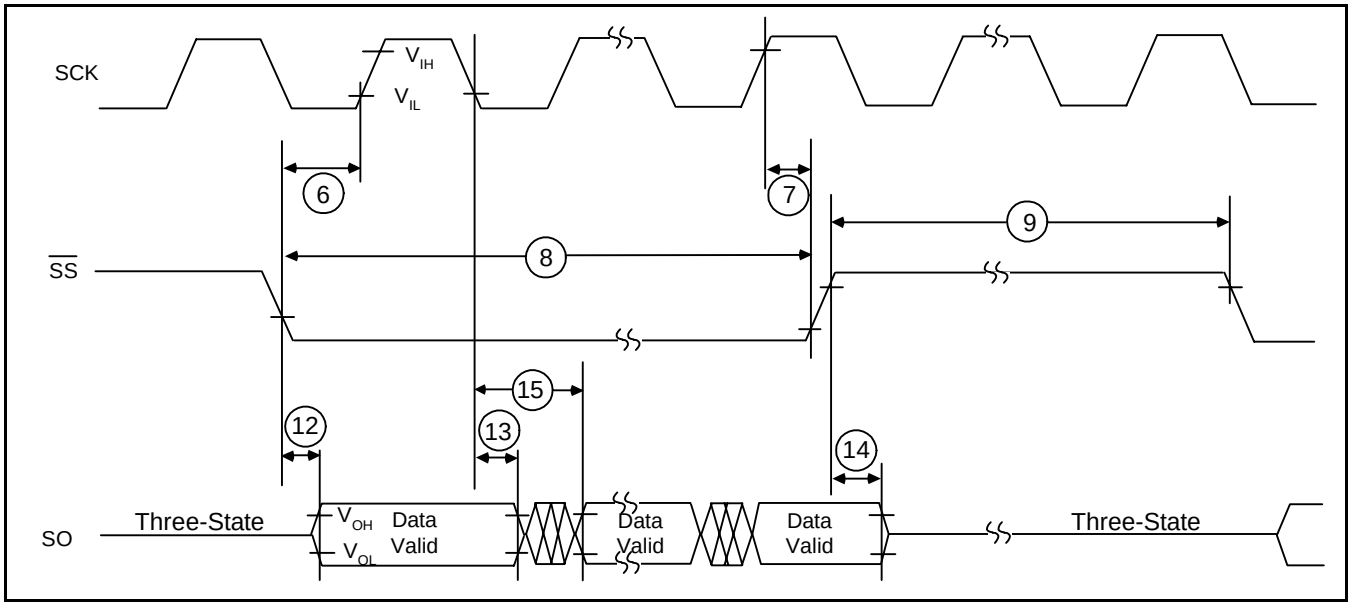


Figure 23 - SPI Interface (Output Timing)

5.3 SPI1 and SPI2 Timing

Two Master SPI blocks are provided to communicate with the MPI interfaces of up to 8 QISLAC (4 OISLAC) devices each. This interchip highway carries control information between the VCP II and the ISLAC devices. Timing will be met as long as loading and signal integrity issues are properly handled on the printed circuit board.

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	t_{DCY}	Data clock period	114	129	3657.1	ns	
2	t_{DCH}	Data clock ON pulse width	34	—	1809		
3	t_{DCL}	Data clock OFF pulse width	77	—	1852		
	t_{DCR}	Rise time of clock	—	—	5		2
			—	—	8		3
	t_{DCF}	Fall time of clock	—	—	5		2
			—	—	8		3
4	t_{CSS}	Chip select setup to first clock edge	62	—	—		2
			62	—	—		3
5	t_{CSO}	Chip select output delay	2	—	15		
6	t_{MOSIS}	Data output setup to first clock edge	50	—	—		2
			50	—	—		3
7	t_{MOSIH}	Data output hold time	1	—	15		2
			1	—	15		3
8	t_{MISOS}	MISO/MOSI(3-wire) input setup time	15	—	—		
9	t_{MISOH}	MISO/MOSI(3-wire) input hold time	0	—	—		

Table 17 - SPI1 and SPI2 Timing Parameters[1]

Note:

1. *Refer to Figure for timing diagram test points.*
2. *Assumes 40-pF load on SPI_CLK, SPI_MOSI, and SPI2_$\overline{CS}$ or GPIO[31:16].*
3. *Assumes 150-pF load on SPI_CLK and SPI_MOSI, but 40-pF load on SPI2_$\overline{CS}$ or GPIO[31:16]. Assumes a 50 Ω series termination at output of SPI_CLK.*

5.3.1 Timing Requirements

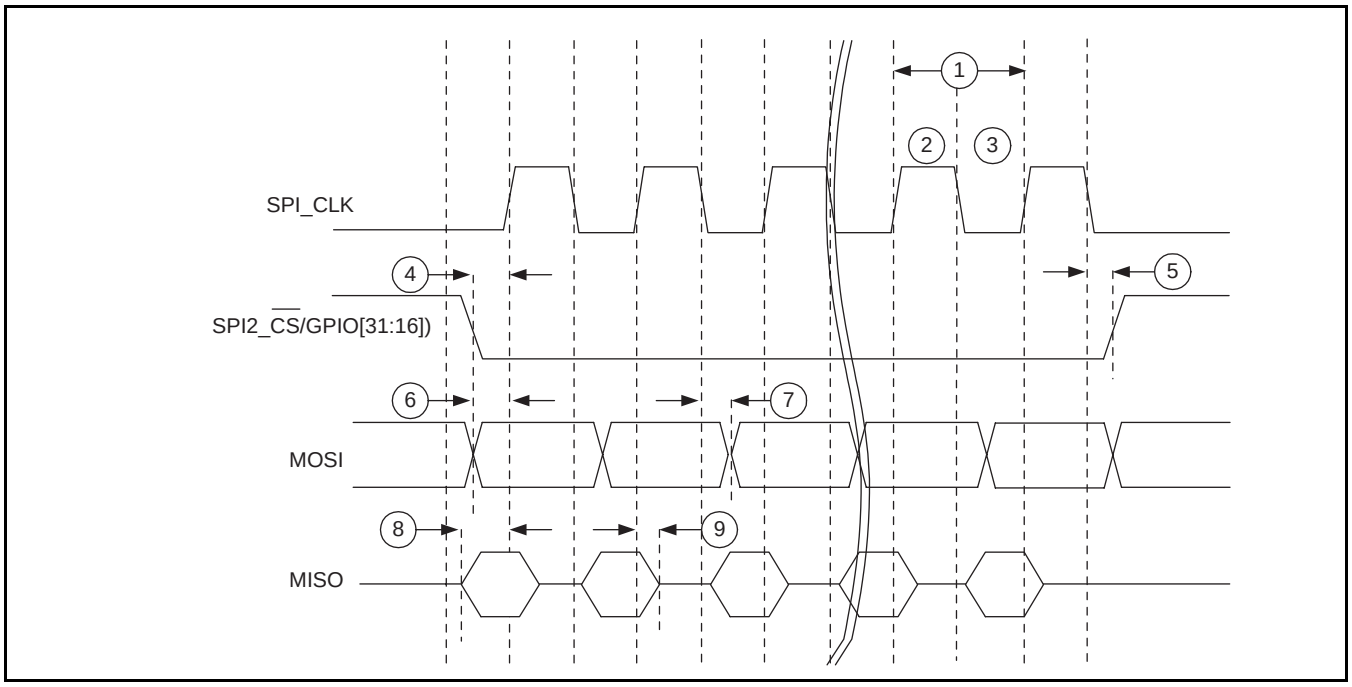


Figure 24 - SPI Timing Waveforms

5.4 PCM Interface

Two PCM blocks reside on the Le79114 device. There is a Slave PCM Highway A/Redundant block comprised of the PCLKA, FSA, DXA, DRA, TSCXA, TSCRA, PCLKB, FSB, DXB, DRB, TSCXB, and TSCRB pins, and a block used as the Slave PCM Highway B comprised of the MPCLK, MFS, MDX, and MDR pins. The Slave PCM Highway A/Redundant block requires PCLKA or PCLKB as inputs. The Slave PCM Highway B requires MPCLK as an input. In hardware, MPCLK and MFS can be configured as outputs, therefore specifications for output use are provided in Table 18.

The Redundant highway is useful if the A highway suffers a system failure. PCLKA and PCLKB are closely monitored by CLKGEN to perform an automatic highway switch (if desired) when the selected highway fails.

The Slave PCM Highway A/Redundant block provides backplane driver tristate control outputs $\overline{\text{TSCXA}}$ and $\overline{\text{TSCXB}}$ when DXA or DXB are active respectively. The Slave PCM Highway B block does not have a redundant backup or the tristate control outputs.

Timing for these blocks is shown in Figure 25 and Table 18. PCLK accuracy = ± 100 PPM

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
1	t_{PCY}	PCLKx or MPCLK period	61	—	1953.1	ns	2,4,6,7
			122	—	1953.1		2,5,6,7
2	t_{PCH}	PCLKx or MPCLK HIGH pulse width	24	—	—		4
			48	—	—		5
3	t_{PCL}	PCLKx or MPCLK LOW pulse width	24	—	—		4
			48	—	—		5
	t_{PCF}	Fall time of PCLKx (Input)	—	—	8		
	t_{PCR}	Rise time of PCLKx (Input)	—	—	8		
	t_{MPCF}	Fall time of MPCLK (Output)	—	—	8		10
	t_{MPCR}	Rise time of MPCLK (Output)	—	—	8		10
4	t_{FSD}	FS delay (Output rising or falling)	2	—	15		4
			2	—	25		5
5	t_{FSS}	FS setup time (Input)	11	—	t_{PCY}–2		
6	t_{FSH}	FS hold time (Input)	0	—	—		
7	t_{DOH}	Data output hold time	5	—	16		4
			5	—	25		5
8	t_{DOZ}	Data output delay to high-Z	0	—	10		3
9	t_{TSCD}	TSC output delay	5	—	16		4
			5	—	25		5
10	t_{TSCZ}	TSC output delay to high-Z	0	—	10		
11	t_{DIS}	Data input setup time	10	—	—		9
12	t_{DIH}	Data input hold time	10	—	—		9
	t_{PCT}	Allowed PCLK jitter time	–97	—	97		7
	t_{FST}	Allowed Frame sync jitter time	$-t_{PCY}/2$	—	$t_{PCY}/2$		8

Table 18 - PCM Interface Timing Parameters[1]

1. *Refer to Figure for timing diagram test points.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of 512 kHz +/- 6000 ppm and be specified to within 100ppm. The minimum clock frequency is 512 kHz.*
3. *$\overline{TSC}$ is an open drain driver. t_{TSO} is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The minimum pull-up resistance to VDD is 360 Ω.*
4. *C_{load} = 40 pF*
5. *C_{load} = 150 pF*
6. *If PCLK is used to drive the main system clock, it must be present at all times to maintain proper internal operation. A total clock failure will result in a 60% reduction in internal MIPs within 125 µs. If the clock failure can be restored within 2 µs, a MIP drop of only 1% will result. The VCP II device has the capability to detect an abrupt frequency change greater than 8% and switch within 2 us.*
7. *Maximum PCLK jitter is +/- 97ns or 1/2 of the PCLK period whichever is less.*
8. *The number of PCLKs per FS period may deviate by 1 clock (not by +/-1 which would be 2).*
9. *Data input setup and hold times occur within a sampling window which is referenced to an internal clock. Setup and hold times are specified assuming standard firmware usage.*
10. *Assumes 150-pF load on MPCLK and a 50 Ω series termination at output of MPCLK.*

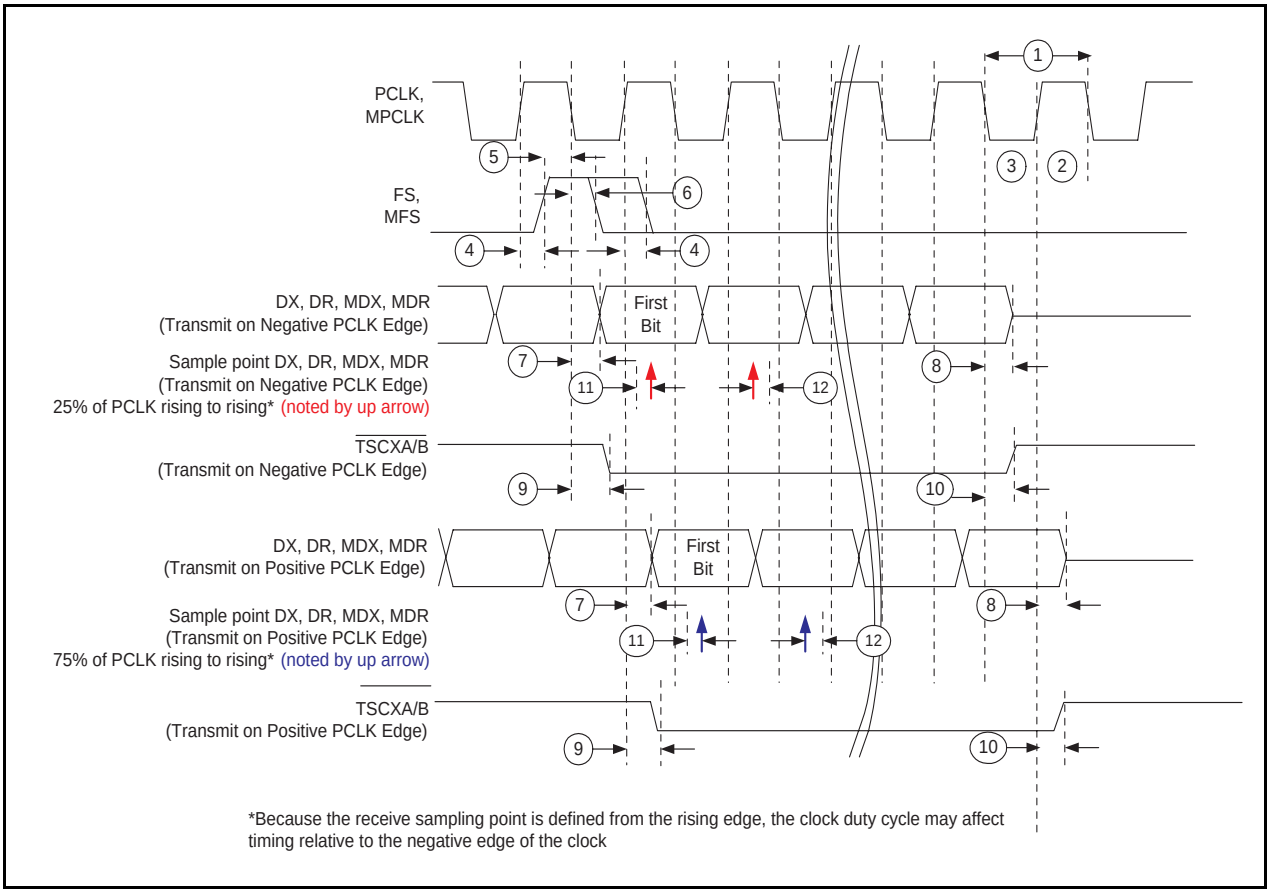


Figure 25 - PCM Highway Timing

6.0 The VCP II Device Interrupt Report and Service Mechanism

There are two types of interrupt generated in the VCP II device: the System Interrupt and the Event Interrupt.

The System Interrupts are hardware implemented and are maskable. Multiple System Interrupt sources may be reported simultaneously.

The Event Interrupts are defined by the application and are reported one at a time. Three Event queues allow these interrupts to be spooled off in the order they were received, per priority level.

An interrupt is normally reported to the host whenever there is any outstanding interrupt in the System Interrupt Source register or one of the event queue interrupt fifo. An "event_delay" bit exists so that the lowest 2 event queues will not assert an interrupt until a system or queue one interrupt occurs. This second option reduces the number of interrupts received by the host processor to only the number of higher priority events. Interrupt to the external host is level sensitive. The $\overline{\text{INT}}$ pin remains High if there is no pending interrupt. When an interrupt occurs, the $\overline{\text{INT}}$ pin is pulled Low to signal the external microcontroller that an interrupt has occurred. Reading the interrupt indication register by the external microcontroller clears the interrupt. After reading the interrupt indication register by the external microcontroller, the $\overline{\text{INT}}$ pin will go High if there is no pending interrupt. The $\overline{\text{INT}}$ pin will continuously stay Low if there is another pending interrupt.

Interrupts are reported based on their priority. System interrupts have the highest priority. For the event interrupts, event queue 1 has the highest priority and event queue 3 has the lowest priority. The interrupt signal is latched before reporting to the host through the $\overline{\text{INT}}$ pin.

7.0 Debug Interfaces

Zarlink recommends that footprints for two connectors be provided for in the PCB layout. Having access to the VCP HBI/PCM interface and Debug port can help to facilitate initial line card start-up.

7.1 HBI/PCM Interface Header

The HBI/PCM interface header is a 38-position matched impedance socket (Mictor) mounted on the line card. When properly configured, the header allows the line card to be controlled by the Zarlink Le71HP0300 Universal Voice Board (UVB) instead of the user’s control interface. The header will receive a cable that interfaces to the UVB’s DIN connector.

The PCB should be laid out to accept a Samtec Micro High Speed Interface Socket MIS-019-01-F-D, or equivalent. On production line cards, this socket does not need to be populated. Figure 26 defines the pin-out of the socket. Note that in addition to the 38 signal positions, the socket provides 5 ground connections.

When this interface is used, it needs to be isolated from the user’s control interface. One way to provision for this is to use series termination resistors on each PCM and HBI signal and then to simply remove them if the debug interface is to be used. An example of series termination placement is shown in Figure 27. Signals driven from the Host Processor or Network Interface have series termination resistors placed near their respective drivers. Signals driven from the VCP have series termination resistors placed near the VCP II, but placed on the other side of the Mictor socket so that the Mictor socket can be fully isolated during a debug implementation.

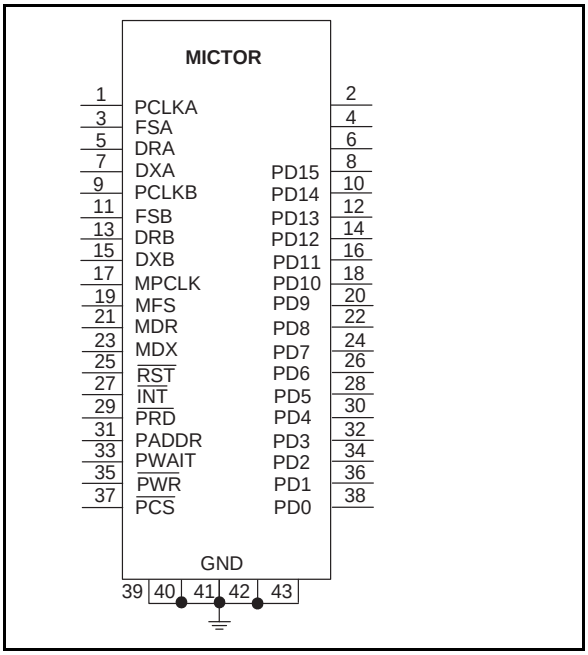


Figure 26 - Mictor Socket Pin-out

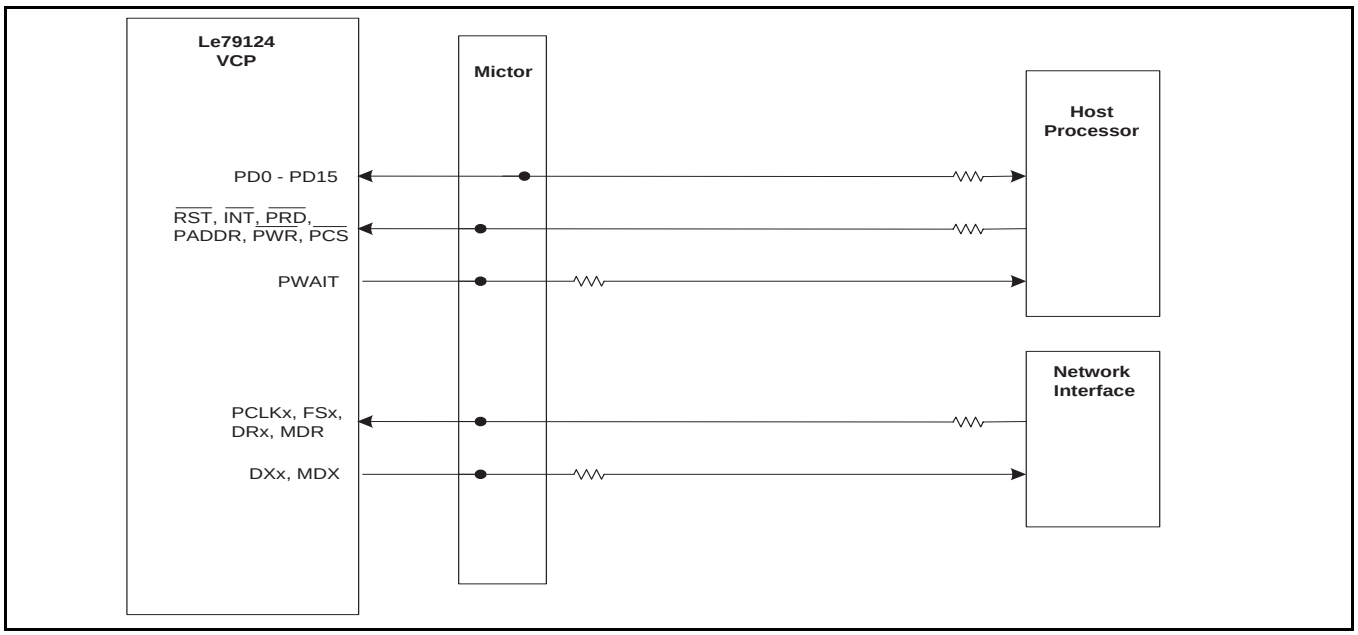


Figure 27 - Series Termination Resistor Placement

7.2 Debug Port

This port is for debug use only. If debug of VCP II operation becomes necessary, Zarlink may require access to this port.

Two Debug port access methods are presented.

The board can be laid out with a population option debug header and with population option pull-up and pull-down resistors. This interface is detailed in Figure 28. The 14-pin header pins should be spaced 2.54 mm (100 mils) row to row and 2.54 mm (100 mils) column to column.

An alternate approach is to simply bring TCK, TMS, TDI, TDO, and $\overline{\text{TRST}}$ pins out to test points with $\overline{\text{TRST}}$ tied to digital ground through a 1 KΩ resistor (R3 in Figure 28 and $R_{\overline{\text{TRST}}}$ in Figure 30). This will allow easy access if it becomes necessary to jumper to the Debug port. Holding $\overline{\text{TRST}}$ low ensures that the Debug port is kept in reset during power supply bring-up.

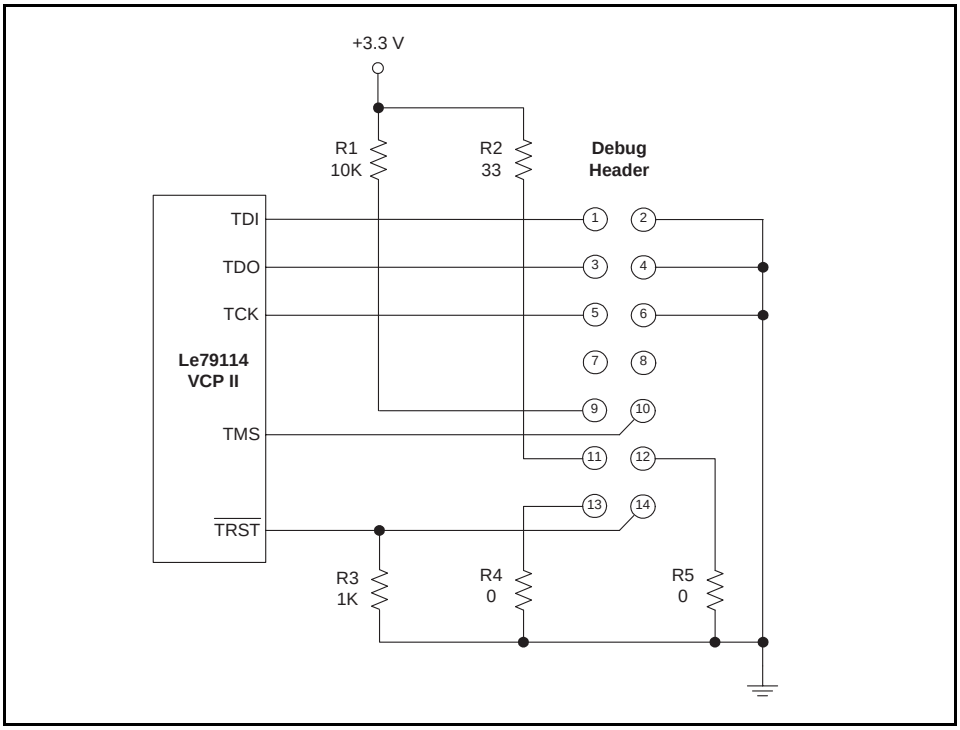


Figure 28 - VCP Debug Port - Optional Header Interface

8.0 Timing Diagram Test Points

DVDD = PLL_VDD = 3.3 V ±5%, PLL_VSS = DVSS = 0 V.

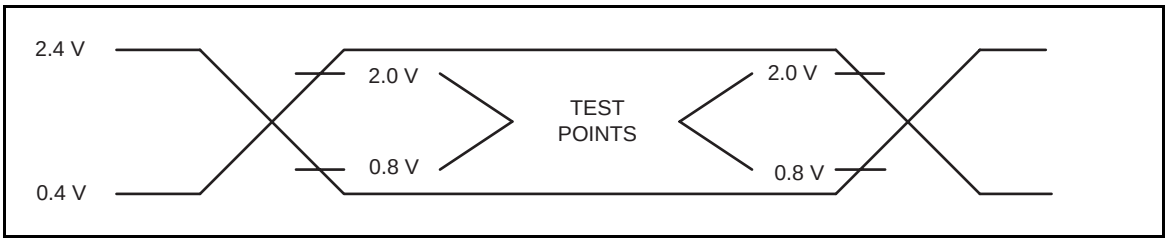


Figure 29 - Timing Diagram Test Points

9.0 Troubleshooting at Initial Start-up

Verify that the power supplies and the Configuration pins are appropriately set. Configuration pins must be set before releasing the VCP II device from reset.

Next perform the following steps to check that the VCP II can be read and written through the HBI.

1. Probe the PWAIT pin. With reset inactive, perform a write of 0x04 to the Configure Interface register (CMD 0xFD04). This should result in the PWAIT pin going High; writing 0x06 (CMD 0xFD06) will make PWAIT go Low. This verifies the basic HAL function - VpHalHbiCmd().
2. With reset inactive, perform a read of the CMD register. This should return 0x0002 (the 2 bit is the interrupt pin status—it should be High, inactive). To read the CMD register in 8-bit mode, perform two back to back 8-bit reads of the CMD register location. For this step, no HAL function needed, simple address read.
3. Write to the Page register (CMD 0xFEzz - zz being any page number 0 - 0xFF). This write should be reflected in a subsequent read of the CMD register above. A CMD of 0xFEAA should result in a read from the CMD register of 0xAA02. This is writing the Page register which gets reflected in a read of the CMD register (again, the read is two 8-bit reads of the CMD register location—the same location read twice).
4. A read of the PCLK-Selection register (CMD 0x8801, followed by two 16-bit reads of the data register) with no PCLK or FS will result in a value of 0x92FB 0x92FB. If both PCLK and FS are present, then the value read will be the exact PCLK detected by the device (see page 21 or 22 for returned value). This step reads two words using HAL function - VpHalHbiRead(). The command to read the PCLK registers (A and B) is 0x8801 to read two words. Word 0 is PCLKB and will return the exact PCLK detected by the VCP or 0x92FB if PCLKB is not present. Word 1 is PCLKA and will return the exact PCLK detected by the VCP or 0x92FB if PCLKA is not present.

If the four steps above were completed successfully, the VCP II device is now functional.

Finally, run the quickstart application that is provided in the package and boot-load the API image. This provides verification of the VCP II firmware image download and execution, the MPI to SLAC interface, and the integrity of the PCM highway and the voice path. It also verifies basic call control, usage of profiles, DTMF decoding, and line testing. The boot-load is supplied as a binary firmware load to the VCP II. It is to be boot-loaded into the VCP II along with some C host code to boot-load and control the image.

10.0 Application Circuits

64-channel application circuits are provided highlighting the VCP II hardware interfaces.

Figure 30 illustrates VCP II HBI control, VCP II SPI connections to the ISLAC MPI port, and PCM connections using a single PCM highway. Powering options and configuration pins are also shown.

The 16-bit parallel HBI is shown. For a 64-channel application, 16-bit parallel is the recommended interface.

The SPI connections consist of VCP II SPI port 1 controlling the first group of 32 channels and VCP II SPI port 2 controlling the second group of 32 channels. VCP II GPIO pins are used to control the ISLAC chip select and receive ISLAC interrupts.

VCP II Slave PCM Highway A is used and it services voice and data for all 64 channels. The PCM highway runs off of SYS_PCLK and SYS_FS from the backplane.

A Line Card Parts List for the VCP II device follows the application circuits.

The next figures highlight other PCM options.

Figure 31 illustrates a single PCM highway with the Redundant highway back-up option.

This application demonstrates use of VCP II Slave PCM Highway A and the VCP II Redundant Slave PCM Highway. All ISLAC devices share the same PCM highway. Both ports run off of SYS_PCLK and SYS_FS from the backplane.

Figure 31 illustrates a dual PCM highway option.

The VCP II Slave PCM Highway A services voice and data for the first group of 32 channels and the VCP II Slave PCM Highway B services voice and data for the second group of 32 channels. The Slave PCM Highway A is wired to ISLAC port A, the Slave PCM Highway B is wired to ISLAC port B (that is, DRB and DXB of the ISLAC). PCM highway 1 runs off of SYS_PCLK1/SYS_FS1 and PCM highway 2 runs off of SYS_PCLK2/SYS_FS2 from the backplane.

PCLKB to MPCLK and FSB to MFS connections allow clock failure detection to monitor the Slave PCM Highway B. Tie PCLKB and FSB to ground if these connections are not used.

Figure 33 illustrates an alternative clocking scheme for dual PCM highways. Here both highways use a common PCM clock and frame sync.

Figure 34 illustrates a separate voice PCM highway and test PCM highway option.

The VCP II Slave PCM Highway A services voice and data for all 64 channels. Slave PCM Highway A is wired to ISLAC port A on all ISLAC devices.

The VCP II Slave PCM Highway B services all 64 channels but is dedicated to line testing. The Slave PCM Highway B is wired to ISLAC port B (that is, DRB and DXB) on all ISLAC devices. VCP II MPCLK and MFS connect to SYS_PCLK and SYS_FS respectively, as the VCP II highway B is a slave to the clocking. The PCM and test highways are synchronized and both run off of SYS_PCLK and SYS_FS from the backplane.

All schematics show a 3-state buffer on the ISLAC DXA or DXB lead. For 64-channel operation this is recommended. Refer to the *Ve790 Series MPI and PCM Signal Integrity* application note for more information.

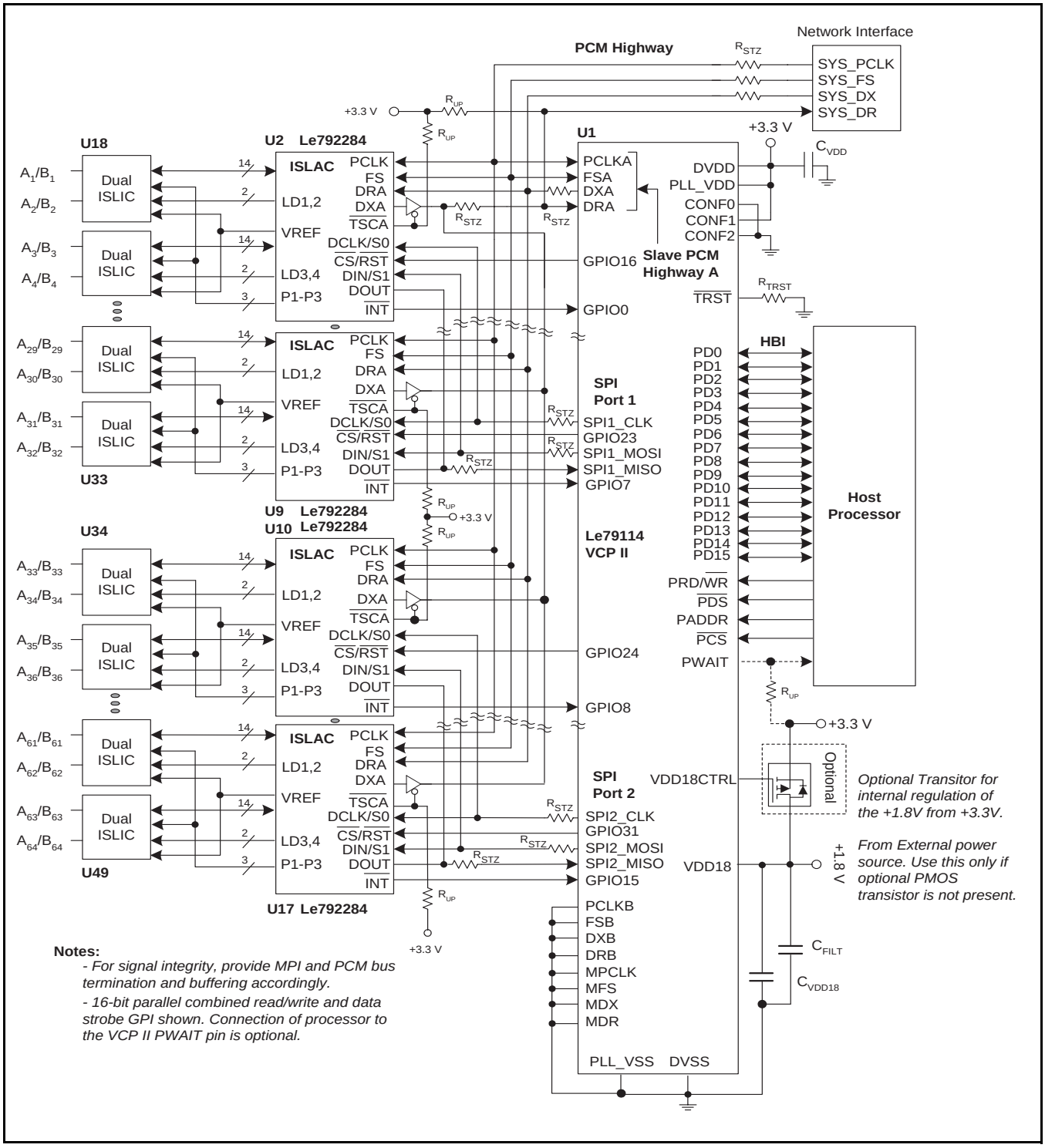
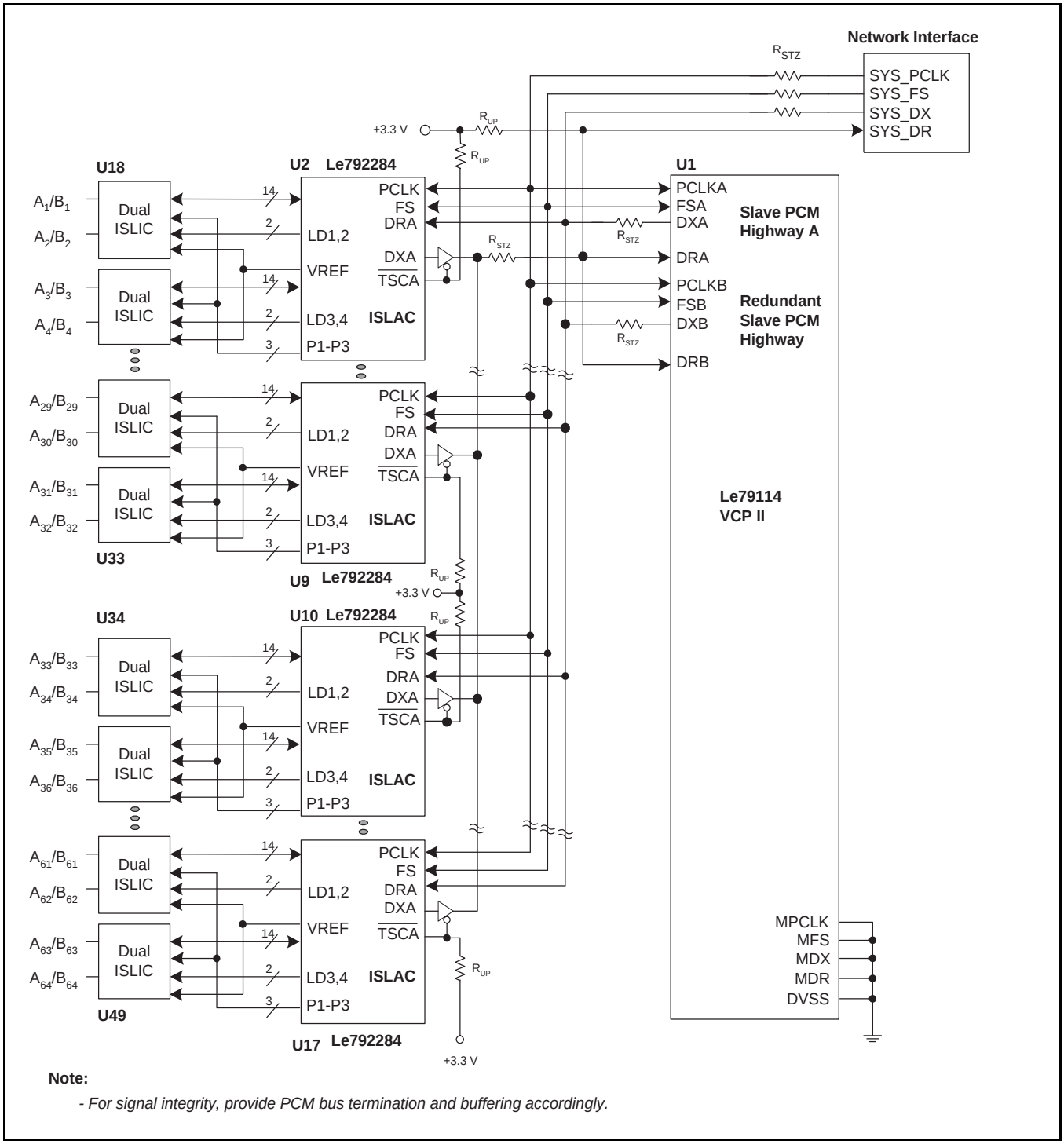


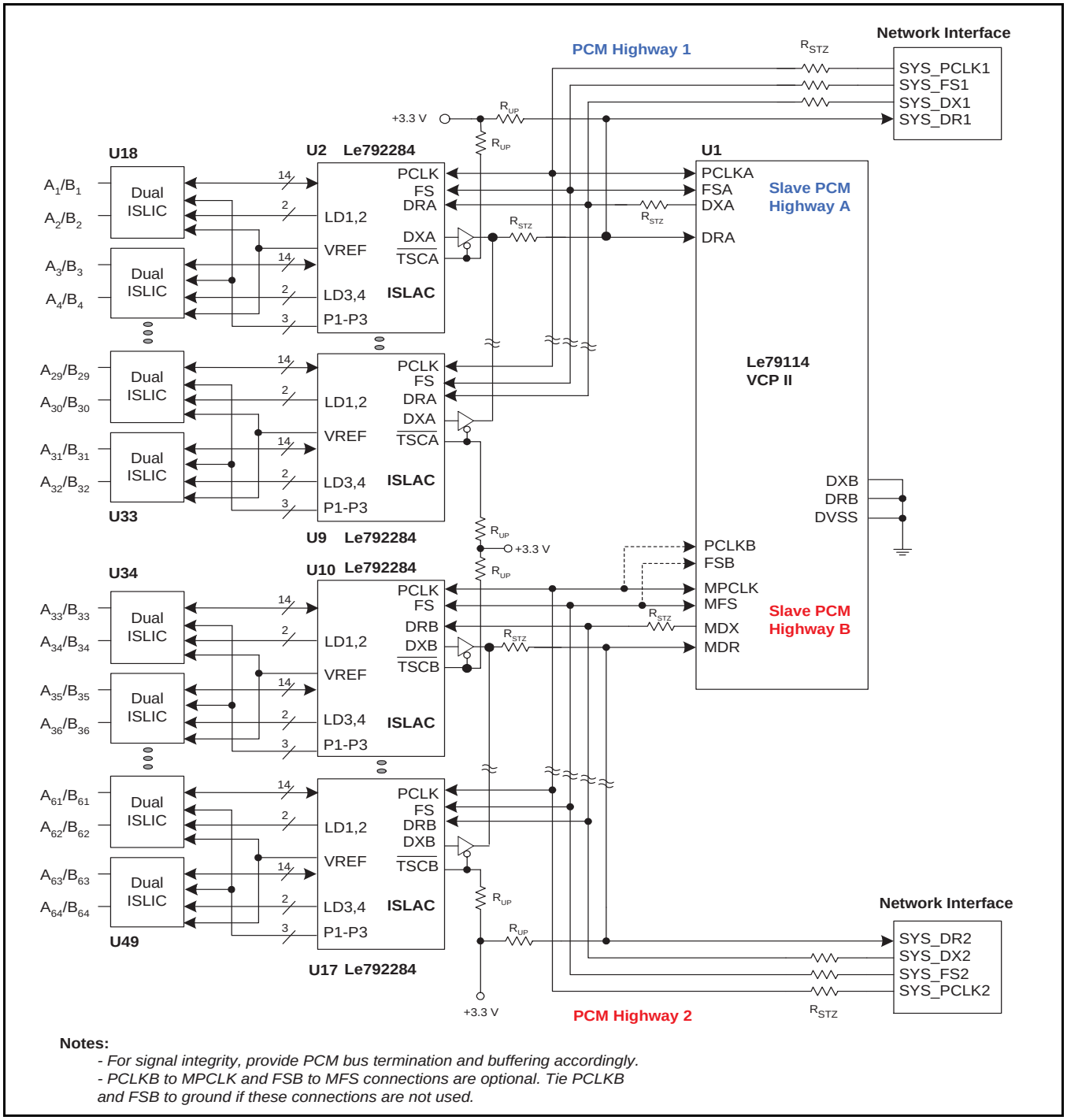
Figure 30 - 64-Channel Application - Illustrating HBI, SPI and a Single PCM Bus



Note:

- For signal integrity, provide PCM bus termination and buffering accordingly.

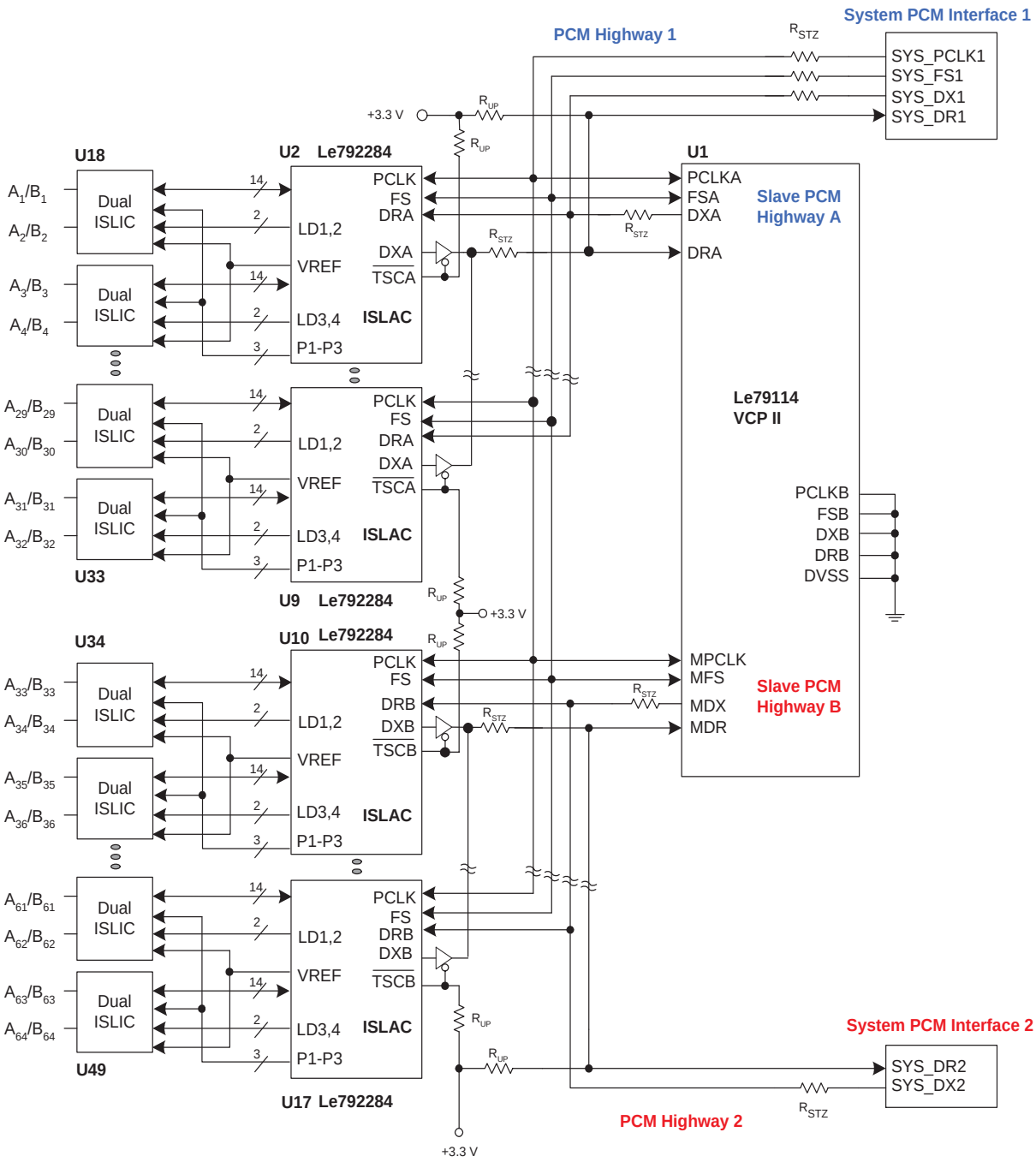
Figure 31 - 64-Channel Application - Single PCM Bus with Redundant Highway



Notes:

- For signal integrity, provide PCM bus termination and buffering accordingly.
- PCLKB to MPCLK and FSB to MFS connections are optional. Tie PCLKB and FSB to ground if these connections are not used.

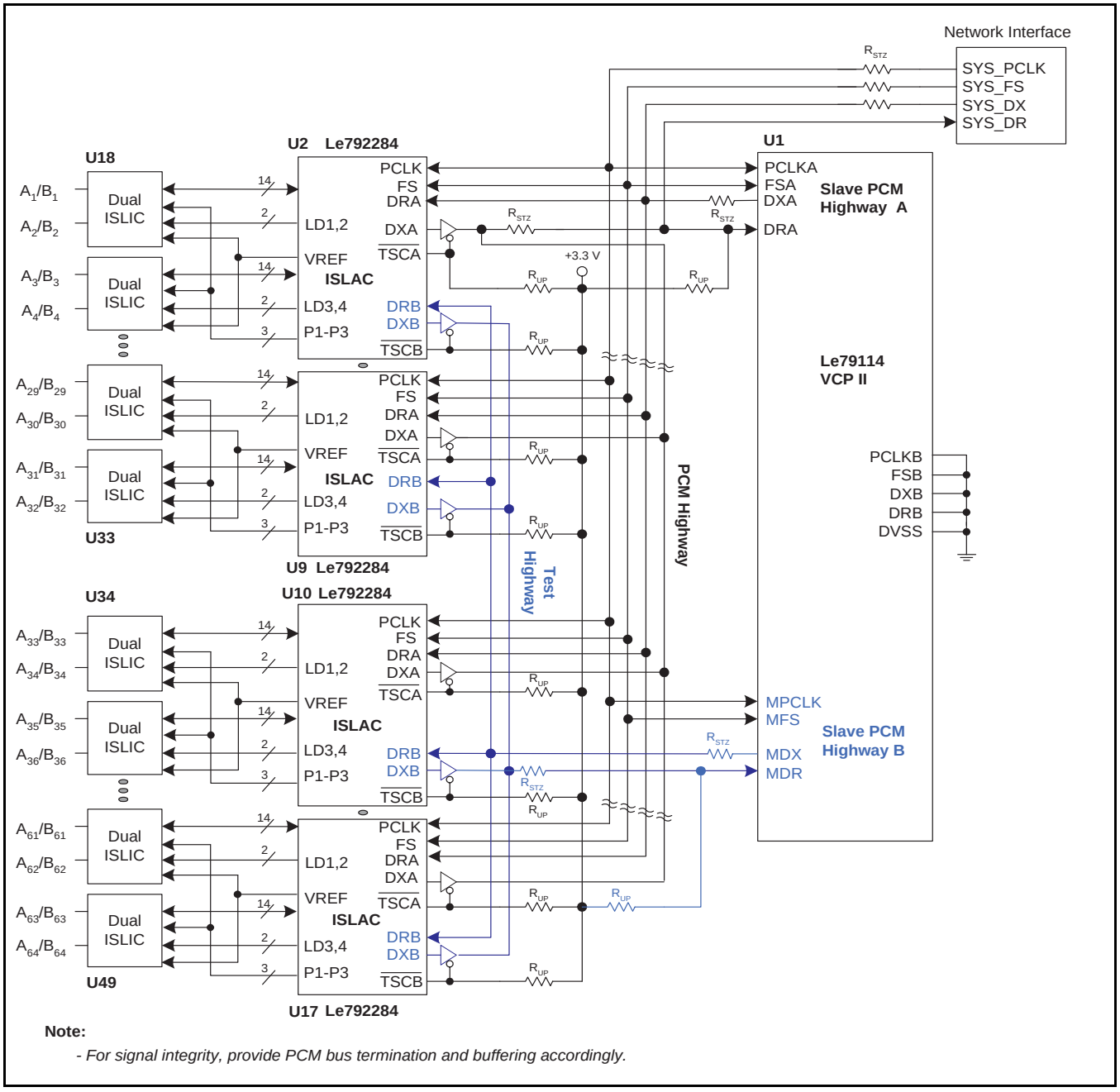
Figure 32 - 64-Channel Application - Dual PCM Highways



Note:

- For signal integrity, provide PCM bus termination and buffering accordingly.

Figure 33 - 64-Channel Application - Dual PCM Highways with a Single Clock and Frame Sync



Note:

- For signal integrity, provide PCM bus termination and buffering accordingly.

Figure 34 - 64-Channel Application - Separate Voice and Test PCM Highways

11.0 Line Card Parts List

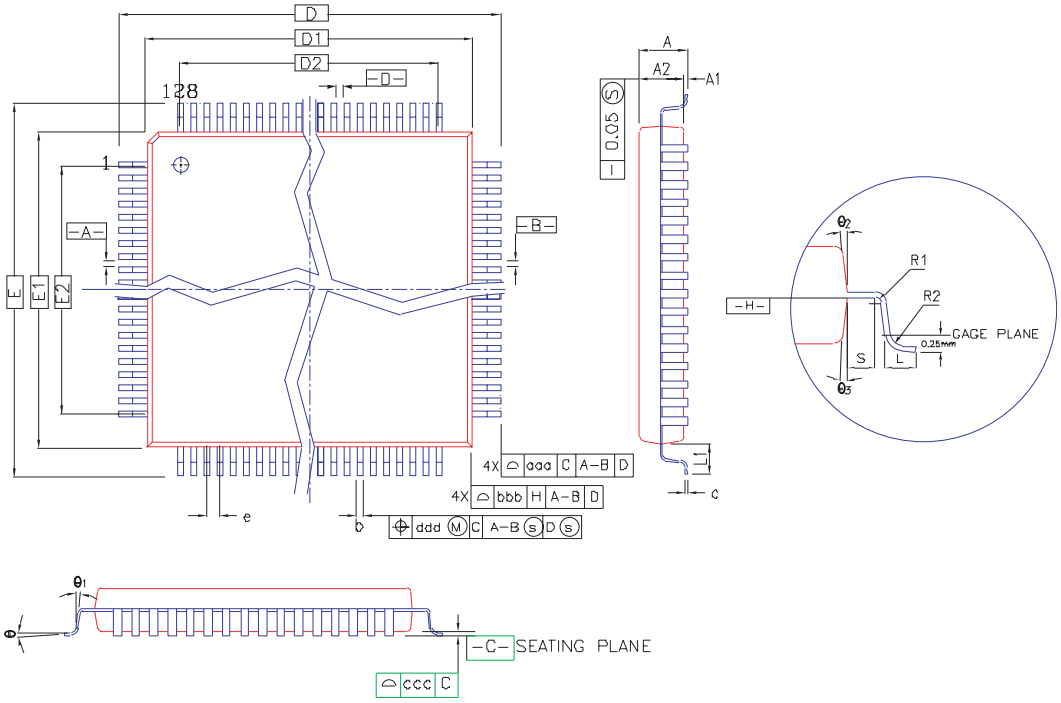
The following table lists the components required for a 64-channel Line Card circuit as shown in Figure 30. External components required for VCP II device use are listed. Refer to the ISLIC™ and ISLAC™ data sheets for external components used with those devices.

Item	Qty	Type	Value	Tol.	Rating	Comments
U1	1	Le79114				VCP II device
U2 – U17	16	Le79Q2284 or other ISLAC™ derivative				ISLAC device
U18 – U49	32	Le79232, Le79242, or Le79252 ISLIC™ device				ISLIC device
R_{UP}	17	Resistor	10 kΩ	10%	1/16 W	
R_{STZ}		Resistor	39 Ω	10%	1/16 W	Select appropriate value for transmission line
R_{TRST}	1	Resistor	1 kΩ	10%	1/16 W	Refer to Debug Interface for debug port options.
C_{VDD}	9	Capacitor	100 nF	20%	10 V	Ceramic
C_{VDD18}	4	Capacitor	100 nF	20%	10 V	Ceramic
C_{FILT}	1	Capacitor	10 µF	20%	6.3 V	Ceramic or tantalum. Use when external supply is used.
			100 µF	20%	6.3 V	Ceramic or tantalum. Use when MOSFET is used.
Q1	1	P-channel MOSFET	1.8 V			Optional

12.0 Physical Dimensions

128-Pin TQFP

PACKAGE OUTLINE
TQFP 128L
14X14X1.0 MM



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	–	0.16	–	–	0.006	–
e	0.40 BSC			0.016 BSC.		
D2	12.4			0.488		
E2	12.4			0.488		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
   MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE
   LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY
   MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS
   OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION
   AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and
   0.5mm PITCH PACKAGES.

Notes:*Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.*

13.0 Revision History

Revision D1 to E1

- Page 1; Block Diagram modified.
- Page 5; $\overline{\text{TSCxx}}$ description enhanced. Modified Table 3 text.
- Page 6; Moved UART from Table 4 to Table 3.
- Page 7; Dual use pin statement added.
- Page 40; Reversed items 2 and 3 in Figure 22.
- Page 41, 42; PCM Interface text enhancements. Data input setup and hold times modified for standard firmware sampling.
- Page 43; Timing and information on Zarlink use only ports removed.
- Page 45, 48; Show C_{FILT} on VCP II VDD18 node.

Revision E1 to F1

- Page 1; Block Diagram modified.
- Page 5; Modified PCM interface descriptions.
- Pages 18 and 19; Changed Highway B to Redundant Highway.
- Page 41; Modified PCM interface description.
- Page 44; Timing and information on Zarlink use only ports removed.
- Page 45; Modified Application Circuits description.
- Pages 46 - 50; Figures 26 - 30, modified and added application schematics.
- Page 51; Line Card Parts List, changed R_{STZ} from 40.2 to 39 ohms.
- Minor text edits.

Revision F1 to G1 (Version 6)

- Page 5; Added pull-down resistor to $\overline{\text{TRST}}$ description.
- Page 6; Added unused comment to SPI2_MOSI and SPI2_MISO descriptions.
- Page 8; Enhanced WDT_$\overline{\text{OUT}}$ description.
- Page 9; Updated Package Assembly description.
- Pages 27 - 29; Enhanced GPI Connections to an External Host section and added hardware drawings.
- Page 36; Enhanced SPI External Pins Connection section and added hardware drawing.
- Page 44; Added HBI/PCM Interface Header section to Debug Interfaces.
- Pages 45 - 46; Modified Debug Port description and <Cross-Reference>Figure .
- Page 47 and 50; Added PCLKB/FSB connections to dual PCM highway option.
- Page 48; Added R_{STZ} to SPI clocks.
- Minor text edits.

Version 6 to Version 7

- Page 9; Absolute Maximum Ratings, added Maximum Junction Temperature.
- Page 9; Modified Package Assembly description.
- Page 9; Added Thermal Resistances section.
- Page 9; Updated Electrical Ranges note.

Version 7 to Version 8

- Changed data sheet to Zarlink format.
- Page 7; Table 1, added "If unused, let pin float" to PWAIT description.
- Page 11 and 63; Added C_{FILT} of 100 µF for MOSFET use.
- Page 14; DC Specifications, Item 5a and 5b, Fixed note references.
- Page 57; Added "Troubleshooting at Initial Start-up" section.
- Minor text edits.

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