Le87270

Microsemi
Power Matters.™

VDSL2 30a, Class AB Line Driver
Preliminary Data Sheet

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FEATURES

- VDSL2 30a profile, 14.5 dBm Line Driver
- Very low power dissipation
  - Class AB operation
- Up to 8 programmable states
- No external gain resistors required
- Small footprint package
  - 16-pin (4 mm x 4 mm) QFN
- RoHS compliant

APPLICATIONS

- VDSL2 Line Driver
- ADSL2+ CPE Line Driver

DESCRIPTION

The Le87270 is a single channel differential amplifier designed to drive full rate VDSL2, as well as ADSL2+ signals with very low power dissipation. The Le87270 contains a pair of wideband amplifiers designed with Microsemi's HV15 Bipolar SOI process for low power consumption.

ORDERING INFORMATION

Le87270NQC	16-pin QFN Green Package	Tray
Le87270NQCT	16-pin QFN Green Package	Tape and Reel

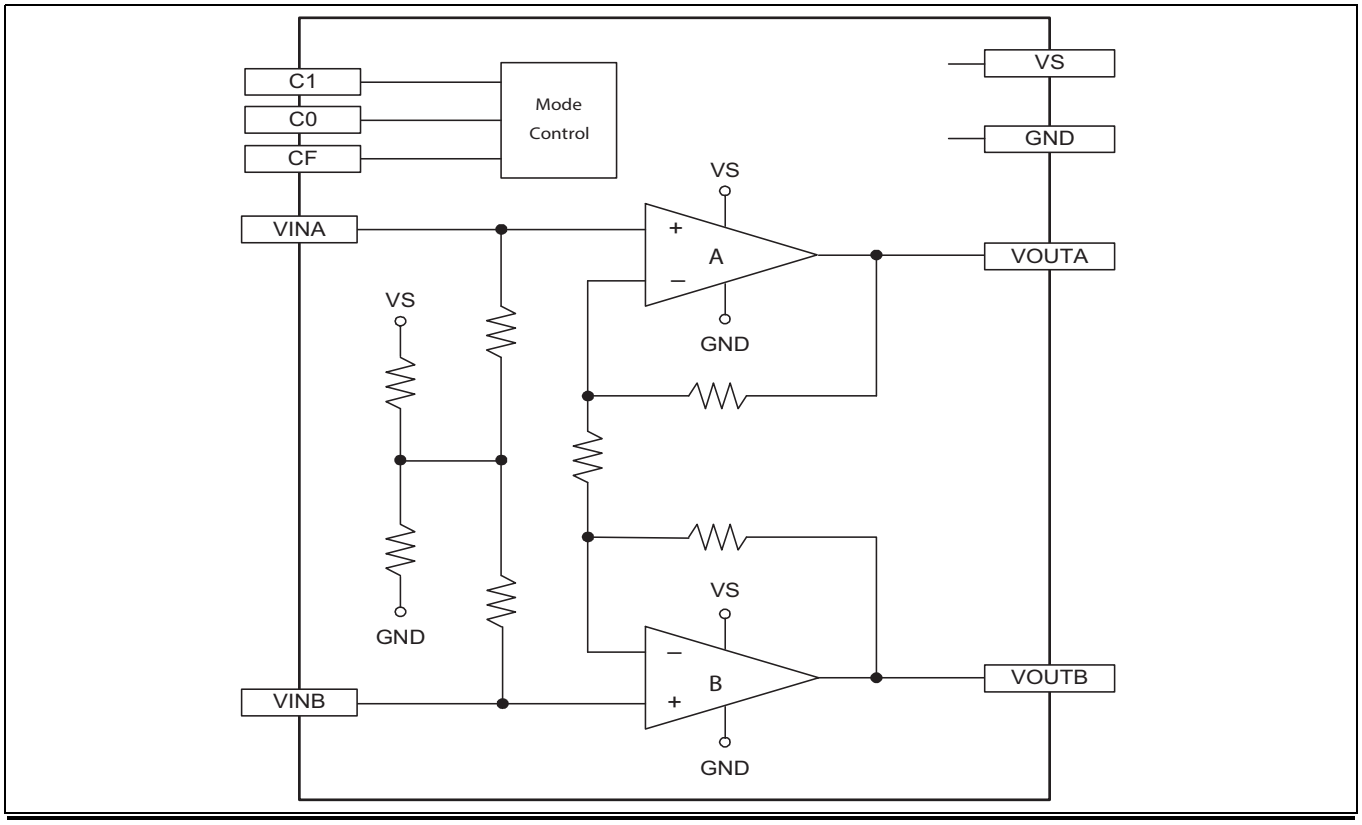
The green package meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

The line driver gain is fixed internally. The amplifiers are powered from a single supply.

Control pins can be used to adjust the supply current to one-of-three or one-of-seven preset Bias level states and a Standby state. The control pins respond to input levels that can be generated with a standard tri-state GPIO.

The Le87270 is available in a 16-pin (4 mm x 4 mm) QFN package with exposed pad for enhanced thermal conductivity.

BLOCK DIAGRAM



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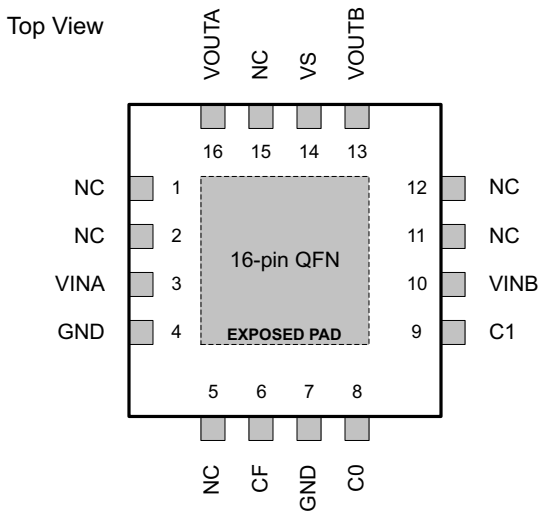
CONNECTION DIAGRAM



Notes:

1. *Pin 1 is marked for orientation.*
2. *The Le87270 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation. It is electrically isolated and maybe connected to GND.*

PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
1	NC		No internal connection
2	NC		
3	VINA	Input	Non-inverting input of amplifier A
4	GND	Ground	Reference ground
5	NC		No internal connection
6	CF	Input	Digital mode control - Fine Bias steps
7	GND	Ground	Reference ground
8	C0	Input	Digital mode control 0
9	C1	Input	Digital mode control 1
10	VINB	Input	Non-inverting input of amplifier B
11	NC		No internal connection
12	NC		
13	VOUTB	Output	Amplifier B output
14	VS	Power	Power supply, +12 V
15	NC		No internal connection
16	VOUTA	Output	Amplifier A output
	Exposed pad		Electrically isolated thermal conduction pad, can be grounded

ABSOLUTE MAXIMUM RATINGS

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-65 \le T_A \le +150°C$
Operating Junction Temperature (Note 1)	$T_A \le +150°C$
VS with respect to GND	–0.3 V to +16 V
Driver inputs (VINA, VINB)	GND to VS
Control inputs with respect to GND	–0.3 V to 4 V
Continuous Driver Output Current	75 mA
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

Note:

1. Continuous operation above 145°C junction temperature may degrade device reliability.

Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 Table 4 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Microsemi guarantees the performance of this device over the industrial (-40°C to 85°C) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled with periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Ambient temperature	T_A	-40°C to +85°C
Power Supply	VS with respect to GND	+12 V ± 5%

DEVICE SPECIFICATIONS

Typical Conditions: As shown in the basic test circuit (Figure 1) with VS = +12 V and T_A = 25°C.

Min/Max Parameters: T_A = -40 to +85°C

Table 1. Electrical Specifications

Symbol	Parameter Description	Condition	Min	Typ	Max	Unit	Notes
Supply Current Characteristics							
I_{VS}	Total Supply Current	High Bias	30	40	50	mA	1
		Medium Bias	23	33	38	mA	
		Low Bias	11	15	19	mA	
		Standby	400	500	650	µA	
Control Input (C0, C1, CF) Level Specifications							
V_{IH}	Input High Voltage		2.0			V	
V_{IL}	Input Low Voltage				0.8	V	
I_{IH}	Input High Current	C0/1 = 3.3 V	10	66	100	µA	2
		CF = 3.3 V	0	0.02	10.0	µA	
I_{IL}	Input Low Current	C0/1 = 0 V	0	0.1	10.0	µA	3
		CF = 0 V	10	50	100	µA	
Amplifier Output Characteristics							
	Differential Gain	VOUT/VIN	5.35	5.50	5.60	V/V	
V_O	Output Voltage		9.5	10		V	
I_O	Output Current		300			mA	4
Amplifier Dynamic Characteristics							
BW	-3 dB Bandwidth	Default bias state		80		MHz	
SR	Slew rate	Default bias state		1100		V/µs	
Noise	Output Voltage Noise	Differential, Default bias state			90	nV/$\sqrt{Hz}$	4
MTPR	Multi Tone Power Ratio	ADSL2, 25 – 138 kHz VDSL2 17a US0 band, 25 – 138 kHz VDSL2 17a US1 band, 3.75 – 5.2 MHz VDSL2 17a US2 band, 8.5 – 12.0 MHz VDSL2 30a US1 band, 3.75 – 5.2 MHz VDSL2 30a US2 band, 8.5 – 12.0 MHz VDSL2 30a US3 band, 22.8 – 30.0 MHz		85 80 74 66 65 60 55		dBc	
THD	Total Harmonic Distortion	Default bias state 200 kHz, 10 MHz 20 MHz 30 MHz		 -89 -75 -72 -71		dBc	

Notes:

1. *Bias states as selected from Table 2.*
2. *Current going into the control pins.*
3. *Current coming out of the control pins.*
4. *Not tested in production. Guaranteed by characterization and design.*

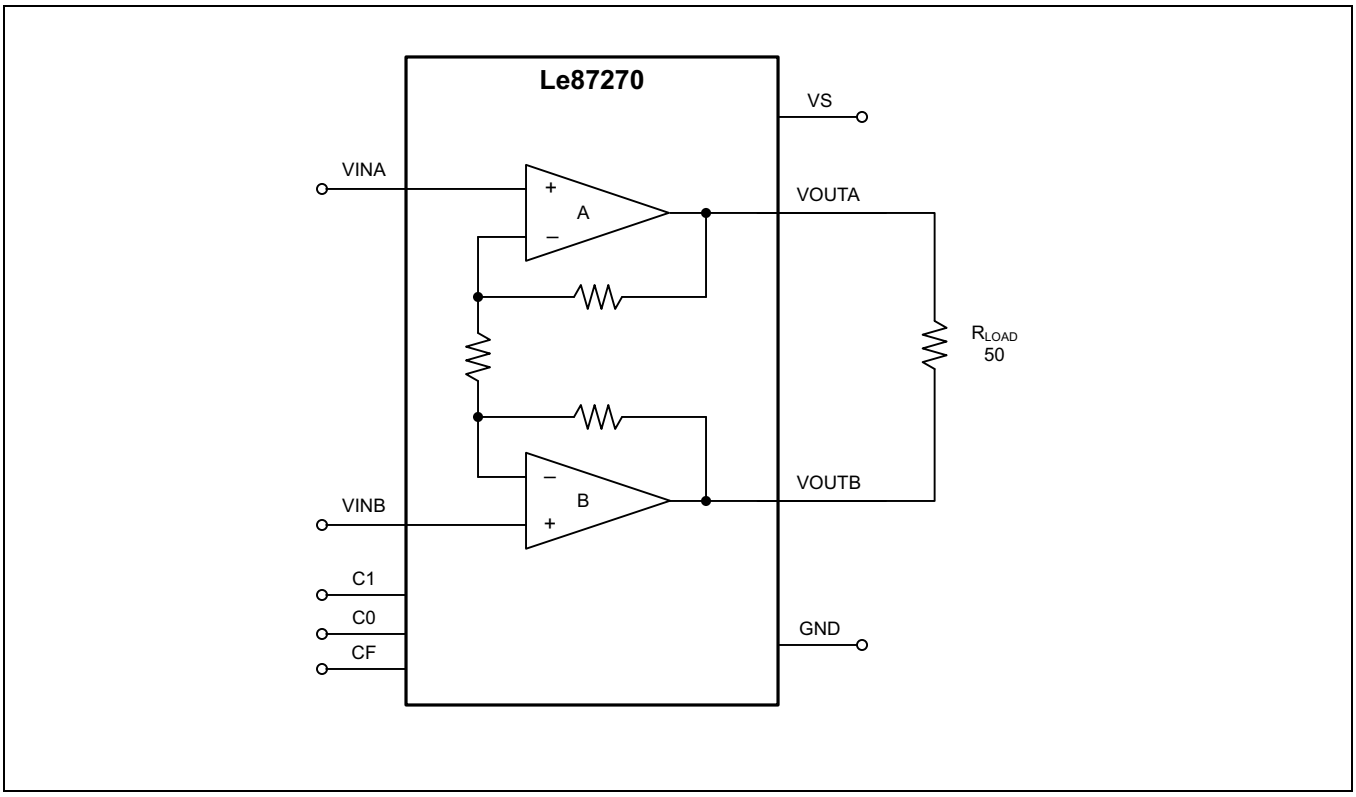


Figure 1. Basic Test Circuit

STATE CONTROL

C1, C0, and CF pins are used as combinatorial logic inputs to control the line driver operating states. The device can be programmed for 4-state or 8-state operation by controlling two or all three of these inputs.

Table 2 shows the four states that are available when programming the device using Control 0 and Control 1 pins, a Standby state and three bias states can be programmed.

Table 3 shows the eight states that are available with the addition of the fine state control, CF. 8-state operation provides the user with finer bias current steps, including bias steps above and below the 4-state matrix levels. Bias levels increment higher in a linear fashion from step 1 up to step 7. The comparable 4-state matrix states are shown in red.

C0 and C1 have internal pull-down resistors and CF has an internal pull-up resistor to force the default state (as shown in the tables) when no inputs are driven and to allow 4-state control when CF is not used.

Table 2. 4-State Control Matrix

C1	C0	State	Application
0	0	High Bias (Default state)	VDSL2 30a
0	1	Medium Bias	VDSL2 17a
1	0	Low Bias	ADSL2+
1	1	Standby	—

Table 3. 8-State Control Matrix

C1	C0	CF	State	Application
0	0	0	Bias Level 7 (Full bias)	—
0	0	1	Bias Level 6 (Default state)	VDSL2 30a
0	1	0	Bias Level 5	—
0	1	1	Bias Level 4	VDSL2 17a
1	0	0	Bias Level 3	—
1	0	1	Bias Level 2	ADSL2+
1	1	0	Bias Level 1 (Lowest bias)	—
1	1	1	Standby	—

Standby State: Amplifiers are disabled. Output port presents the impedance of the internal feedback resistors (several kilohms). Device draws lowest current from VS supply.

Bias States: Line Driver is active for transmission. States are different only in the amount of bias current to the amplifiers, and therefore power consumption. There is a trade-off between bias current and bandwidth.

APPLICATIONS

The Le87270 integrates a set of high-power line driver amplifiers that can be connected for full duplex differential line transmissions. The amplifiers are designed to be used with signals up to 30 MHz with low signal distortion.

Typical Application Circuit

A typical VDSL2 application interface circuit is shown in Figure 2.

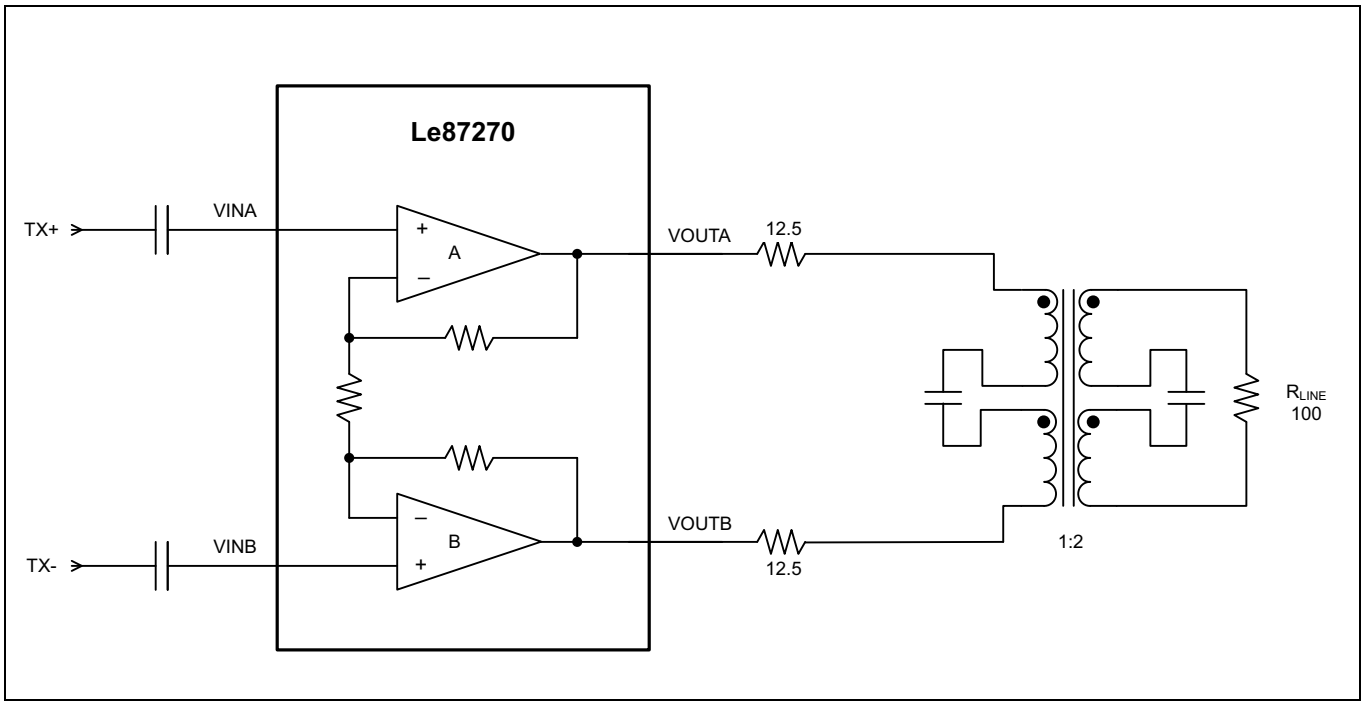


Figure 2. Typical Application Circuit

Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

Output Driving Considerations

The internal metallization is designed to carry up to about 75 mA of steady DC current and there is no current limit mechanism. Driving lines with no series resistor is not recommended.

If a DC current path exists between the two outputs, a large DC current can flow. To avoid DC current flow, the most effective solution is to place a DC blocking capacitor in series at the output, as shown in Figure 2.

Power Supplies and Component Placement

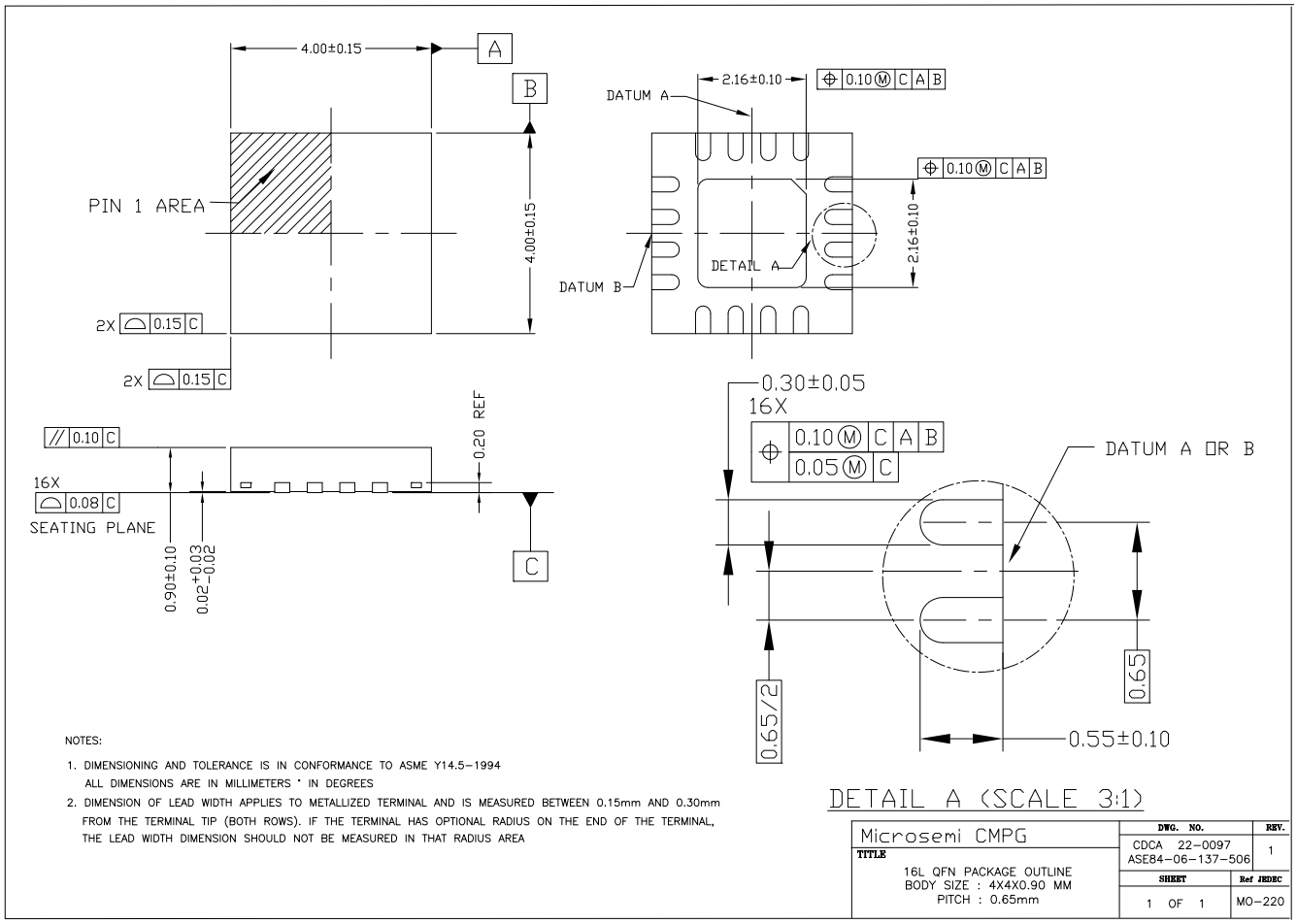
The power supplies should be well bypassed close to the Le87270 device. A 2.2 µF tantalum capacitor and a 0.1 µF ceramic capacitor for the VS supply is recommended.

Line Driver Protection

High voltage transients such as lightning can appear on the telephone lines. Transient protection devices should be used to absorb the transient energy and clamp the transient voltages. The series output termination resistors limit the current going into the line driver and internal clamps. The protection scheme depends on the type of data transformer used and the line protection components used in the front of the data transformer.

PHYSICAL DIMENSIONS

16-pin QFN



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