Le87286

Datasheet

212 MHz G.Fast Single Channel Line Driver

Preliminary

June 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in June 2019. The following is a summary of the changes in revision 3.0 of this document.

- Item 1: Transmission State Specifications (see page 9) table values modified.
- Item 2: RX0 State Specifications (see page 10) table values modified.
- Item 3: RX1 State Specifications (see page 10) table values modified.
- Item 4: Disable State Specifications (see page 11) table values modified.

1.2 Revision 2.0

Revision 2.0 was published in October 2018. The following is a summary of the changes in revision 2.0 of this document.

- Item 1. Pin Descriptions section moved to Chapter 3 (see page 4).
- Item 2. Function Descriptions content moved to Chapter 4, Operating States (see page 6).
- Item 3. G.Fast Applications section removed.
- Item 4. Chapter 6, Applications (see page 13) added.
- Item 5. Typical Application Circuit (see page 13) section added.
- Item 6. Thermal Resistance ratings moved from Absolute Maximum Ratings (see page 8) table to Thermal Resistance Ratings (see page 8) table.
- Item 7. Operational Parameters section changed to Device Specifications (see page 9) section.
- Item 8. Typical conditions in Device Specifications (see page 9) section modified.
- Item 9. Transmission State Specifications (see page 10) table values modified.
- Item 10. RX0 State Specifications (see page 10) table values modified.
- Item 11. RX1 State Specifications (see page 10) table values modified.
- Item 12. Disable State Specifications (see page 11) table values modified.
- Item 13. Timing Specifications (see page 11) table notes modified.
- Item 14. Expected MTPR Performance Specifications (see page 12) table values and notes modified.
- Item 15. Design Considerations chapter content moved to Chapter 6, Applications (see page 13).
- Item 16. Power Supplies and Component Placement section removed.
- Item 17. RREF Adjustment (see page 14) section moved within the chapter.
- Item 18. Fault Protection (see page 14) section content modified.

1.3 Revision 1.0

Revision 1.0 was published in February 2018. It was the first publication of this document.

2 Product Overview

The Le87286 is a single channel line driver designed for home gateway applications. It supports transmission of G.Fast signals with very low power dissipation. The Le87286 contains a pair of wideband amplifiers designed with Microsemi's HV15S Bipolar SOI process for low power consumption.

The line driver gain is fixed internally with two programmable gain levels. The amplifier are powered from a single power supply. When a gain level is selected, the device can be programmed to one of three Transmit (TX) states, Receive (RX) states or the Disable state.

The Le87286 is available in a 16-pin (4 mm x 4 mm) QFN package with exposed pad for enhanced thermal conductivity.

2.1 Features

- Supports high frequency (upto 212 MHz) G.Fast transmission
- Very low power dissipation
  - Class AB operation
- 2 programmable gain levels
- 3 programmable transmit (TX) states and associated Receive (RX) states
- No external gain resistors required
- Small footprint package
  - 16-pin (4 mm x 4 mm) QFN
- RoHS compliant

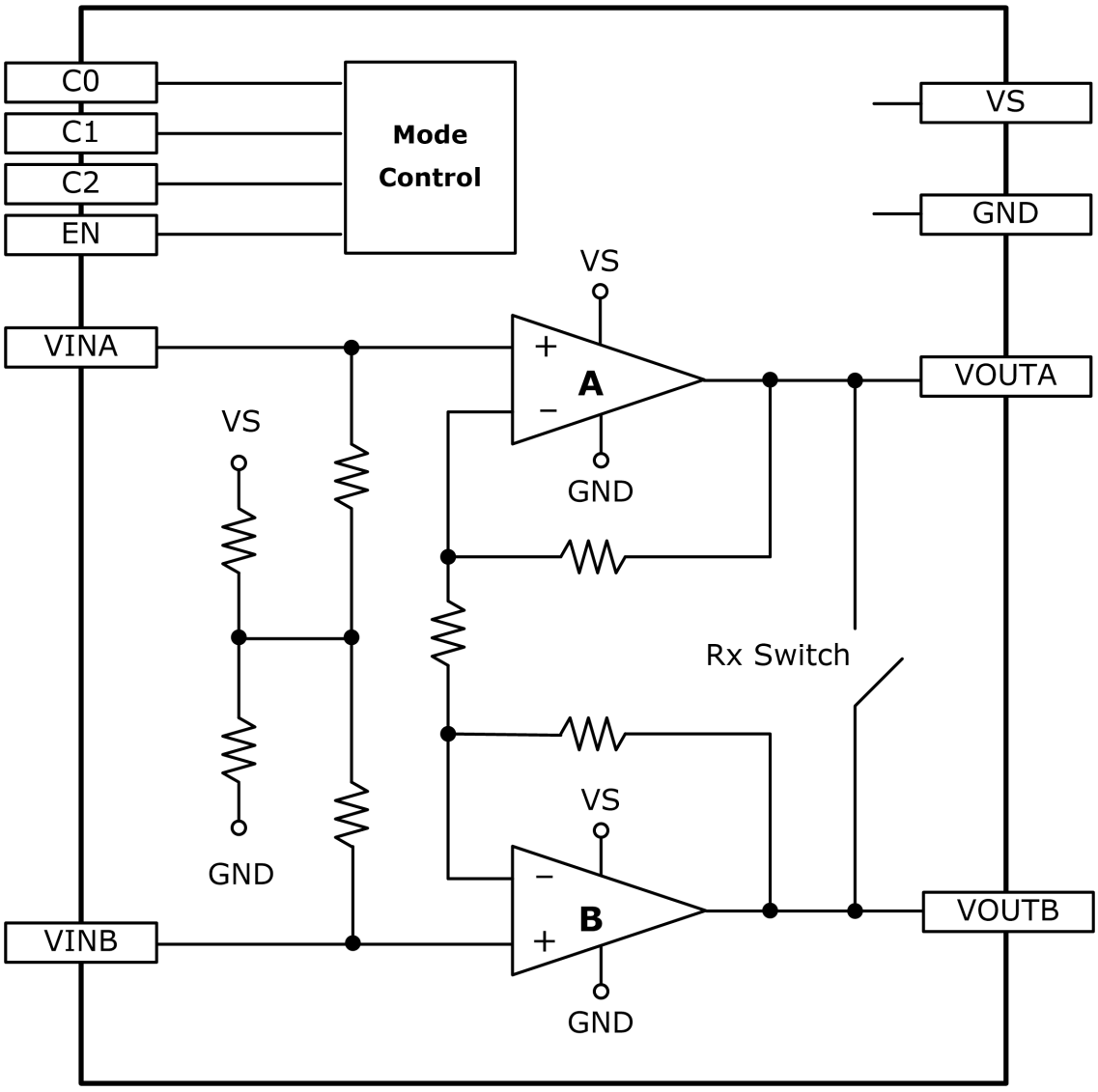
2.2 Applications

- G.Fast Line Driver
- VDSL2 Line Driver
- ADSL2+ CPE Line Driver

2.3 Block Diagram

The following figure illustrates a simplified block diagram of the Le87286 device.

Figure 1 • Le87286 Block Diagram



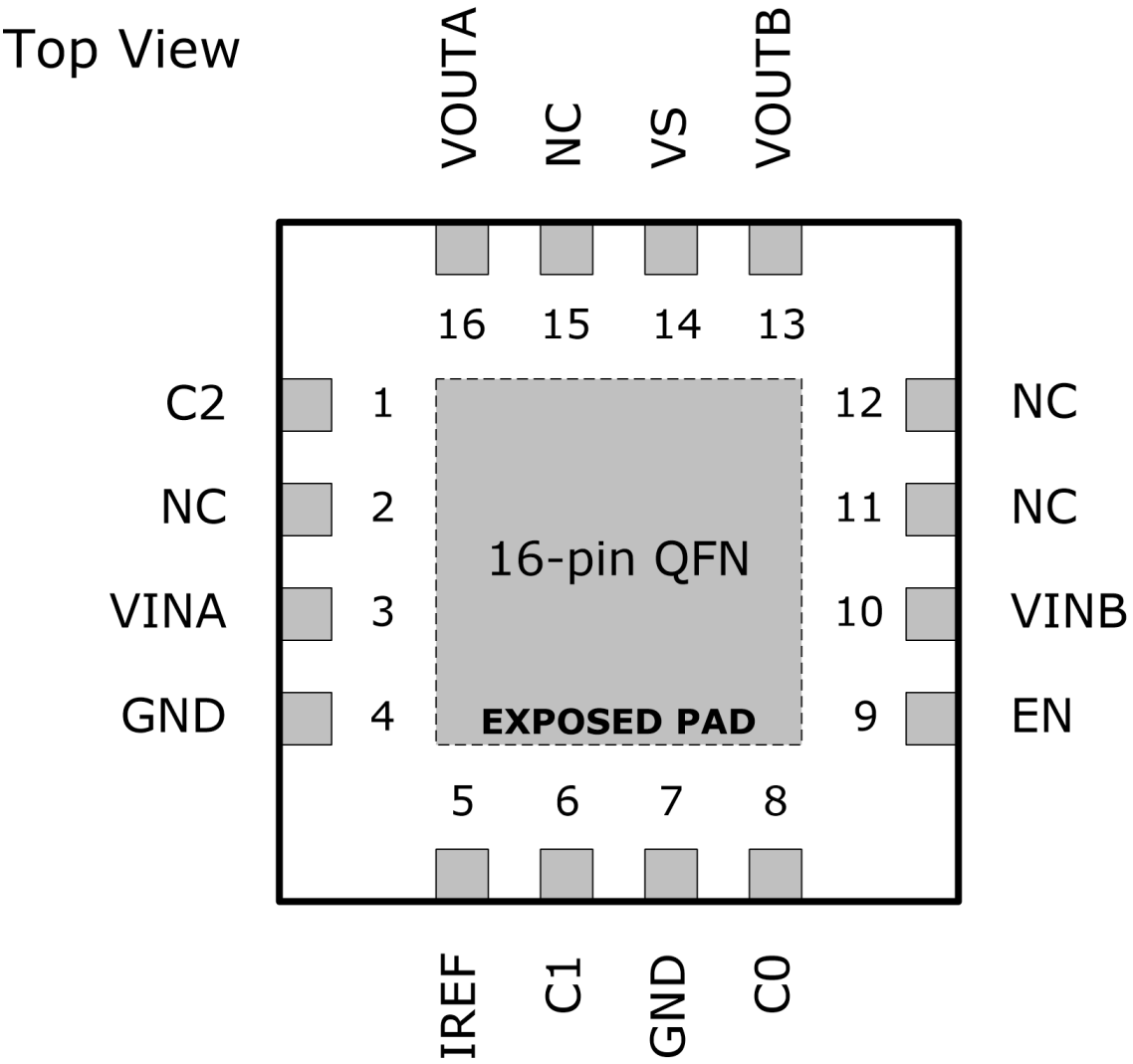
3 Pin Descriptions

This section shows the 16 pins of the Le87286 device.

3.1 Pin Diagram

The following figure illustrates the representation of the Le87286 device, as seen from the top view.

Figure 2 • Pin Diagram



Note: Pin 1 is marked for orientation. The Le87286 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation. It is electrically isolated and may be connected to ground.

3.2 Pin List

The following table lists the pin descriptions of the Le87286 device.

Table 1 • Le87286 Pin Descriptions

Number	Name	Type	Description
1	C2		State control signal
2	NC		No internal connection
3	VINA	Input	Non-inverting input of amplifier A
4	GND	Ground	Reference ground
5	IREF	Input	Device internal reference current. Connect a resistor (RREF) to GND.
6	C1	Input	State control signal
7	GND	Ground	Reference ground
8	C0	Input	State control signal
9	EN	Input	Output enable signal
10	VINB	Input	Non-inverting input of amplifier B
11	NC		No internal connection
12	NC		No internal connection
13	VOUTB	Output	Amplifier B output
14	VS	Power	Power supply, 12 V
15	NC		No internal connection
16	VOUTA	Output	Amplifier A output
	Exposed Pad		Electrically isolated thermal conduction pad; can be grounded.

4 Operating States

The operating state is controlled through four input pins: EN, C0, C1, and C2.
The input pin C2 has an internal pull-up resistor. If it is left undefined, it is effectively a logic high. The other inputs have internal pull-down resistors. The following table lists the operating states.

Table 2 • Operating State Control

EN	C2	C1	C0	State	Gain	Zout	Amplifier
x	0	0	0	Disable		High	Off
0	0	0	1	RX0		High	Off
0	0	1	0	RX0		High	Off
0	0	1	1	RX0		High	Off
1	0	0	1	TX1	High		On
1	0	1	0	TX2	High		On
1	0	1	1	TX3	High		On
x	1/Open	0	0	Disable		High	Off
0	1/Open	0	1	RX1		Low	Off
0	1/Open	1	0	RX1		Low	Off
0	1/Open	1	1	RX1		Low	Off
1	1/Open	0	1	TX1	Low		On
1	1/Open	1	0	TX2	Low		On
1	1/Open	1	1	TX3	Low		On
x	x	x	x	Thermal shut-down	x	x	Off

4.1 Disable State

Line driver amplifiers are turned off, and there is no gain from VIN to VOUT. The amplifier outputs are high-impedance. The gain-setting resistors around the amplifiers remain in place and present a differential impedance at the VOUT pins. The line driver will cause minimal signal distortion on the line when in the disable state. This state uses the lowest power.

4.2 RX0 State

RX0 state presents the same features as Disable state. RX0 state has reduced distortion of RX signals on the line and uses more power than Disable state.

4.3 RX1 State

Line driver amplifiers are turned off and there is no gain from VIN to VOUT. A short is applied across VOUTA-VOUTB, providing a low differential output impedance.

4.4 TX States

In TX states the amplifiers are fully active with gain from VIN to VOUT. The TX states provide three different levels of bias current to the amplifiers. This allows some choice of power versus linearity in the line driver performance.

4.5 Thermal Shut-Down State

The Thermal Shut-Down state (TSD) is activated at high silicon temperature. Amplifiers are turned off. The RX switch is unaffected. There is hysteresis in the TSD temperature threshold. After the silicon cools below the threshold, the line driver returns to the operating state indicated by the control inputs.

5 Electrical Specifications

This section shows the absolute maximum ratings and electrical specifications for the Le87286 device.

5.1 Absolute Maximum Ratings

Stresses above the values listed in the following table of absolute maximum ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Table 3 • Absolute Maximum Ratings

Parameter	Value
Storage temperature	–65 °C ≤ T_A ≤ 150 °C
Operating junction temperature[1]	–40 °C ≤ T_J ≤ 150 °C
VS with respect to GND	–0.3 V to 13.5 V
Control inputs with respect to GND	–0.3 V to 4 V
Continuous driver output current	100 mA
ESD immunity, human body model (HBM)	JESD22 Class 2 compliant
ESD immunity, charged device model (CDM)	JESD22 Class IV compliant

1. Continuous operation above 145 °C junction temperature may degrade device reliability.

5.2 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

The following table lists the thermal resistance ratings of the Le87286 device.

Table 4 • Thermal Resistance Ratings

Parameter	Value
Maximum device power dissipation, continuous , T_A = 85 °C, P_D	1.0 W
Junction to ambient thermal resistance[1], Θ_{JA}	52.0 °C/W
Junction to board thermal resistance, Θ_{JB}	26.0 °C/W
Junction to case bottom (exposed pad) thermal resistance, $\Theta_{JC\ (BOTTOM)}$	14.6 °C/W
Junction-to-top characterization parameter, Ψ_{JT}	3.1 °C/W

1. No air flow.

5.3 Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

See IPC/JEDEC J-Std-020 Table 4 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

5.4 Operating Ranges

Microsemi guarantees the performance of this device over the industrial (–40 °C to 85 °C) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled with periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

The following table lists the operating range of the Le87286 device.

Table 5 • Operating Range

Parameter	Condition	Value
Ambient temperature	T_A	–40 °C to 85 °C
Power supply	VS with respect to GND	8.5 V to 13.2 V

5.5 Device Specifications

Typical values are characteristic of the device and are the result of engineering evaluation. Typical values are for information purposes only and are not part of the testing requirement. Minimum and maximum values apply across the operating temperature range and the entire supply range unless otherwise specified.

Typical Conditions: VS = 12 V, RREF = 54.9 kΩ, RL = 80 Ω, and T_A = 25 °C.
Min/Max Parameters: T_A = –40 °C to 85 °C.
For more information see section Basic Test Circuit (see page 12).

The following table lists the specifications for the transmission states.

Table 6 • Transmission State Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
IVSq	25.9	30.5	35.1	mA	TX1 state
	33.5	39.4	45.3	mA	TX2 state
	41.0	48.2	55.4	mA	TX3 state
Power[1], TX3		610		mW	106 MHz, 4 dBm
		640		mW	106 MHz, 8 dBm
		620		mW	212 MHz, 4 dBm

Parameter	Min.	Typ.	Max.	Unit	Condition
		660		mW	212 MHz, 8 dBm
Maximum VOUT	8.5			Vpk	
Maximum IOUT	130			mApk	
Input-referred noise[1]		4.0	6.0	nV/√Hz	>2 MHz, C2 = 1
		2.7	4.0	nV/√Hz	>2 MHz, C2 = 0
Gain, VOUT/VIN	8.25	8.5	8.75	V/V	C2 = 1
	16.8	17.7	18.6	V/V	C2 = 0
Bandwidth[1]		460		MHz	–3 dB, C2 = 1
		430		MHz	–3 dB, C2 = 0
Gain flatness[1, 2]	–1		0	dB	2 MHz–106 MHz
	–2.5		–1	dB	106 MHz–212 MHz
Input impedance	10			kΩ	Differential, 2 MHz
Output impedance[1]		1		Ω	Differential, 2 MHz
PSRR[1]		45		dB	100 kHz–212 MHz
Thermal shut-down threshold[1]		170		°C	
Thermal shut-down hysteresis[1]		20		°C	

1. Not tested in production. Guaranteed by design and characterization.
2. Referencing gain at two MHz.

The following table lists the RX0 state specifications.

Table 7 • RX0 State Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
IVSq	2.0	2.3	2.6	mA	
Power[1]			30	mW	Pline = 8 dBm
Output noise[1]			4	nV/√Hz	100 kHz–212 MHz
Output impedance[1]		1100		Ω	Differential, 100 kHz–50 MHz
PSRR[1]		45		dB	100 kHz–212 MHz

1. Not tested in production. Guaranteed by design and characterization.

The following table lists the RX1 state specifications.

Table 8 • RX1 State Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
IVSq	0.7	1.0	1.3	mA	
Power[1]			18	mW	Pline = 8 dBm
Output current sink[1]	85			mApk	
Output noise[1]			4	nV/√Hz	100 kHz–212 MHz
Output impedance[1]			8	Ω	Differential, 100 kHz–50 MHz
PSRR[1]		45		dB	100 kHz–212 MHz

1. Not tested in production. Guaranteed by design and characterization.

The following table lists the disable state specifications.

Table 9 • Disable State Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
IVSq	0.7	1.0	1.3	mA	
Power[1]			15	mW	Pline = 8 dBm
Output noise[1]			4	nV/√Hz	100 kHz–212 MHz
Output impedance		1100		Ω	Differential
PSRR[1]		45		dB	100 kHz–212 MHz

1. Not tested in production. Guaranteed by design and characterization.

The following table lists the control interface specifications. It lists Input High Voltage (V_{IH}), Input Low Voltage (V_{IL}), Input High Current (I_{IH}), Input Low Current (I_{IL}), and Input Impedance (Z_{IN}) for logic inputs of C0, C1, C2, and EN.

Table 10 • Control Interface Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	2.0			V	
V_{IL}			0.8	V	
I_{IH}	100		200	µA	V_{IH} = 3 V, C0, C1, EN
	–20		20	µA	V_{IH} = 3 V, C2
I_{IL}	–30		0	µA	V_{IL} = 0 V
Z_{IN}		20		kΩ	C0, C1, EN
		200		kΩ	C2

The following table lists the timing specifications.

Table 11 • Timing Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
Switching time[1]			400	ns	Any RX state
Switching time[1]			400	ns	Any TX state
Switching time[1]			2	µs	Any Disable state

1. Not tested in production. Guaranteed by design and characterization.

The powers of a given missing tone and the power of the tone right next to it are measured. The calculated difference of the two power levels is the Missing Tone Power Ratio (MTPR) of that given missing tone. All MTPR numbers within a given band are mathematically averaged to produce the MTPR number listed in the following table.

The source file is created with one tone missing every 32 tones. The Peak-to-Average Ratio (PAR) is 5.3 Vpk/Vrms. For the four dBm case, the Power Spectral Density (PSD) is even across the transmission band. For the eight dBm case, PSD below 30 MHz is eight dB higher than PSD above 30 MHz.

Table 12 • Expected MTPR Performance Specifications

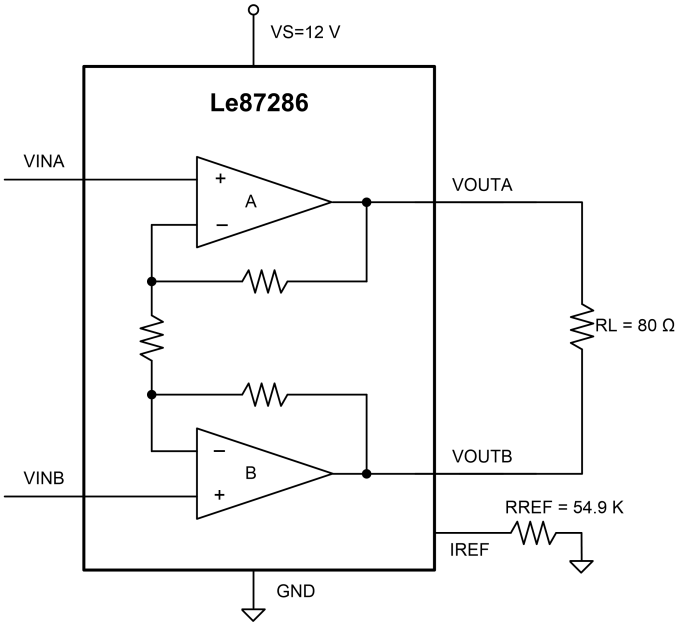
Parameter	Min.	Typ.	Max.	Unit	Condition
MTPR, 4 dBm, 212 MHz, TX3[1]		–58		dBc	2 MHz–30 MHz
		–54		dBc	30 MHz–106 MHz
		–51		dBc	106 MHz–160 MHz
		–50		dBc	160 MHz–212 MHz
MTPR, 8 dBm, 106 MHz, TX3[1]		–65		dBc	2 MHz–30 MHz
		–54		dBc	30 MHz–106 MHz
MTPR, 4 dBm, 212 MHz, 6.8 PAR[1]		–76	–70	dBc	RX0 state
		–76	–70	dBc	RX1 state
		–50		dBc	Disable state
MTPR, 8 dBm, 106 MHz, 6.8 PAR[1]		–75	–70	dBc	RX0 state
		–68	–66	dBc	RX1 state
		–50		dBc	Disable state

1. Not tested in production. Guaranteed by design and characterization.

5.6 Basic Test Circuit

The following figure illustrates the basic test circuit for the Le87286 device.

Figure 3 • Basic Test Circuit



6 Applications

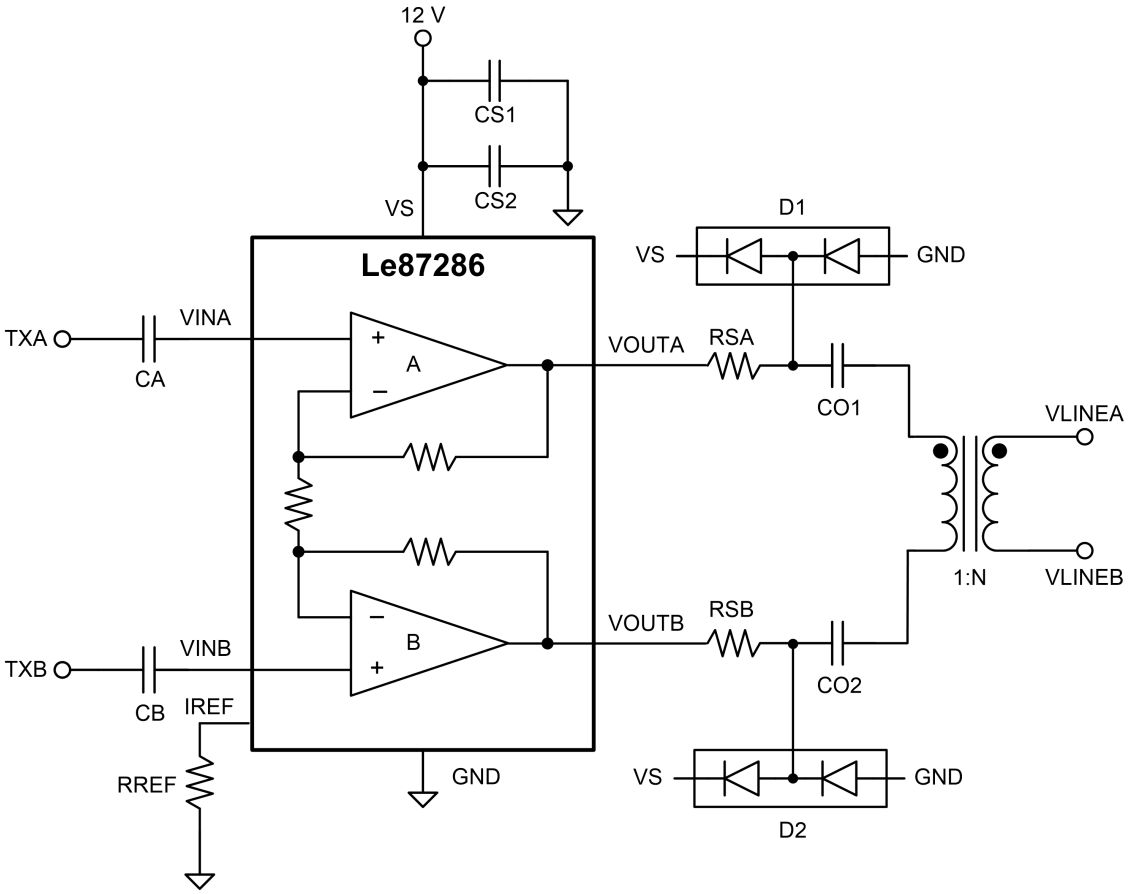
This section shows the applications of the Le87286 device.

6.1 Typical Application Circuit

The Le87286 device features two line driver amplifiers that can be connected for half-duplex differential line transmissions for G.Fast. In this application, the amplifiers are designed to be used with signals up to 212 MHz with low signal distortion.

The following figure illustrates an application circuit with amplifiers A and B in transmission for G.Fast.

Figure 4 • Typical Application Circuit for G.Fast



The following table lists the components of the typical application circuit.

Table 13 • Typical Application Circuit Elements

Name	Type	Value	Unit	Tolerance	Rating
RSA[1]	Resistor	22.1	Ω	1%	0805
RSB[1]	Resistor	22.1	Ω	1%	0805
RREF	Resistor	54.9	KΩ	1%	0402
CA	Capacitor	0.01	µF	10%	X7R, 16 V
CB	Capacitor	0.01	µF	10%	X7R, 16 V
C01[2]	Capacitor	0.01	µF	10%	X7R, 16 V
C02[2]	Capacitor	0.01	µF	10%	X7R, 16 V
CS1	Capacitor	0.1	µF	10%	X7R, 25 V
CS2	Capacitor	2.2	µF	10%	Tantalum, 25 V
D1	Diode bridge	BAV99			
D2	Diode bridge	BAV99			

1. The value of the sense resistors is associated with the turn ration of the transformer and the line impedance, typically 100 Ω. As shown, a turn ratio of 1:1.5 is assumed. A transformer with a different ratio may be used, with high or low gain of the device set by the state of C2. The value of the sense resistors may be further adjusted to take into account the equivalent impedance of the receive path.
2. The two capacitors may be combined into one and be connected between two windings of the transformer on the secondary (line drive) side.

6.2 RREF Adjustment

The 54.9 kΩ resistor on the IREF pin could be reduced to increase the line driver power and signal bandwidth for better MTPR performance. This is a design trade off and will result in greater power dissipation.

6.3 Board Capacitance

Board capacitance at pins VINx and VOUTx should be limited to 2 pF or less.

6.4 Output Driving Considerations

The internal metallization is designed to carry up to 100 mA of steady DC current and there is no current limit mechanism. The device does feature integrated thermal shutdown protection however with hysteresis. Driving lines with no series resistor is not recommended.

6.5 Fault Protection

High voltage transients such as lightning can appear on DSL lines. Transient protection devices should be used to absorb the transient energy and clamp the transient voltages. The series output termination resistors limit the current going into the line driver and internal clamps. The protection scheme depends on the type of data transformer used and the line protection components used in the front of the data transformer.

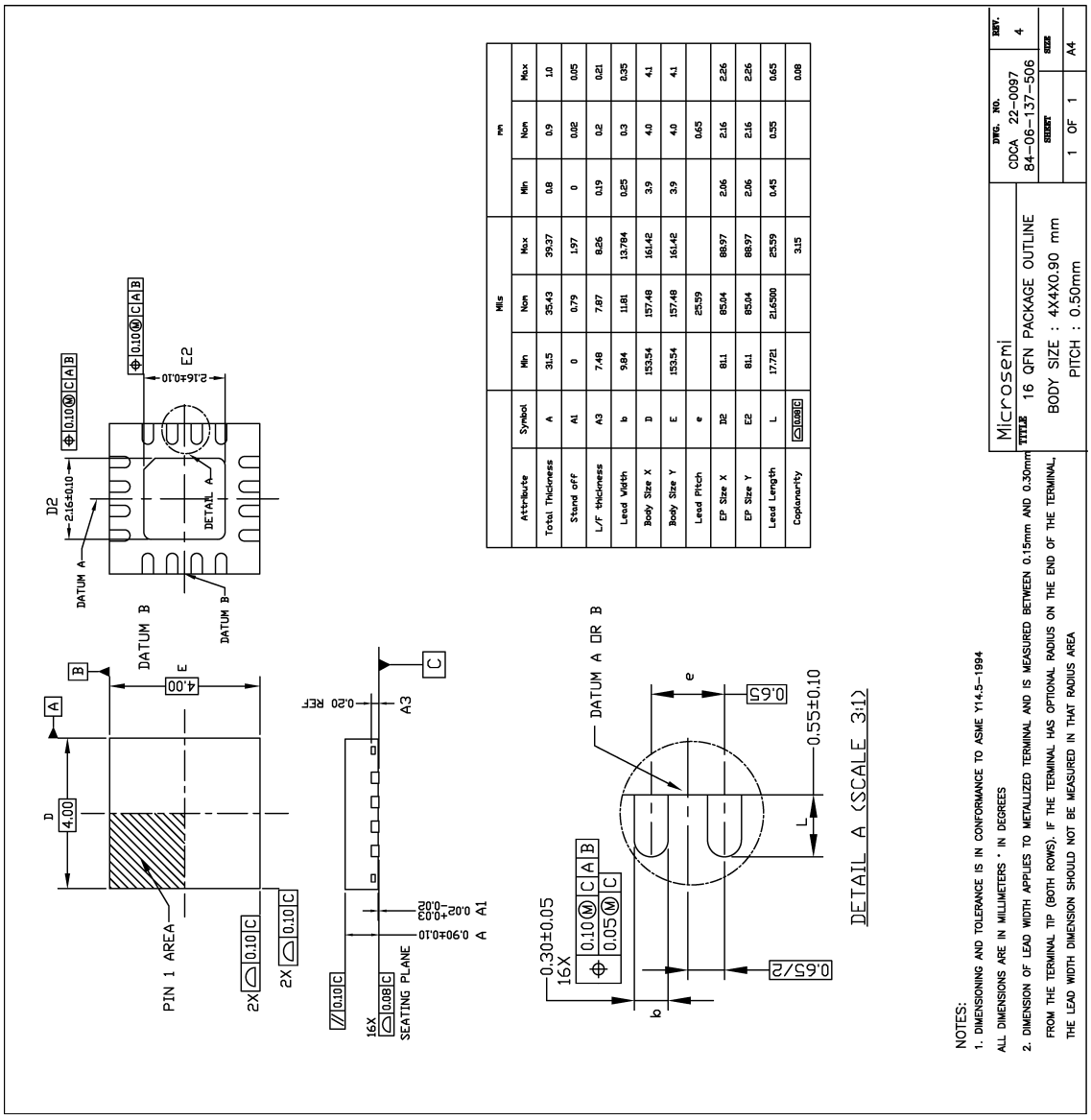
Appropriate external protection is needed for the line driver to survive K.21 surge tests.

As shown in the Figure 4 (see page 13), Typical Application Circuit for G.Fast, diode bridges may be used to clamp signals between V_S and ground. The diode bridges should be connected on the transformer side of the sense resistors. The fault current will then be dumped into VS/ground. It is possible that a capacitor will be required to be added at the diode bridge to effectively absorb fault energy.

7 Package Specification

The following figure illustrates the package drawing of the Le87268 device. Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit, or function of the device. Markings vary with the mold tool used in manufacturing.

Figure 5 • Package Drawing



8 Ordering Information

The following table lists the ordering information of the Le87286 device.

Table 14 • Ordering Information

Part Number	Description	Package
Le87286NQC	16-pin QFN green package	Tray
Le87286NQCT	16-pin QFN green package	Tape and Reel

Note: The green package meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

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