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Features

- Best in Class Density
- Dual Channel Architecture
- 28-pin, 4x5 mm QFN Package
- Low Power Operation
- Class AB Operation
- Independent Channel Enable/Disable Control
- Capable of Driving Line Impedance Between 12 Ω to 100 Ω
- Operations to 86 MHz
- RoHS Compliant

Applications

- Power Line Communications
- Home Networking
- HPNA
- G.HN

Description

The Le87502 is a 2-channel line driver designed to work in Home Plug Alliance HPAV2 systems.

Each channel can be enabled independently allowing multiple-in, multiple-out (MIMO) or single-in, single-out (SISO) operations.

When each channel is enabled, the operating level can be set to Full, 90% or 80% power. The Le87502 delivers superior performance and can drive a line impedance of 100 Ω down to 12 Ω through a proper transformer.

In addition, the Le87502 features a Standby state which forces both channels into a long-term sleep mode.

Ordering Information

Le87502MQC	28-pin QFN Green Pkg.	Tray

The green package is Halogen free and meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

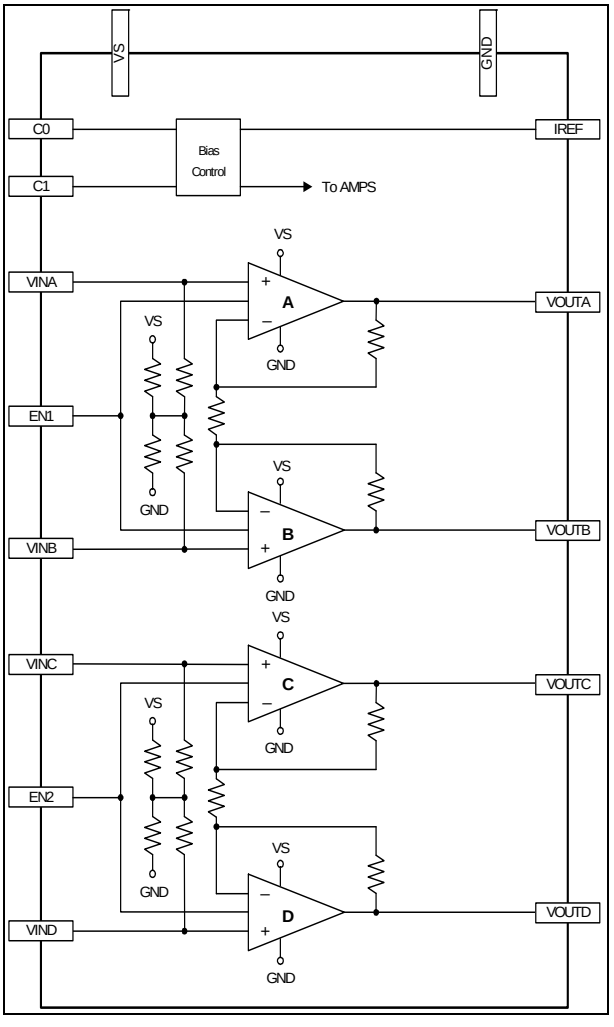

Figure 1 - Block Diagram

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Pin Diagram

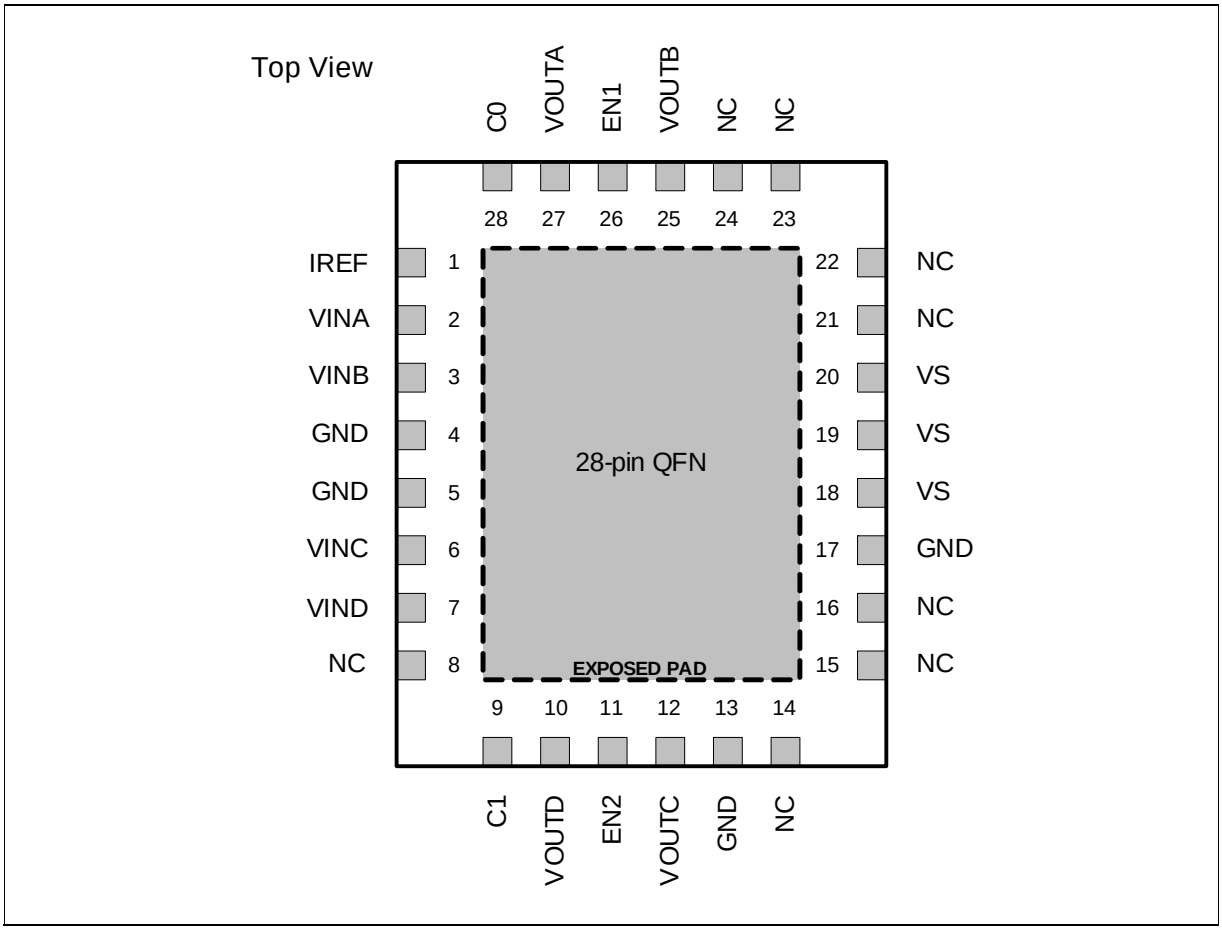


Figure 2 - Pin Diagram

Note 1: Pin 1 is marked for orientation.

Note 2: The device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias for proper heat dissipation. It is electrically isolated and may be connected to GND.

Pin Description

Pin #	Pin Name	Type	Description
1	IREF	Input	Device Internal Reference Current. Connect a resistor to GND.
2	VINA	Input	Amplifier A input
3	VINB	Input	Amplifier B input
4	GND	Ground	Low noise analog ground
5	GND		
6	VINC	Input	Amplifier C input
7	VIND	Input	Amplifier D input
8	NC		No connect
9	C1	Input	State control. Sets operation state when channel enabled.
10	VOUTD	Output	Amplifier D output
11	EN2	Input	Channel C and D Enable/Disable control
12	VOUTC	Output	Amplifier C output
13	GND	Ground	Low noise analog ground
14	NC		No connect
15	NC		
16	NC		
17	GND	Ground	Low noise analog ground
18	VS	Power	Power supply
19	VS		
20	VS		
21	NC		No connect
22	NC		
23	NC		
24	NC		
25	VOUTB	Output	Amplifier B output
26	EN1	Input	Channel A and B Enable/Disable control
27	VOUTA	Output	Amplifier A output
28	C0	Input	State control. Sets operation state when channel enabled.

Table 1 - Pin Descriptions

Absolute Maximum Ratings

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-65°C \le T_A \le +150°C$
Operating Junction Temperature	$-40°C \le T_J \le +150°C$[1]
VS to GND	-0.3 V to +16 V
Driver inputs VINA/B/C/D	VS to GND
Control inputs C0/1, EN1/2	–0.3 V to +4 V
Continuous Driver Output Current	200 mArms
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant
Note 1: Continuous operation above 145°C junction temperature may degrade device long term reliability.	

Table 2 - Absolute Maximum Ratings

Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

Operating Ranges

Microsemi guarantees the performance of this device over the 0°C to +85°C temperature range by conducting electrical characterization and a single insertion production test coupled with periodic sampling. These procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Ambient temperature	0°C to +85°C
VS with respect to GND	+10 to +15 V

Table 3 - Operation Ranges

MIMO operation has the same Device Specification as SISO operation. The difference is that more power is delivered to the line in SISO operation.

Device Specifications

Typical values are for T_A = +25°C and VS = +12 V and are provided for informational purposes only. Minimum and maximum values are tested in production, unless otherwise noted. Minimum and maximum values are over the T_A = 0°C to +85°C temperature range and supply voltage range as shown in "Operating Ranges".

The Le87502 is in the Enable Full Power state and uses the Basic Test Circuit (Figure 6), unless otherwise specified.

Refer to "Performance Characteristics" for more device performance information.

Parameter	Condition	Min.	Typ.	Max.	Unit
Power					
I_{VS} (per channel)	Quiescent, VINA/B and VINC/D floating				
	Enable Full Power State	46	52	75	mA
	Enable 90% Power State	36	46	67	mA
	Enable 80% Power State	32	40	59	mA
I_{VS} (per device)	Disable State	0.8	1.3	3.3	mA
	Standby State	0.1	0.6	2.0	mA
Control Input (C0/1, EN1/2) Characteristics					
Internal 50 kΩ pull-down on all control inputs					
V_{IH}		1.2		3.6	V
V_{IL}		-0.3		+0.6	V
I_{IH}			60	120	µA
I_{IL}			0	20	µA
Channel Input (VINA/B, VINC/D) Characteristics					
Input Offset Voltage		-35	0	+35	mV
Differential Input Impedance	VINA – VINB, VINC – VIND; at 2 MHz	12	15	18	kΩ

Table 4 - Electrical Specifications

Parameter	Condition	Min.	Typ.	Max.	Unit
Channel Output (VOUTA/B, VOUTC/D) Characteristics					
Output Voltage[1]		9.5			V
Output Current	R_{Load} = 10 Ω		600		mA
Disabled Output Impedance	Differential		1400		Ω
Channel Dynamic Characteristics					
Voltage Gain	VOUT/VIN at 1 MHz	5.5	6.5	7.5	V/V
Bandwidth	-3 dB		180		MHz
Input Referred Noise	Differential		15		nV/$\sqrt{Hz}$
MTPR	P_{Load} = 40 mW 0.5 - 30 MHz 30 - 86 MHz		 -62 -32		 dBc dBc
Enable Time	Between Disable and any Power-up state		500		ns
Disable Time			500		ns
TSD Temperature			170		°C
Note 1: Not tested in production, guaranteed by design and device characterization.					

Table 4 - Electrical Specifications

Performance Characteristics

The following graphs depict typical device performance using the Basic Test Circuit (Figure 6).

Figure 3 plots device gain performance versus frequency for Full, 90%, and 80% Power States. Performance is representative of either channel.

Figure 4 plots line driver power to the load with the device operating in the Full Power State and loaded with 40 Ω. Performance is representative of either channel.

Figure 5 plots channel 1 and channel 2 output impedance versus frequency in the disabled state.

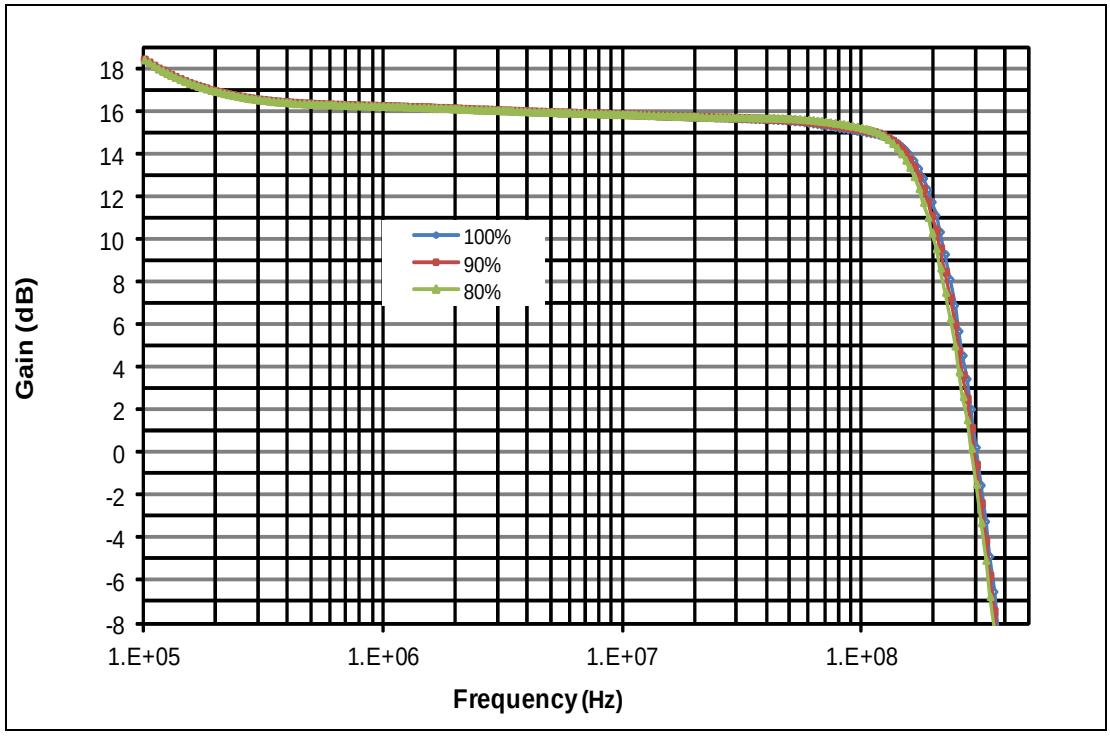


Figure 3 - Differential Gain

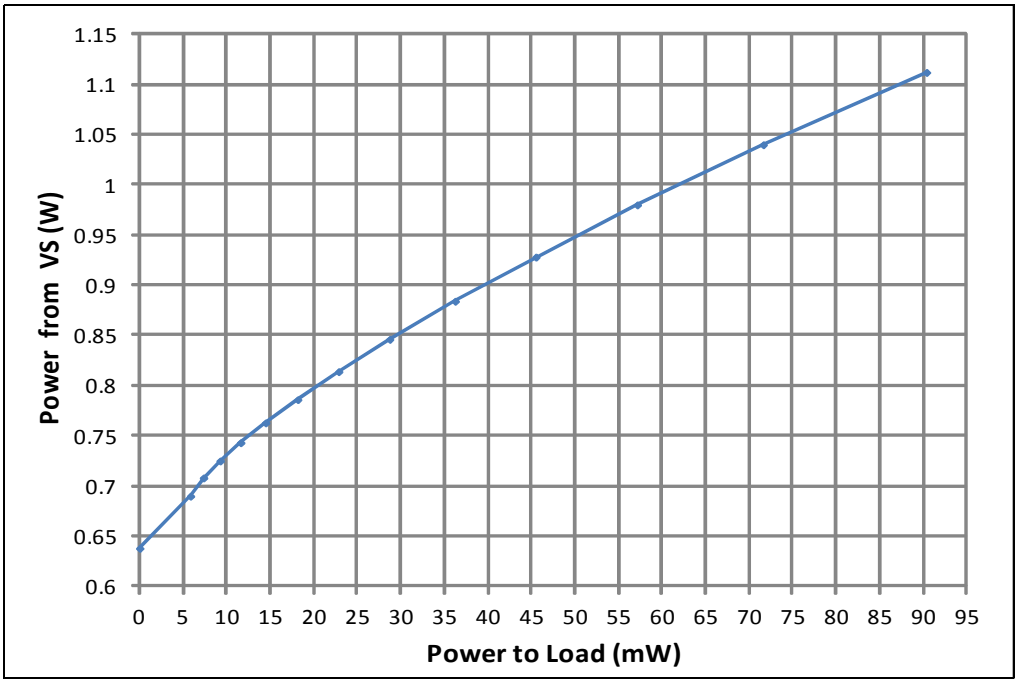


Figure 4 - Supply Power Versus Load Power

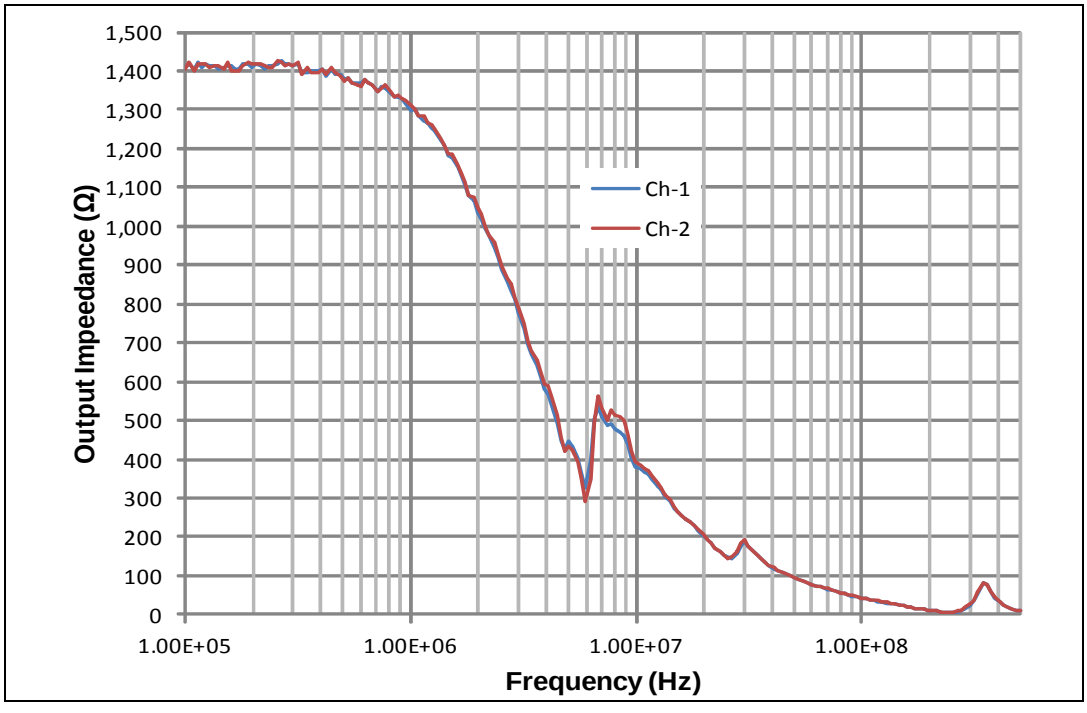


Figure 5 - Disabled Output Impedance

Test Circuit

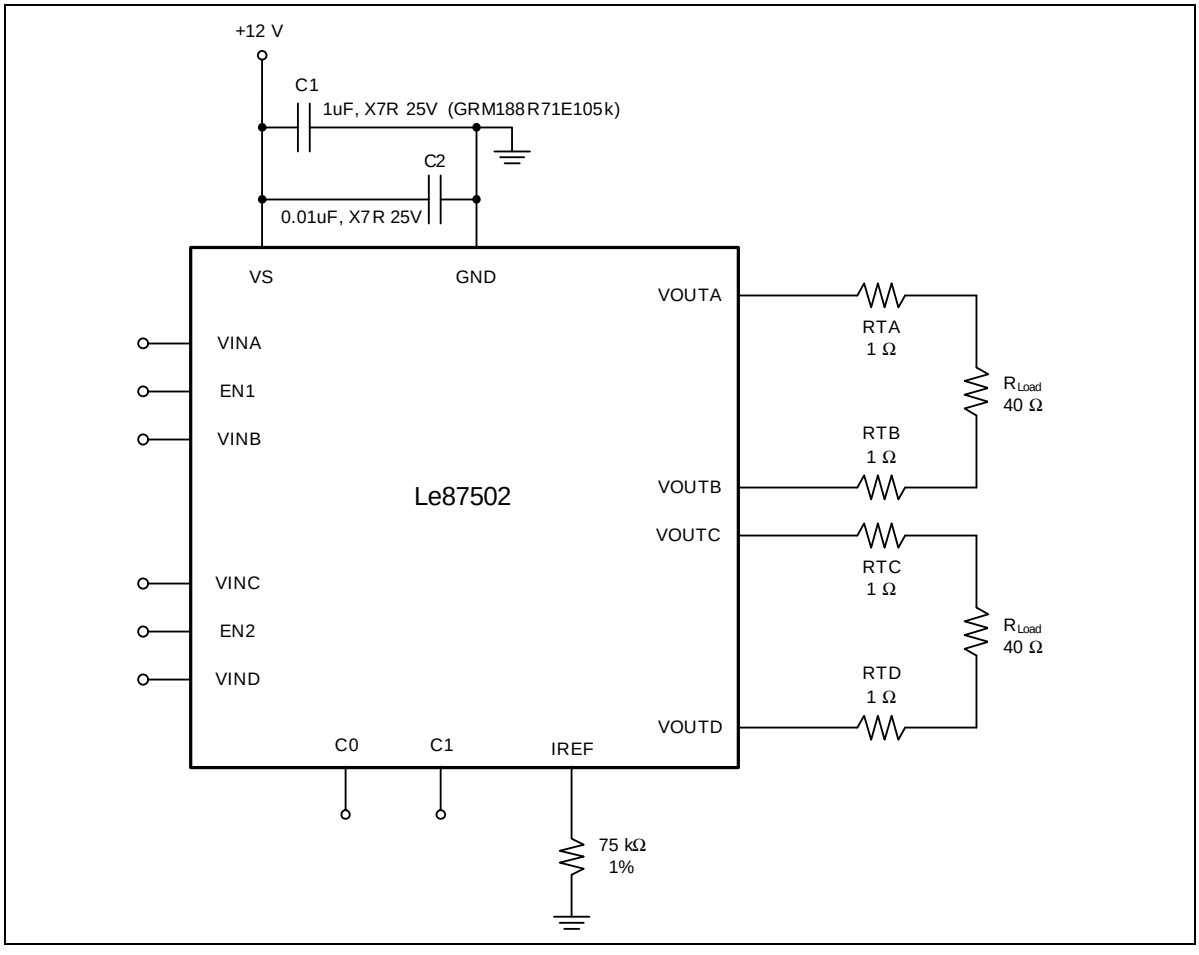


Figure 6 - Basic Test Circuit

Operation States

Operation state control is depicted in Table 5.

For active operation, each channel will either be in Enable state (Power-up mode) or Disable state (Power-down mode). A Standby state (long-term Sleep mode) is also provided.

EN1 and EN2 independently control each channel's power mode:

- EN1 = 0, channel A/B in Power-down mode; EN1 = 1, channel A/B in Power-up mode
- EN2 = 0, channel C/D in Power-down mode; EN2 = 1, channel C/D in Power-up mode

C0 and C1 control state selection and their setting applies to both channels. A setting of C0 = C1 = 0 overrides EN1/2 and places both channels in Standby state.

Standby is the default state when power is initially supplied.

EN1 or EN2	C1	C0	Device State	Mode
1	1	1	Enable Full Power	Power-up
1	0	1	Enable 90% Power	
1	1	0	Enable 80% Power	
X	0	0	Standby	Sleep
0	1	1	Disable	Power-down
0	1	0		
0	0	1		

Table 5 - Operation State Control

X = Don't care.

Applications

The Le87502 integrates two sets of high-power line driver amplifiers. The amplifiers are designed for low distortion for signals up to 86 MHz.

A typical application interface circuit (for one channel) is shown in Figure 7.

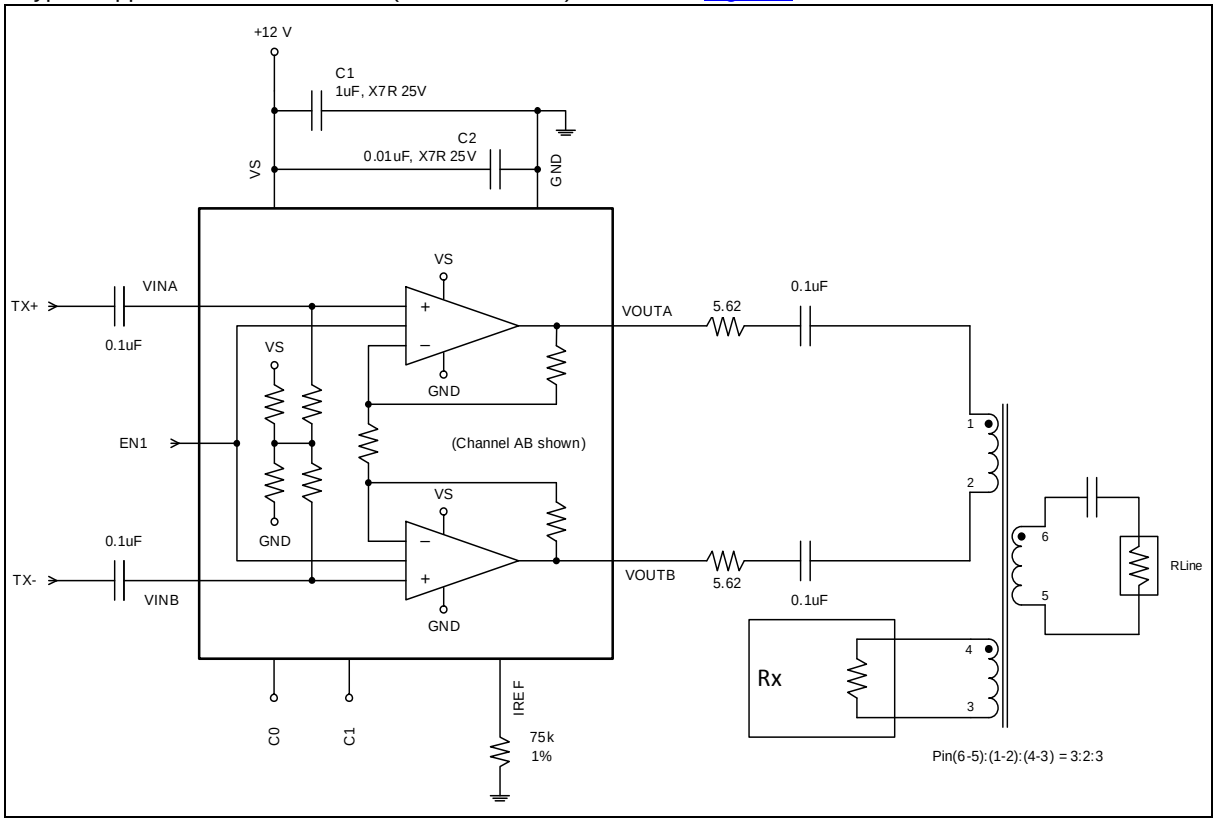


Figure 7 - Typical Application Circuit

The amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

Output Driving Considerations

The internal metallization is designed to drive 200 mArms sinusoidal current and there is no current limit mechanism. Driving lines without a series resistor is not recommended.

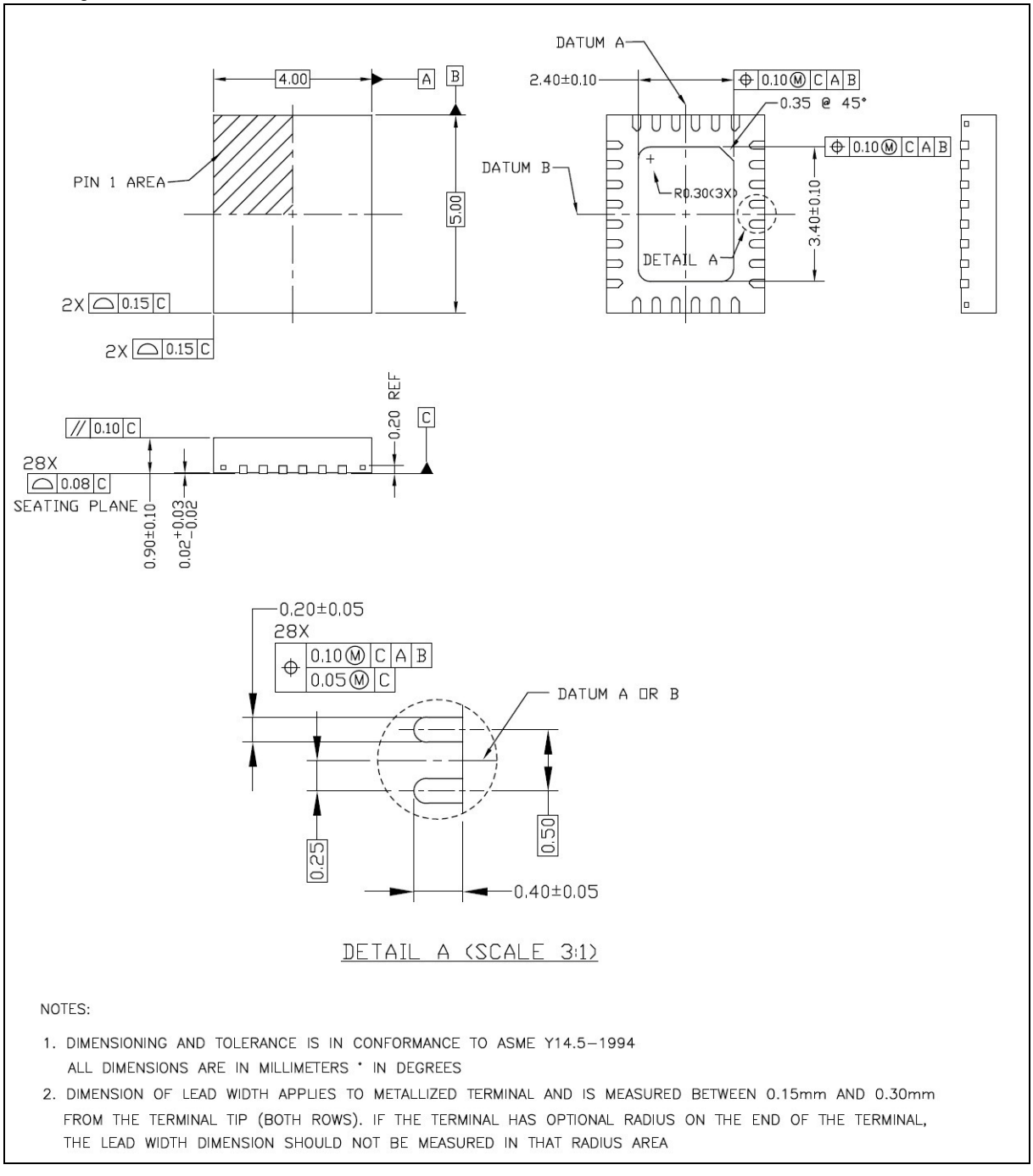
If a DC current path exists between the two outputs, a DC current can flow through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series with the output as shown in Figure 7.

Power Supplies and Component Placement

The power supply should be well bypassed with decoupling placed close to the Le87502.

Physical Dimensions

28-Pin QFN



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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