MXT57

Low Jitter, Temperature Compensated Crystal Oscillator

Features

- Output Frequency 2.5 MHz to 850 MHz
- Phase Noise as Low as 190 fs (F_0 = 156.25 MHz, Integration Bandwidth 1.875 MHz to 20 MHz)
- Ultra-Low Spurs (–100 dBc or Greater Typical)
- ±2.5 ppm over Voltage and Temperature
- Supports CMOS, LVPECL, LVDS, and HCSL Outputs
- 2.375V to 3.63V Supply Voltage
- Output Enable Option: Can be Ordered on Pin 1 or Pin 2
- Industry-Standard and Space-Saving 5.0 mm x 7.0 mm 6-Lead Package
- –40°C to +85°C Operating Temperature Range
- Pb-Free and RoHS Compliant
- Analog TCXO, No Phase Bumps during Temperature Transitions
- Short Production Lead Time

Applications

- 10/40/100G Ethernet
- SONET-Optical Communications
- PCIe Gen 3/4/5
- Fibre Channel/SAS
- CPRI/OBSAI, XAUI and Backplane SERDES

General Description

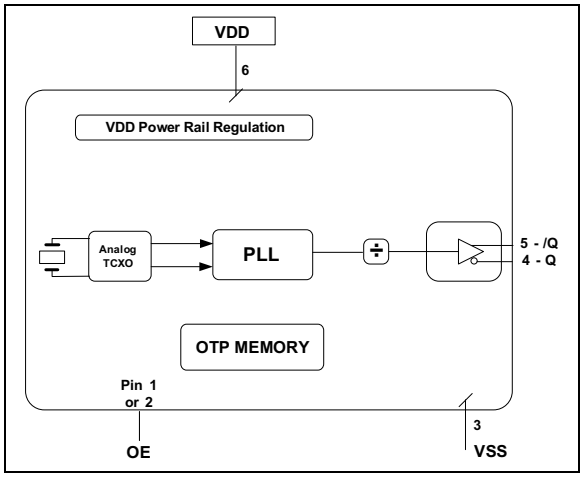
The MXT57 product line is a family of ultra-low jitter, industry standard TCXO that are designed to maximize performance in networking, storage, server, and telecommunications equipment.

The MXT57 is available in a 5 mm x 7 mm LLGA package. These devices are capable of ±2.5 ppm total stability across the –40°C to +85°C operating temperature range, using proven assembly methods that improve long term reliability and minimize aging drift compared to traditional TCXO assembly processes.

As a custom ASIC with programmable output format and OE options, these TCXOs can be configured to be footprint-compatible with any standard 6-pin TCXO available today. Standard options and frequencies are available.

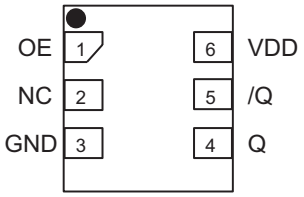
Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet, and order samples.

Functional Block Diagram

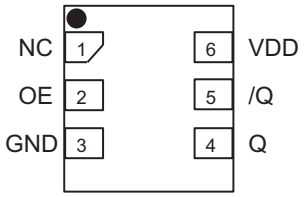


Package Types

MXT57 Pinout
Enable Pin 1 Option



MXT57 Pinout
Enable Pin 2 Option



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to + 4.0V
Input Voltage ..... –0.3V to V_{DD} +0.3V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) 400V
ESD Protection (CDM) ..... 1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 2.375V to 3.63V, T_A = –40°C to +85°C with output terminated per output logic type.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.375	—	3.63	V	—
Supply Current	I_{DD}	—	—	95	mA	Output enabled LVCMOS (no load).
		—	120	130		LVPECL
		—	90	100		LVDS
		—	95	105		HCSL
		—	60	—		Output disabled (Tri-state)
Frequency Stability	Δf	—	A = ±5	A = ±8	ppm	Inclusive of initial accuracy, temperature drift, aging, shock and vibration.
		—	B = ±2.5	B = ±5		
Start-up Time	t_{SU}	—	—	20	ms	From 90% V_{DD} to valid clock output, T = +25°C
Input Logic Levels	V_{IH}	2	—	V_{DD}+0.3	V	Input logic-high
	V_{IL}	–0.3	—	0.8		Input logic-low
Enable Active High Option (Note 2)	—	—	50	—	kΩ	Pull-up resistor on Pin 1 or 2
Enable Active Low Option (Note 3)	—	—	50	—	kΩ	Pull-down resistor on Pin 1 or 2
LVCMOS						
Frequency	f_0	2.5	—	250	MHz	—
Integrated Phase Noise (Random)	ϕj	—	450	—	fs_{RMS}	12 kHz to 20 MHz @ 156.25 MHz
		—	110	—		1.875 MHz to 5 MHz @ 156.25 MHz
Output High Voltage	V_{OH}	V_{DD} – 0.8	—	—	V	R_L = 50Ω
Output Low Voltage	V_{OL}	—	—	0.6	mV	Single-ended
Output Rise/Fall Time	t_r/t_f	100	—	500	ps	—
Duty Cycle	SYM	45	—	55	%	—
LVPECL						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	480	—	fs_{RMS}	12 kHz to 20 MHz @ 200 MHz
		—	100	—		1.875 MHz to 20 MHz @ 200 MHz

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.375V to 3.63V, T_A = –40°C to +85°C with output terminated per output logic type.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{DD}–1.35	V_{DD}–1.01	V_{DD}–0.8	V	R_L = 50Ω
Output Low Voltage	V_{OL}	V_{DD}–2.0	V_{DD}–1.78	V_{DD}–1.6	mV	Single-ended
Output Differential Voltage	V_{OD}	0.65	0.77	0.95	mV	—
Output Rise/Fall Time	t_r/t_f	85	—	350	ps	—
Duty Cycle	SYM	45	—	55	%	—
LVDS						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	430	—	fs_{RMS}	12 kHz to 20 MHz @ 200 MHz
		—	100	—		1.875 MHz to 20 MHz @ 200 MHz
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	—
Output Low Voltage	V_{OL}	0.898	1.025	1.252	mV	—
Output Differential Voltage	V_{OD}	247	350	454	mV	—
Common Mode Output Voltage	V_{CM}	1.125	1.2	1.375	mV	—
Output Rise/Fall Time	t_r/t_f	100	—	400	ps	—
Duty Cycle	SYM	45	—	55	%	—
HCSL						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	450	—	fs_{RMS}	12 kHz to 20 MHz @ 100 MHz
		—	110	—		1.875 MHz to 20 MHz @ 100 MHz
Output High Voltage	V_{OH}	660	700	850	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Output Differential Voltage	V_{OD}	—	200	250	mV	20% to 80%
		—	250	300		R_L = 50Ω
Common Mode Output Voltage	V_{CM}	48	—	52	mV	Differential
Output Rise/Fall Time	t_r/t_f	150	300	450	ps	—
Duty Cycle	SYM	48	—	52	%	—

Note 1: VDD Pin should have basic VDD filtering as shown in Figure Something.

2: Output is enabled if pad floated (not connected) or pulled high; output tri-stated if pulled low.

3: Output is enabled if pad floated (not connected) or pulled low; output tri-stated if pulled high.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+125	°C	—
Soldering Temperature	—	—	—	+260	°C	10 sec. max.
Package Thermal Resistance						
Thermal Resistance from Junction to Ambient, LGA-6Ld	θ_{JA}		—	53	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

TABLE 2-1: PIN FUNCTION TABLE (ENABLE PIN 1 OPTION)

Pin Number	Pin Name	Pin Type	Description
1	OE	I	Output Enable. Active-High and Active-Low options.
2	DNC	NC	Do not connect, leave floating.
3	GND	Ground	Power supply ground.
4	Q	O	Clock output +.
5	/Q	O	Clock output –.
6	VDD	Power	Power supply.

TABLE 2-2: PIN FUNCTION TABLE (ENABLE PIN 2 OPTION)

Pin Number	Pin Name	Pin Type	Description
1	DNC	NC	Do not connect, leave floating.
2	OE	I	Output Enable. Active-High and Active-Low options.
3	GND	Ground	Power supply ground.
4	Q	O	Clock output +.
5	/Q	O	Clock output –.
6	VDD	Power	Power supply.

3.0 PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

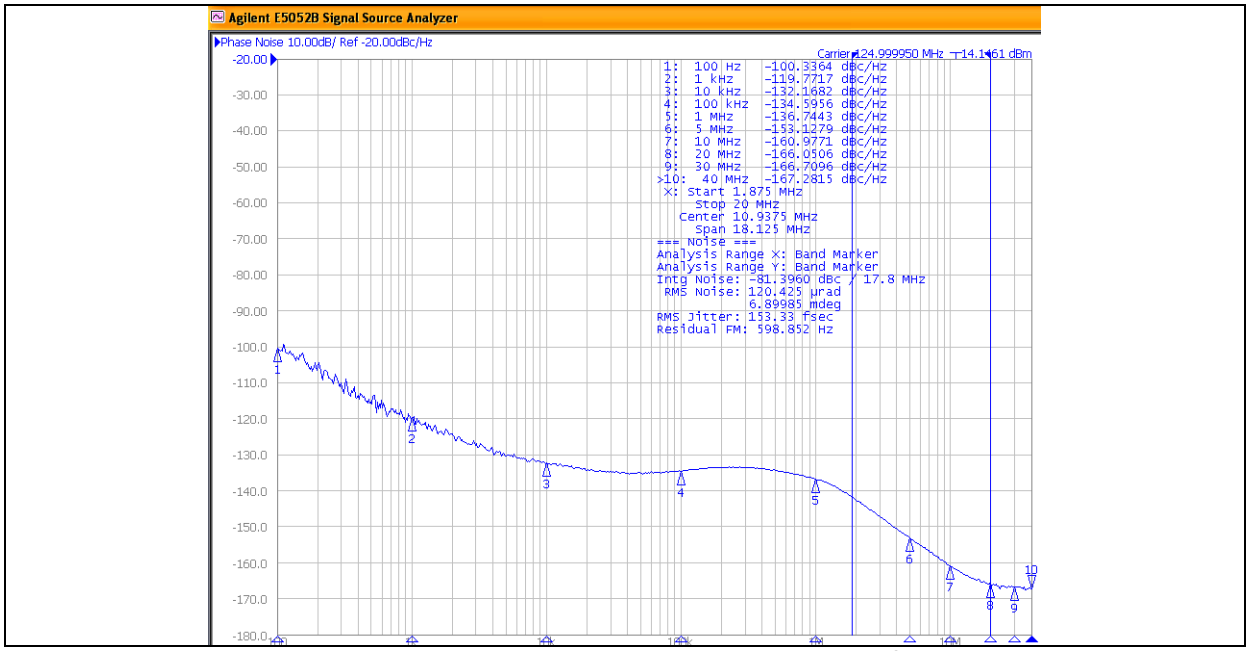


FIGURE 3-1: *LVCMOS Output 125 MHz 1.875 MHz to 20 MHz, 154 fs.*

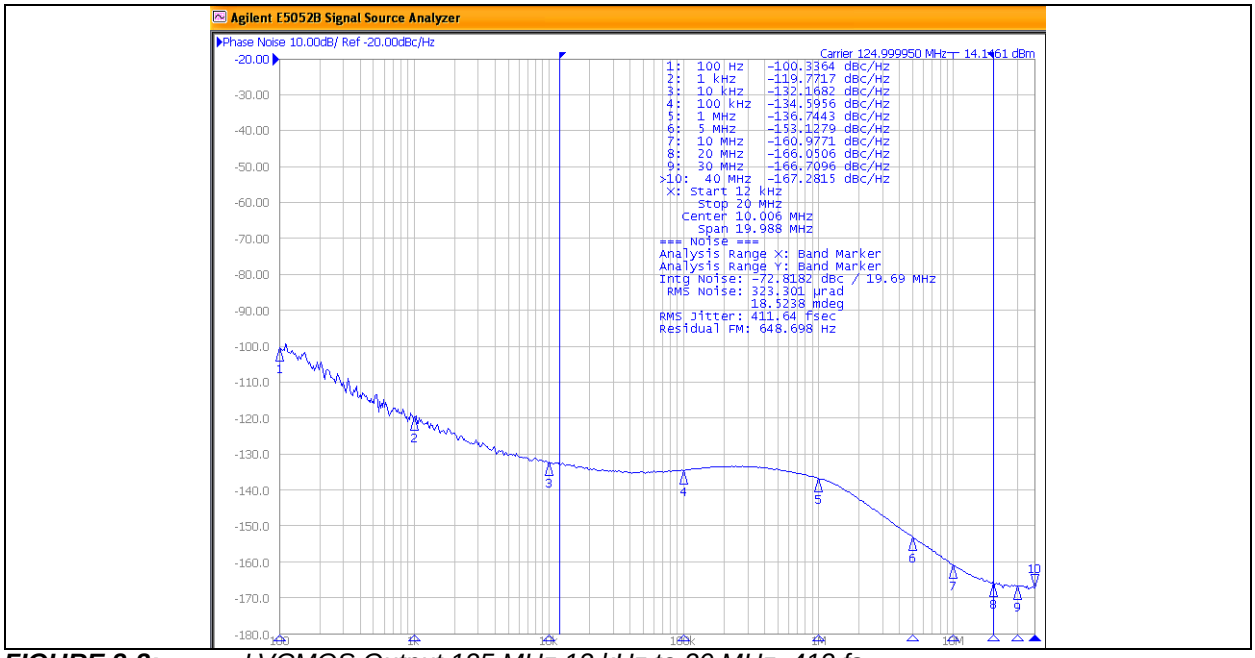


FIGURE 3-2: *LVCMOS Output 125 MHz 12 kHz to 20 MHz, 412 fs.*

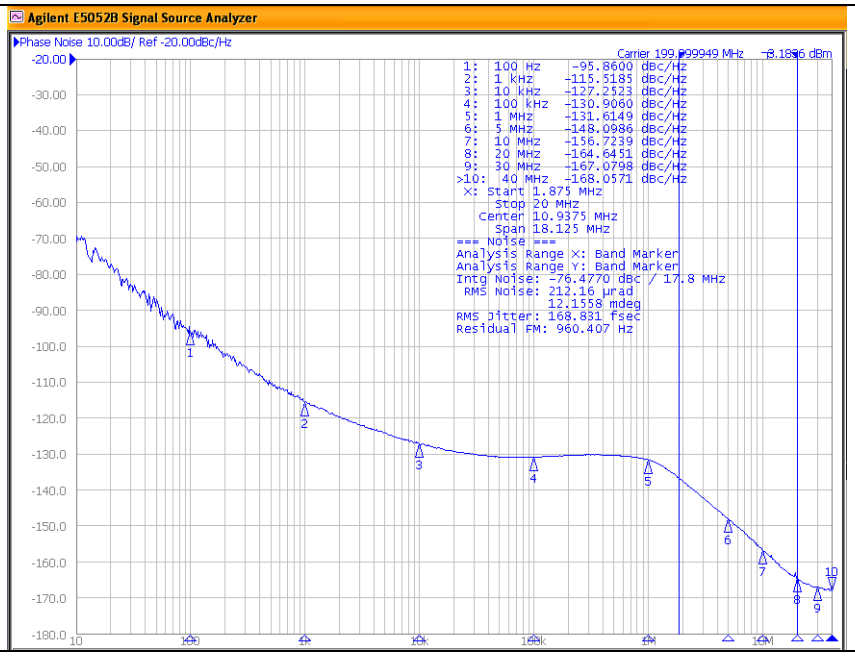


FIGURE 3-3: *LVPECL Output 200 MHz 1.875 MHz to 20 MHz 169 fs.*

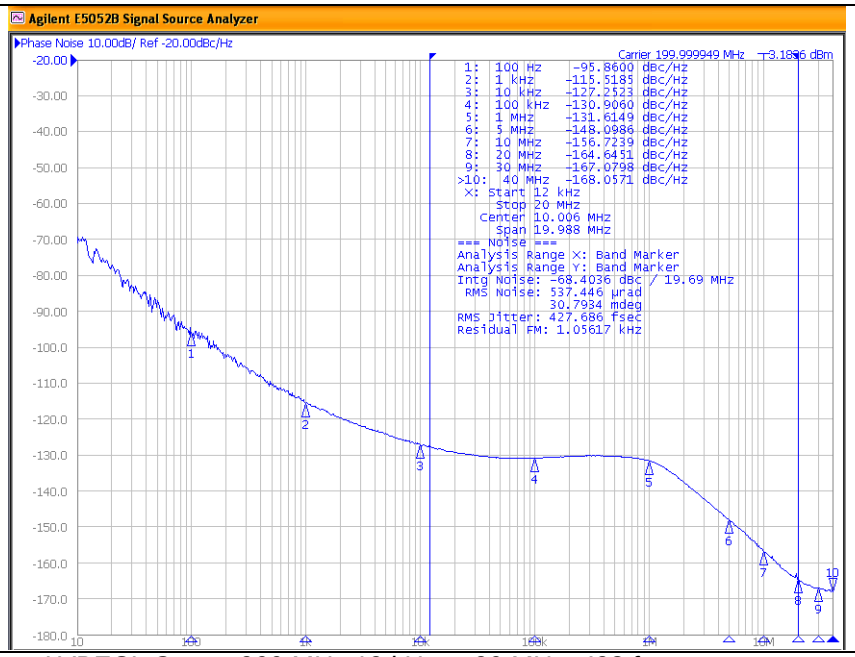


FIGURE 3-4: *LVPECL Output 200 MHz 12 kHz to 20 MHz, 428 fs.*

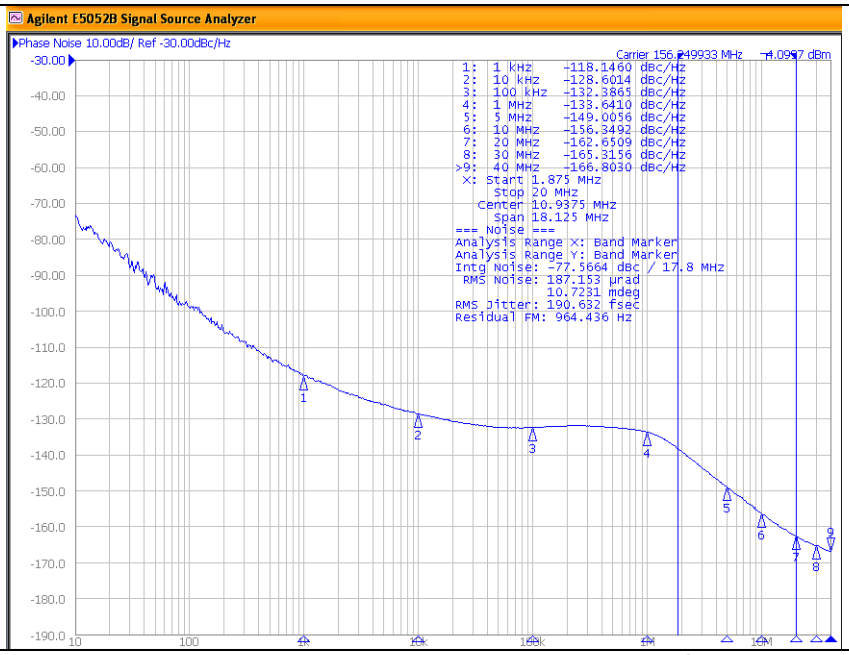


FIGURE 3-5: *HCSL Output 156.25 MHz 1.875 MHz to 20 MHz, 191 fs.*

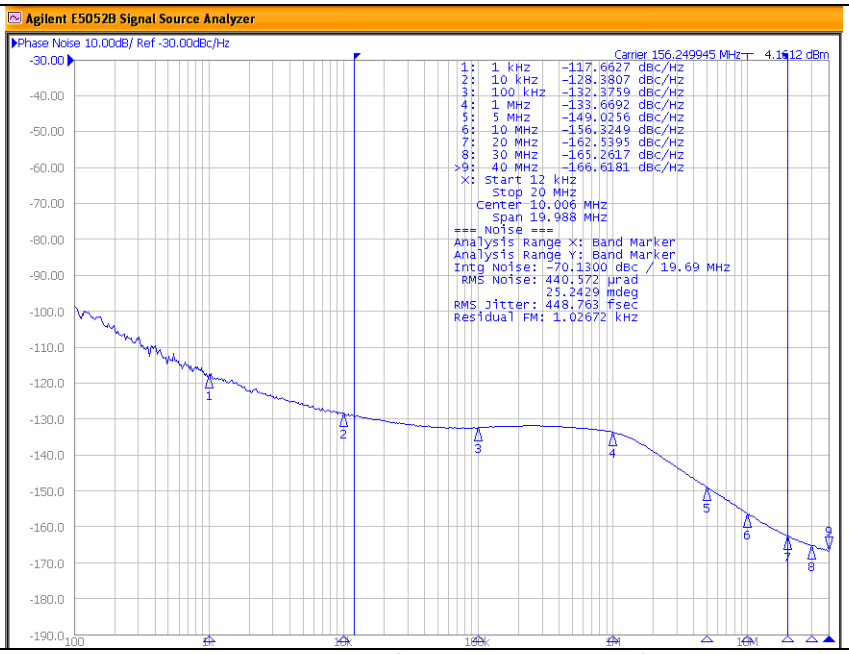


FIGURE 3-6: *HCSL Output 156.25 MHz 12 kHz to 20 MHz, 449 fs.*

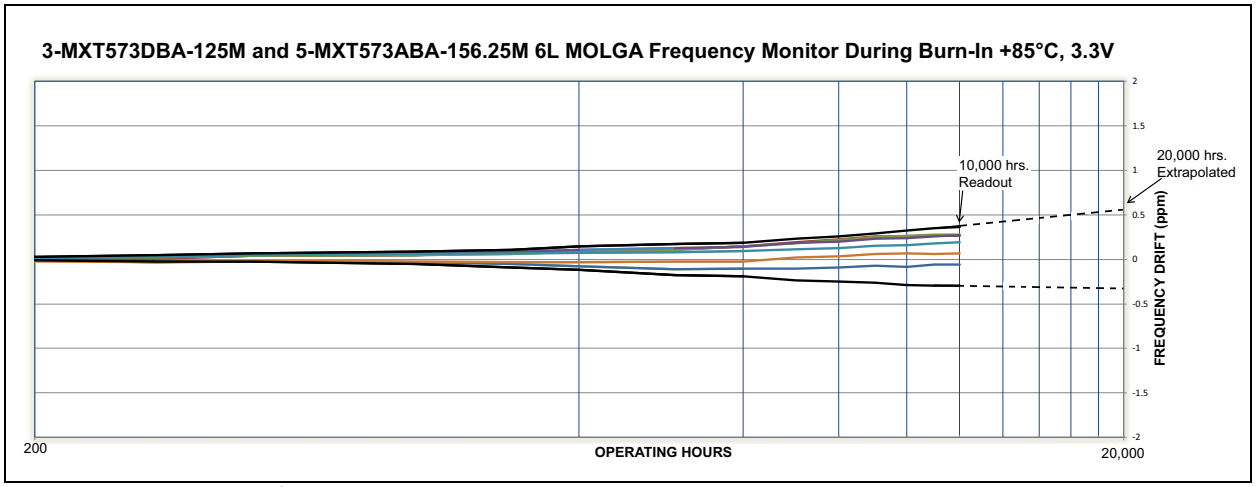


FIGURE 3-7: *Aging.*

4.0 OUTPUT WAVEFORM

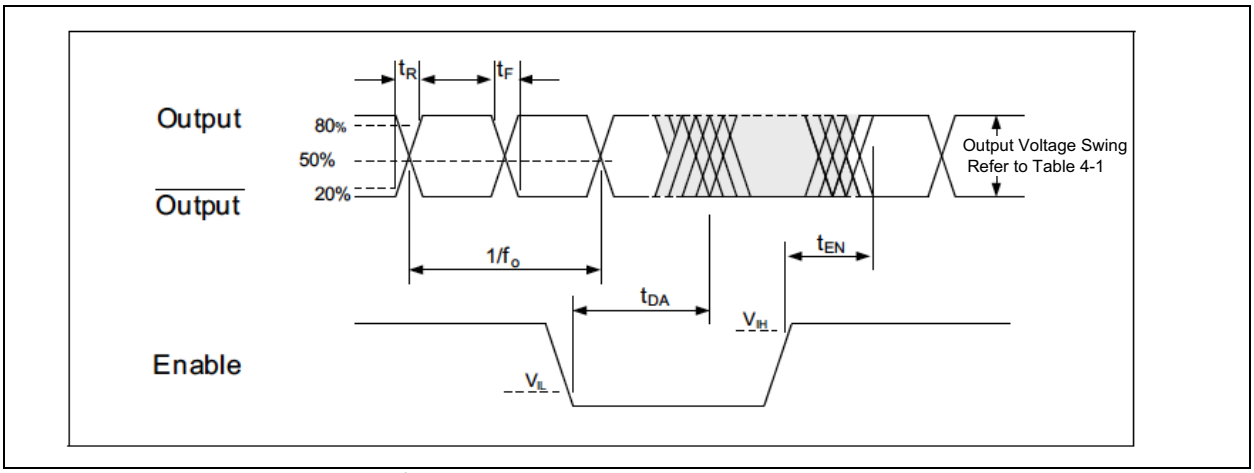


FIGURE 4-1: *Output Waveform: LVPECL, LVDS, HCSL, LVCMOS.*

TABLE 4-1: OUTPUT VOLTAGE SWING

Output Logic Protocol	Output Swing (Peak-to-Peak, Typical)
LVCMOS	V_{OH} – 3V, V_{OL} + 3V
LVPECL	770 mV
LVDS	350 mV
HCSL	700 mV

5.0 SOLDER REFLOW PROFILE

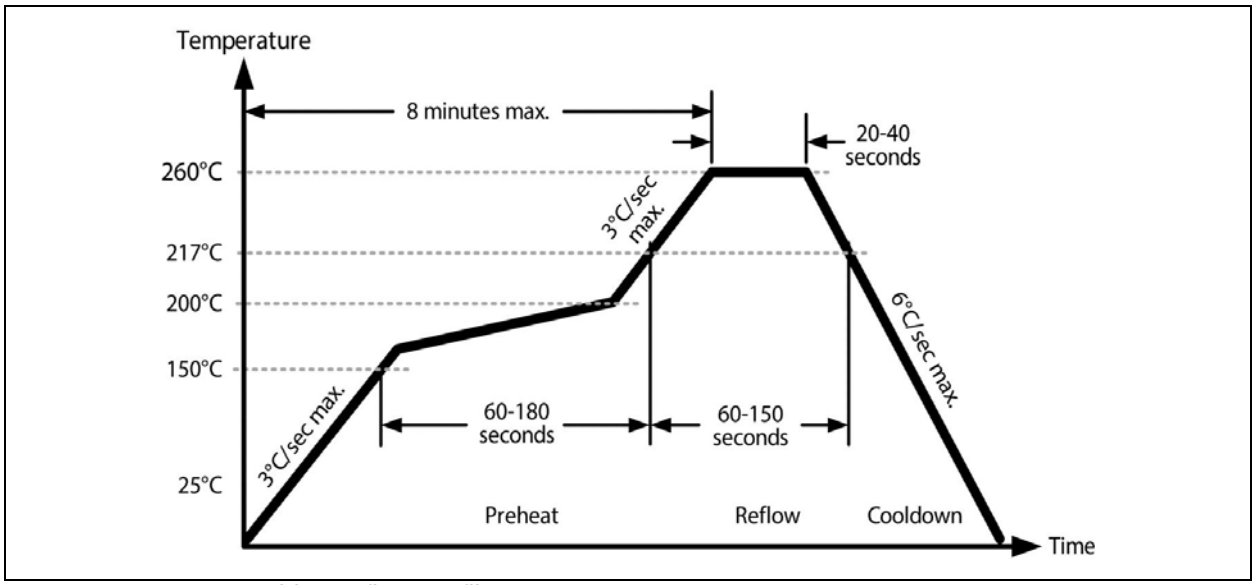


FIGURE 5-1: *Solder Reflow Profile.*

TABLE 5-1: SOLDER REFLOW

Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

6.0 ENVIRONMENTAL SPECIFICATIONS

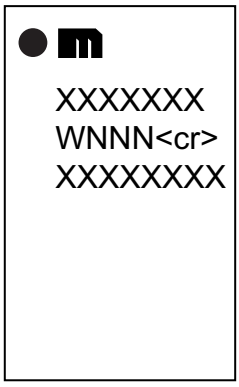
TABLE 6-1: ENVIRONMENTAL SPECIFICATIONS

Parameter	Specification
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2022, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free Devices (Except 2 Cycles Max)
Hazardous Substance	Pb-Free/RoHS/Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1 = $2x10^{-8}$ ATM CC/S
Solvent Resistance	MIL-STD-202, Method 215

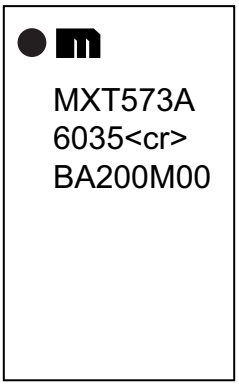
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

6-Lead LGA*



Example

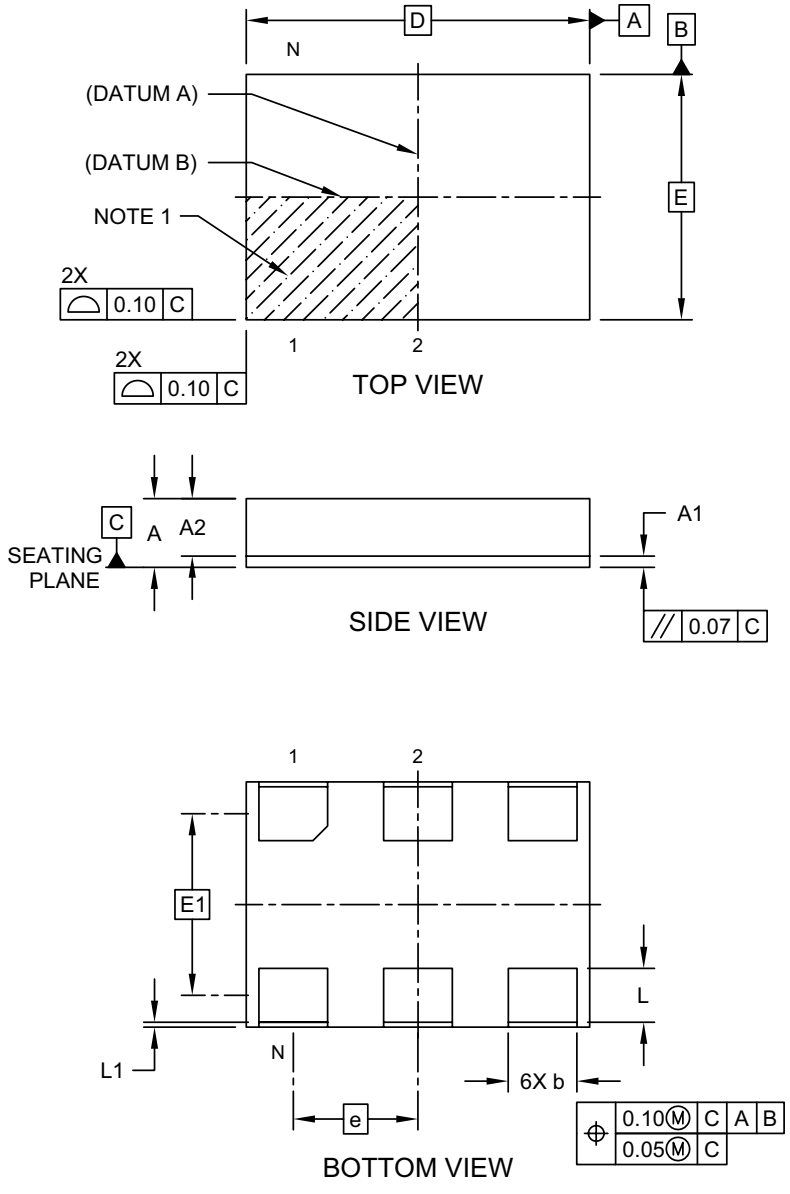


Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6-Lead 7.0 mm x 5.0 mm LLGA Package Outline and Recommended Land Pattern

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

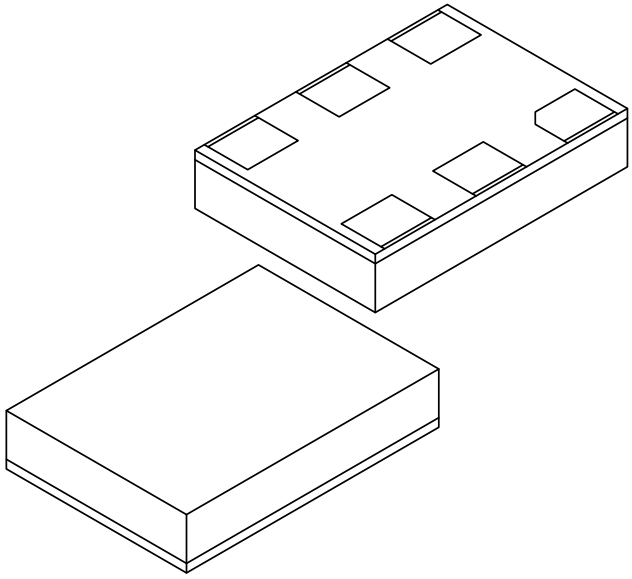
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1071A Sheet 1 of 2

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54 BSC	
Overall Height	A	1.26	1.33	1.40
Substrate Thickness	A1	0.19	0.23	0.27
Mold Cap Thickness	A2	1.07	1.10	1.13
Overall Length	D		7.00 BSC	
Pitch	E1		3.70 BSC	
Overall Width	E		5.00 BSC	
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.05	1.10	1.15
Pullback	L1	0.05	0.10	0.15

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

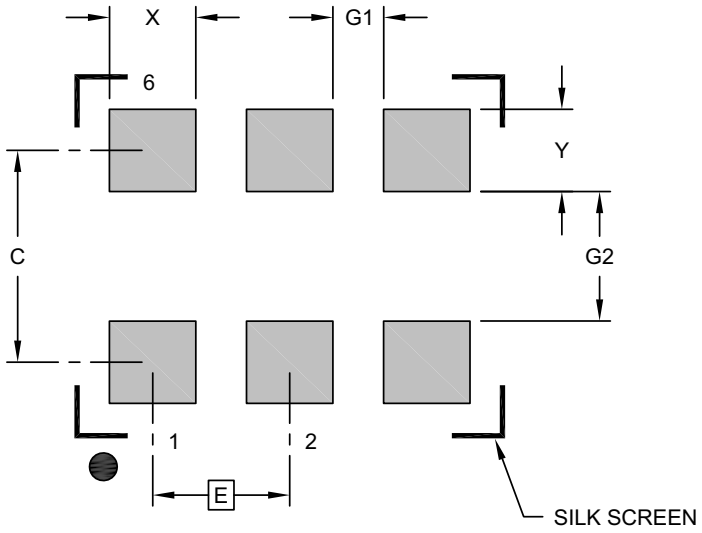
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1071A Sheet 2 of 2

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.54 BSC		
Contact Pad Spacing	C		3.93	
Contact Pad Width (X6)	X			1.60
Contact Pad Length (X6)	Y			1.53
Contact to Contact (X4)	G1	0.94		
Contact to Contact (X3)	G2	2.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3071A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2018)

- Initial creation of MXT57 Microchip data sheet DS20006037A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	X	X	XXXMXXX	XX
Device	Crystal Frequency	Enable Pin Option	Output Logic Type	Output Frequency	Shipping

Device:	MXT57:	Low Jitter, Temperature Compensated Crystal Oscillator (6-Lead 7x5 LLGA)
Crystal Frequency:	5A (Example Only) =	Selected by ClockWorks Configurator; Dependent on the ordered output frequency.
Enable Pin Option:	B = Pin 1 N = Pin 2	
Output Logic Type: (For Enable Pin 1)	A = PECL (Active-High) B = LVDS (Active-High) C = CMOS (Active-High) D = HCSL (Active-High) F = PECL (Active-Low) G = LVDS (Active-Low) H = CMOS (Active-Low) J = HCSL (Active-Low)	
Output Logic Type: (For Enable Pin 2)	R = PECL (Active-High) S = LVDS (Active-High) T = CMOS (Active-High) U = HCSL (Active-High) L = PECL (Active-Low) M = LVDS (Active-Low) N = CMOS (Active-Low) P = HCSL (Active-Low)	
Output Frequency:	xxxMxxx =	2.5 MHz to 850 MHz
Shipping:	TA = 43/Tube RA = 1,000/Reel	

Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet and order samples.

Examples:

a) MXT573ABF 100M000TA — MXT57, 3A Crystal Frequency code, OE Pin 1, PECL (Active-Low), 100 MHz, 43/Tube.

b) MXT574DBC 33M5000RA — MXT57, 4D Crystal Frequency code, OE Pin 1, CMOS (Active-High), 33.5 MHz, 1,000/Reel.

c) MXT575CNU 740M250TA — MXT57, 5C Crystal Frequency code, OE Pin 2, HCSL (Active-High), 740.25 MHz, 43/Tube,

d) MXT577FNN 3M300000RA — MXT57, 7F Crystal Frequency code, OE Pin 2, CMOS (Active-Low), 3.3 MHz, 1,000/Reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Fax: 44-118-921-5820