LE71SK7920-SW

Ve792 Software Package

Next Generation Carrier Chipset (NGCC)

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SOFTWARE PACKAGES

- **Basic Test**
  - Call Control Functions
  - Basic Test Package
  - GR909 and extensive Line Test and Self Test capabilities
- **No Test**
  - Call Control Functions

BENEFITS

- **Most cost-effective, highly-integrated, highly-featured line interface solution** for plug-and-play analog line cards in self contained architectures and worldwide applications.
- **Detailed 32 Channel RoHS compliant** reference schematics available.
- **Field upgradeable firmware.**
- **Simplified programming interface** as well as a sample quick start application to reduce development cycle and speed time to market.
- **Lenient hard real-time constraints** compared to previous products and competitive solutions.

Benefits with the Basic Test Package

- **Line testing solution** for applications requiring multi-line analog line card test functionality.
- **Self-diagnostics** simplify production & system testing for lower cost of ownership.
- **Fully validated** test routines with published accuracies.

ORDERING INFORMATION

Software Package	Description
LE71SK7920BT	Basic Test
LE71SK7920NT	No Test

DESCRIPTION

Microsemi's Ve792 Software Package is a complete software solution that simplifies control of the Microsemi Voice Termination Devices (VTDs) to provide a simplified programming interface.

The Ve792 Software Package provides a set of functions additional to the feature set of the underlying VTDs. It significantly reduces the product development cycle and time-to-market. This document describes the software packages for the Next Generation SLAC devices. Two NGSLAC devices are supported – the Le79238 Octal SLAC device and the ZL79258 Octal External Ringing SLAC device.

The Basic Test (BT) Software Package implements all supported call control features plus GR909 and extensive Line Test and Self Test capabilities.

The No Test (NT) Software Package implements all supported call control features.

Both software packages provide external ringing control for the ZL79258 SLAC device.

Five hardware topologies are supported. Detailed reference designs are available.

RELATED LITERATURE

- **133931 VoicePath™ API-II Ve792 Reference Guide**
- **135491 VoicePath™ API-II Test Library User's Guide**
- **081193 Le79238 Octal NGSLAC Data Sheet**
- **136868 ZL79258 Octal External Ringing NGSLAC Data Sheet**
- **081555 Le79271 NGSLIC Data Sheet**
- **138884 Le79272 Dual NGSLIC Data Sheet**
- **126583 NGCC Hardware Design Guide**

TABLE OF CONTENTS

MICROSEMI'S VE792 SOFTWARE PACKAGE

Key Features

Microsemi's Ve792 Software Package implements common features and functions to reduce complexity.

Key features of the Ve792 Software Package include:

- Provides an abstract, uniform software interface for any combination of Microsemi voice products.
- Provides various design tools to help in the creation and organization of parameters specific to the design and market.
- Supports any combination of FXS lines configured for either loop-start signaling or ground-start signaling.
- Exposes device functionality for pulse-digit and flash decoding, ringing cadencing and tone cadencing.
- Proven on embedded operating systems such as Linux and VxWorks, and also compatible with non-OS environments; fits into common driver and static/dynamic library models.
- Can be used with single or multi-threaded applications.
- Implemented in C code that is efficient, portable, and ANSI C compliant.
- Provides Self Test and line testing.
- Sample Quick Start Guide and Quick Start Application software provided with source code to facilitate startup and troubleshooting.
- Includes comprehensive documentation, an excellent starting point to help the developer quickly become familiar with the architecture.

The Ve792 Software Package includes the following items.

VoicePath™ API-II

Microsemi's VoicePath™ Application Programmer Interface (VP-API-II) is a C source code module that provides a standard software interface for implementing call control and line testing functions for a set of subscriber lines using Microsemi VTDs. The VP-API-II abstracts and simplifies the details of controlling the Microsemi VTDs and allows software developers to focus on the application instead of the underlying hardware.

The API-II functions can be summarized into the following four groups:

- **Initialization functions:** These functions perform the configuration required before a particular feature may be used. Example of initialization functions include:
  - Configure all lines with specified design parameters.
  - Calibrate all analog circuits of termination devices.
- **Query Functions:** The query functions provide several methods for servicing and checking the status of the lines. These functions allow the user to read option settings or line conditions, and to retrieve event contents or test results. Examples of query functions include:
  - On/Off hook, read loop conditions for a specific line.
  - Global device status for up to 32 lines.
  - Read various VoicePath™ API-II device options and test results.
- **Control Functions:** These functions control the current line state and options that may change during run-time. Examples of control functions include:
  - Set a line to a desired state.
  - Place a cadenced DTMF call progress tone on the line.
  - Start metering on a particular line.
  - Set various VoicePath™ API-II device specific options.
- **Test Functions:** The test functions provide a toolbox of line tests and diagnostic utilities. Example of test functions include:
  - Perform Self Test on a particular line or the entire system.
  - Test primitives to support GR909 line tests on any given channel.

VoicePath™ Test Library

The VoicePath™ Test Library (VP-TL) is a collection of functions and data types that further utilize the line testing capabilities of Microsemi's VP-API-II. These algorithms are executed on the host processor interfaced to Microsemi's NGCC devices through the VoicePath™ API-II.

The VP-TL offers the following key features:

- Performs a complete high-level test by running several VP-API-II test primitives in sequence.
- Provides optimal default values for test input parameters that do not typically change at run-time, such as integration times, settling times, etc.
- Converts fixed-point results returned by the VP-API-II test primitives into standard units that the application can readily use.
- Includes line self-testing to check for possible problems before putting a line into service.

Design Toolset

Microsemi products can be configured to meet standards worldwide, including custom requirements. To address such varying system-level specifications, Microsemi provides tools like WinSLAC™ and Profile Wizard to help engineers generate design data. The design data provided by these tools is organized into profiles to meet specific system requirements. The data for each profile is created with the Profile Wizard application. Profiles can be generated for the following design parameters:

- **System Profile** - The System Profile is a data array that contains set-and-forget parameters for the event mask, clocks, etc., and for other global configuration options.
- **AC Profile** - The AC Profile is a transmission characteristic profile. The AC profile holds the SLAC device's gain block and filter block commands and data. Each AC Profile is designed to address the specific AC transmission requirements for a given design. In general, AC Profiles are used to address the varying requirements of different market segments.
- **DC Profile** - The DC Profile holds the SLAC device's DC feed and Loop Supervision command and data. Each DC profile is designed to address the specific DC feed and Loop Supervision requirements of a given design. Examples of different DC feed profiles include a Constant Current Profile and a Resistive Feed Profile.
- **Ringing Profile** - The Ringing Profile contains the necessary commands and data to set up the ringing generator of a SLAC device. Different Profiles can be used to vary the ringing characteristics of a line. Options available in the Ringing Profile include: ringing waveform, frequency, amplitude, DC offset, and ring trip detector mode.
- **Metering Profile** - The Metering Configuration Profile contains the necessary commands and data to set up the Pulse Meter Signal Generator of the SLAC device. The parameters configured include voltage limits.
- **Tone Profile** - The Tone Profile defines the various call progress tones that might be used in a system. The tones include dial tone, busy, ring-back, and reorder. The Tone Profiles are used to address the market variations that exist around the world.
- **Tone Cadence Profile** - The Tone Cadence Profile defines the various cadences that might be used in a system for call progress tones. The Tone Cadence Profiles are used to address market variations.
- **Ring Cadence Profile** - The Ring Cadence Profile defines the various cadences that might be used in a system for ringing. The Ring Cadence Profiles are used to address market variations.
- **Caller ID** - Defines the various Caller Line Identity (CLI) types that might be used in a system. The Caller ID Profiles are used to address the market variations that exist around the world.

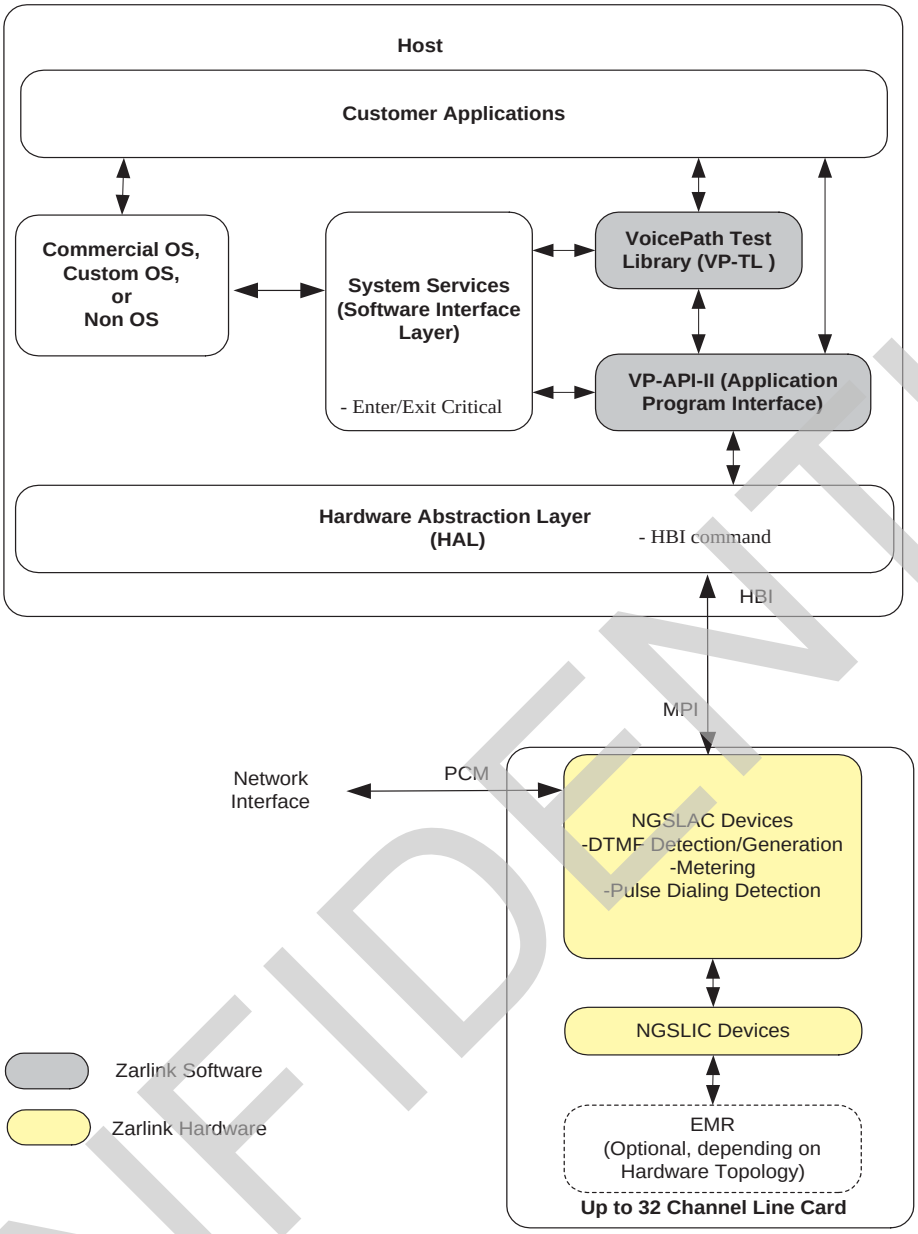
Once the profiles have been created, they can be compiled into the user's application and passed into the VoicePath™ API-II. The application keeps the profiles on the host and downloads them on demand.

The VoicePath™ Profile Wizard and WinSLAC are Microsoft® Windows® based applications that are part of the NGCC Design Kit and are used to create the various profiles needed to fulfill the specific market requirements.

SYSTEM ARCHITECTURE

Figure 1 illustrates a typical system block diagram incorporating the software block diagram and a detailed block diagram of the underlying hardware. The VoicePath™ software requires the System Services Layer and Hardware Abstraction Layer to operate correctly. The following sections describe each of the blocks.

Figure 1. NGCC System Architecture



Software Architecture

Customer Application

This block represents the user's *line management* module that performs tasks such as initializing the system, configuring lines, changing line states in response to line events and other inputs, switching digitized voice traffic, line testing etc. These functions may be distributed across a complex system. Microsemi provides example applications as part of the Ve792 Software Package.

Operating System

This block represents whatever operating system (if any) the user is running on the host processor. The VP-API-II does not directly utilize any operating system resources (e.g. queues, semaphores, etc.). The application developer may use operating system features such as tasks or shared memory with the VP-API-II. Chapter 3 in the *API Reference Guide* covers using the VP-API-II in a multitasking environment in detail.

System Services Layer

The System Services Layer abstracts platform-specific functions such as test relay control and other customer specific functions. This layer derives the functions required by the VP-API-II from the facilities provided by the underlying hardware or operating system. This module is also platform-dependent and must be implemented by the VP-API-II user. Microsemi provides example System Services Layer source code.

VoicePath™ Test Library

The VoicePath™ Test Library (VP-TL) algorithms are executed on the host processor using the VoicePath™ API-II.

VoicePath™ API-II

The VP-API-II is the core component of the Ve792 Software Package. This software module runs on the host processor that controls Microsemi VTDs. This code is supplied by Microsemi and should not be modified by the application developer.

Hardware Abstraction Layer

The Hardware Abstraction Layer (HAL) provides access to Microsemi devices through the Host Bus Interface (HBI). The HAL software is platform-dependent and must be implemented by the VP-API-II user. Microsemi provides example HAL source code with the Ve792 Software Package.

Host Bus Interface

The Host Bus Interface (HBI) provides a means for the host to communicate with the SLAC. The HBI includes the Application, Transport, and Physical Layers of the SLAC device's host interface.

The physical layer defines the electrical characteristics of the interface (pins, timings, etc.) between the host and the SLAC. The SLAC supports a Microprocessor Peripheral Interface (MPI) physical layer.

This layered architecture allows the host programmer to program the SLAC independently of the configuration of the physical layer (8-bit vs. 16-bit, byte-framing vs. command-framing).

Hardware Architecture

The hardware consists of the Le79238 or ZL79258 NGSLAC and the Le79271 NGSLIC Voice Termination Devices.

The host can choose to poll the SLAC device(s) or service them by waiting for an interrupt to indicate that servicing is needed. To support (up to) four SLAC devices (32 channels), four chip select and four interrupt lines are required from the host.

Using VoicePath API-II functions, the channels from multiple SLACs can be assigned a contiguous set of logical line numbers as shown in Table 1. At system initialization, a software line object needs to be created for each individual line, indicating the SLAC, channel, and line termination type for that line. This is done with the VpMakeLineObject() function, which also creates a line context pointer for this line object. A unique logical line ID can then be assigned to each line, as shown in the table, using the VpMapLineId() function. After system initialization is complete, all VP-API-II functions use the line context pointer and/or the line ID as a channel identifier, such that the host application code needs not be concerned with the physical SLAC channel mapping.

Table 1. Channel ID

Logical Line ID	Physical SLAC Channel ID	SLAC	Chip Select	Interrupt
0 to 7	0 to 7	0	CS0	INT0
8 to 15	0 to 7	1	CS1	INT1
16 to 23	0 to 7	2	CS2	INT2
24 to 31	0 to 7	3	CS3	INT3

Hardware Topologies

Microsemi specifies standard line circuit configurations ("hardware topologies") that determine the capabilities and behavior of VoicePath™ Test Library software. The configuration determines which "line termination type" must be assigned to each line in the system at initialization with the VpMakeLineObject() function. Table 2 lists the supported hardware topologies and corresponding line termination types.

Table 2. VoicePath™ Test Library Supported Termination Types

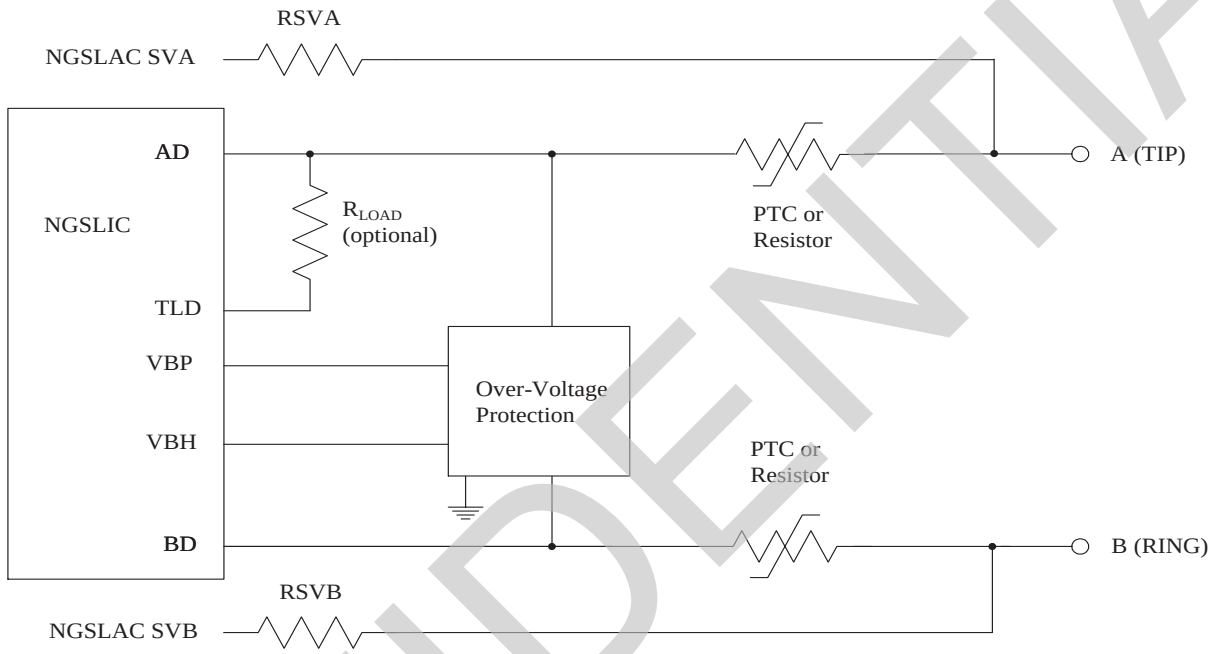
Hardware Topologies	Software Termination Types	Description
Configuration C	VP_TERM_FXS_GENERIC	Generic FXS termination
Configuration D	VP_TERM_FXS_TI	FXS termination with Test-In relay
Configuration E	VP_TERM_FXS_RR	FXS termination with Ringing relay
Configuration E	VP_TERM_FXS_RR_MW	FXS termination with Ringing and Message Waiting relays
Configuration F	VP_TERM_FXS_RR_TI	FXS termination with Ringing and Test-In relays

Configuration C Topology (VP_TERM_FXS_GENERIC)

Features:

- POTS service.
- Foreign voltages in excess of the SLIC power rail voltages can be measured when the PTCs are activated or if the fault current doesn't exceed the SLIC current drive capability.
- The test load resistor is used for self-testing.
- No disconnect relay. There is no means to disconnect the line from the loop during Self Test. The published Self Test accuracies are given for production testing only, when no loop is connected to the equipment port. If Self Tests are performed in the field, the host application needs to take into account any loop impedance present.

Figure 2. Configuration C Topology



This configuration supports the relay states listed in Table 3. See the *VoicePath™ API-II Reference Guide* for details of the VpSetRelayState() function. Connectivity for the various relay states is depicted in Table 4.

Table 3. Software States for Configuration C

Software State (VpRelayState)	Description
VP_RELAY_NORMAL	Test load switch off
VP_RELAY_TALK	Test load switch off
VP_RELAY_BRIDGED_TEST	Test load switch on

Table 4. Configuration C Bus Connections

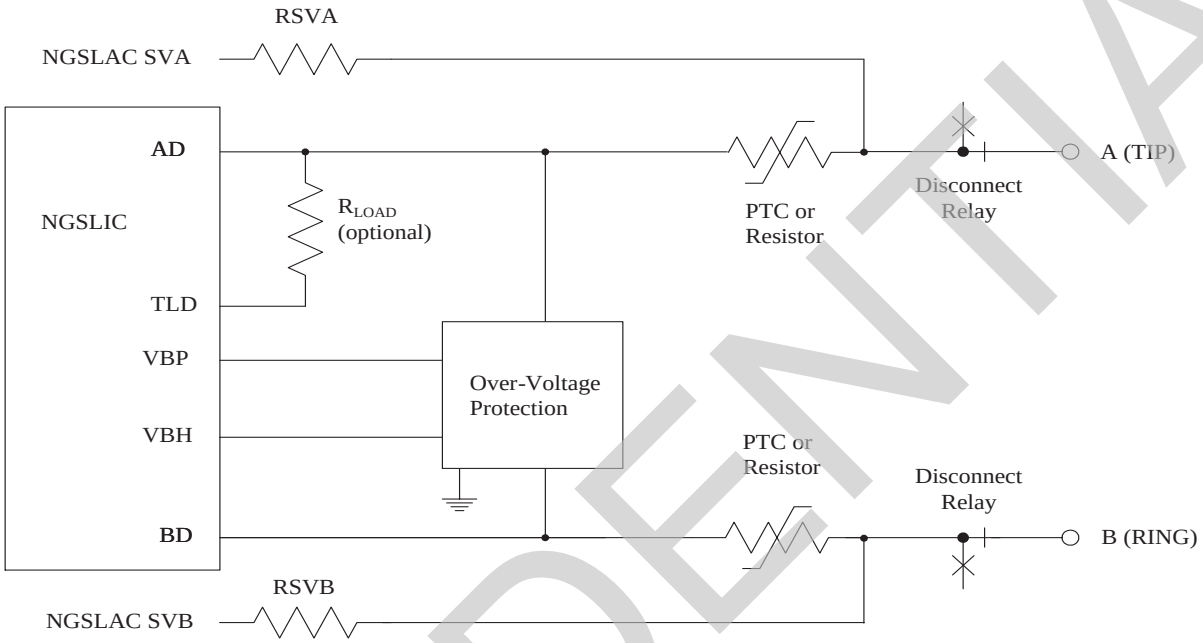
Software State	AD/BD	SVA/SVB	Rload	TIP/RING
VP_RELAY_NORMAL	●	●		●
VP_RELAY_TALK	●	●		●
VP_RELAY_BRIDGED_TEST	●	●	●	●

Configuration D Topology (VP_TERM_FXS_TI)

Features:

- POTS service with a disconnect relay.
- Foreign voltages in excess of the SLIC power rail voltages can be measured when the PTCs are activated or if the fault current doesn't exceed the SLIC current drive capability.
- The relay is used to disconnect the loop during self-testing.
- Self Test is performed using the per-channel test load resistor.

Figure 3. Configuration D Topology



This configuration supports the relay states listed in Table 5. See the *VoicePath™ API-II Reference Guide* for details of the VpSetRelayState() function.

Connectivity for the various relay states is depicted in Table 6.

Table 5. Software States for Configuration D

Software State (VpRelayState)	Description
VP_RELAY_NORMAL	Test load switch off
VP_RELAY_TALK	Test load switch off
VP_RELAY_TEST	Test load switch off, Disconnect relay activated
VP_RELAY_DISCONNECT	Test load switch off, Disconnect relay activated
VP_RELAY_BRIDGED_TEST	Test load switch on
VP_RELAY_SPLIT_TEST	Test load switch on, Disconnect relay activated

Table 6. Configuration D Bus Connections

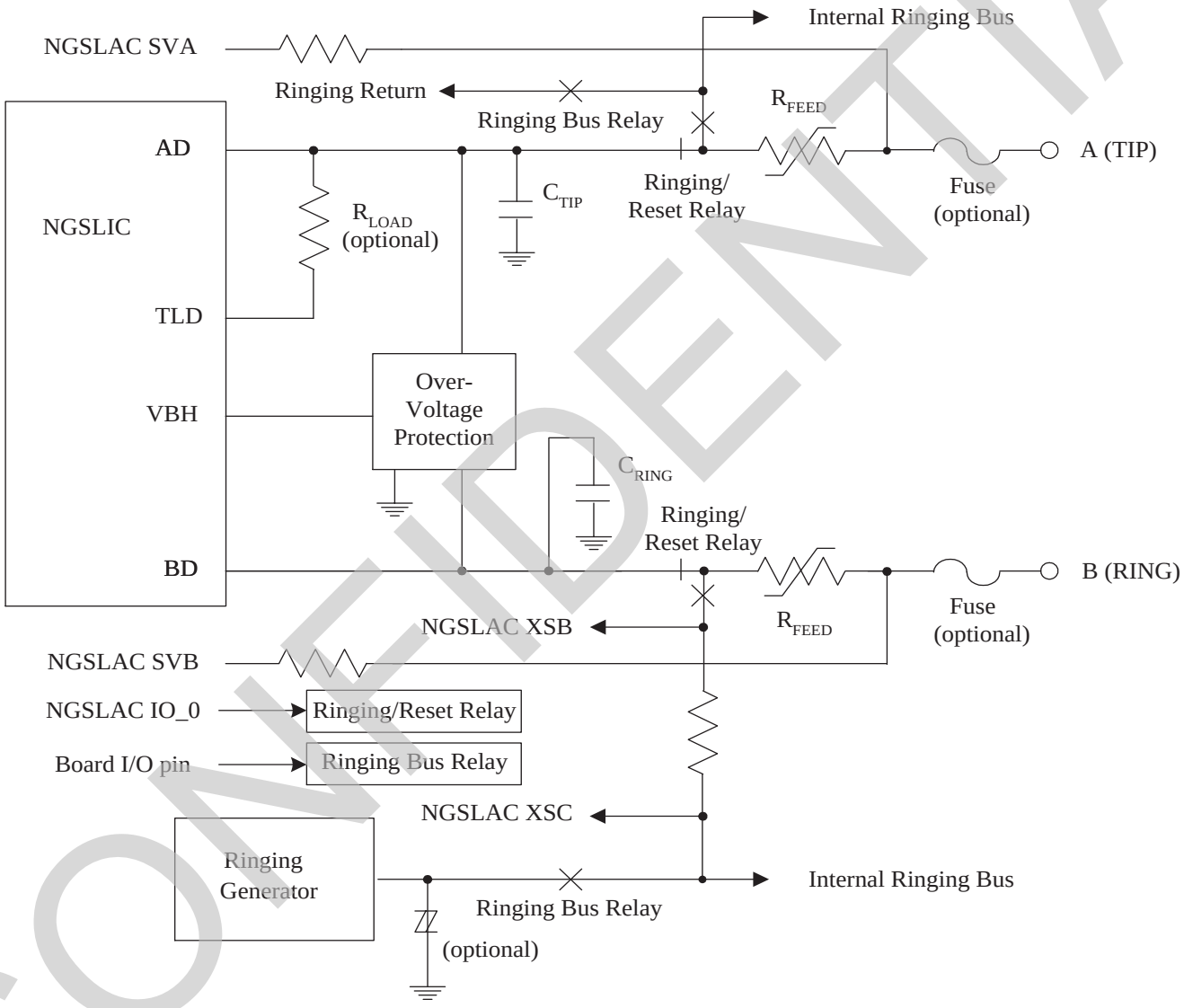
Software State	AD/BD	SVA/SVB	Rload	TIP/RING
VP_RELAY_NORMAL	●	●		●
VP_RELAY_TALK	●	●		●
VP_RELAY_TEST	●	●		
VP_RELAY_DISCONNECT	●	●		
VP_RELAY_BRIDGED_TEST	●	●	●	●
VP_RELAY_SPLIT_TEST	●	●	●	

Configuration E Topology (VP_TERM_FXS_RR)

Features:

- POTS service with external ringing.
- Foreign voltages in excess of the SLIC power rail voltages can be measured when the PTCs are activated, if the fault current doesn't exceed the SLIC current drive capability, or by operating the ringing relay to disconnect the SLIC drivers from the external port. The last option is only available if the ringing bus can be made high impedance during the foreign voltage test.
- The test load resistor is used for self-testing.
- No disconnect relay. There is no means to disconnect the line from the loop during Self Test. The published Self Test accuracies are given for production testing only, when no loop is connected to the equipment port. If Self Tests are performed in the field, the host application needs to take into account any loop impedance present.

Figure 4. Configuration E Topology



This configuration supports the relay states listed in Table 7. See the *VoicePath™ API-II Reference Guide* for details of the VpSetRelayState() function.

Connectivity for the various relay states is depicted in Table 8.

Table 7. Software States for Configuration E

Software State (VpRelayState)	Description
VP_RELAY_NORMAL	Ringing relay on or off based on line state, test load released
VP_RELAY_TALK	Ringing/Reset relay released, test load released
VP_RELAY_RINGING	Ringing relay active, test load released
VP_RELAY_BRIDGED_TEST	Ringing/Reset relay released, test load active
VP_RELAY_RESET[1]	Ringing relay active, test load released, ringing bus relay active
1. Note: The application developer must implement the VpIlSysCaptureRingingBus() and the VpIlSysReleaseRingingBus() functions in order to use the VP_RELAY_RESET state. The ringing bus relay is controlled by those two functions, not by the VpSetRelayState() function. Refer to the VoicePath™ API-II Test Library User's Guide for more details.	

Table 8. Configuration E Bus Connections

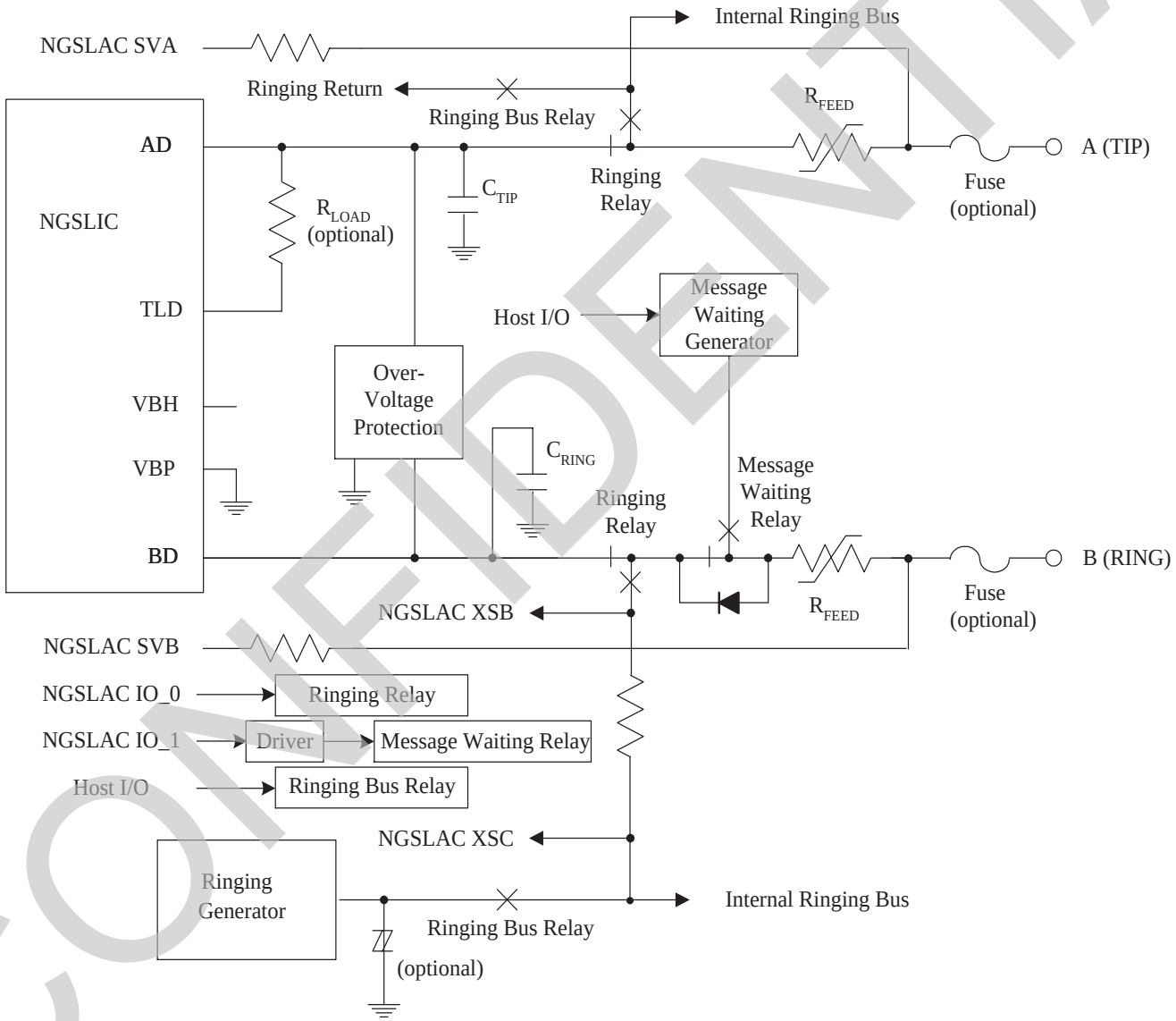
Software State	AD/BD	SVA/SVB	R_{load}	Ringing	TIP/RING
VP_RELAY_NORMAL[1]	●	●			●
VP_RELAY_NORMAL[2]		●		●	●
VP_RELAY_TALK	●	●			●
VP_RELAY_RINGING		●		●	●
VP_RELAY_BRIDGED_TEST	●	●	●		●
VP_RELAY_RESET		●			●
1. Non-ringing line state. 2. Ringing line state.					

Configuration E Topology (VP_TERM_FXS_RR_MW)

Features:

- POTS service with external ringing and Message Waiting signalling.
- Foreign voltages in excess of the SLIC power rail voltages can be measured when the PTCs are activated, if the fault current doesn't exceed the SLIC current drive capability, or by operating the ringing relay to disconnect the SLIC drivers from the external port. The last option is only available if the ringing bus can be made high impedance during the foreign voltage test.
- The test load resistor is used for self-testing.
- This configuration does not use a VBP supply, therefore some test restrictions apply.
- No disconnect relay. There is no means to disconnect the line from the loop during inward looking test, therefore Self Test can only be performed in the factory. The published Self Test accuracies are given for production testing only, when no loop is connected to the equipment port. If Self Tests are performed in the field, the host application needs to take into account any loop impedance present.

Figure 5. Configuration E Topology



This configuration supports the relay states listed in Table 9. See the *VoicePath™ API-II Reference Guide* for details of the VpSetRelayState() function.

Connectivity for the various relay states is depicted in Table 10.

Table 9. Software States for Configuration E

Software State (VpRelayState)	Description
VP_RELAY_NORMAL	Ringing relay on or off based on line state, test load released, message waiting relay off
VP_RELAY_TALK	Ringing relay off, test load released, message waiting relay off
VP_RELAY_RINGING	Ringing relay active, test load released, message waiting relay off
VP_RELAY_BRIDGED_TEST	Ringing relay off, test load active, message waiting relay off
VP_RELAY_LAMP_ON	Ringing relay off, test load released, message waiting relay on
VP_RELAY_RESET[1]	Ringing relay active, test load released, message waiting relay off, ringing bus relay active
1. Note: The application developer must implement the VpttlSysCaptureRingingBus() and the VpttlSysReleaseRingingBus() functions in order to use the VP_RELAY_RESET state. The ringing bus relay is controlled by those two functions, not by the VpSetRelayState() function. Refer to the VoicePath™ API-II Test Library User's Guide for more details.	

Table 10. Configuration E Bus Connections

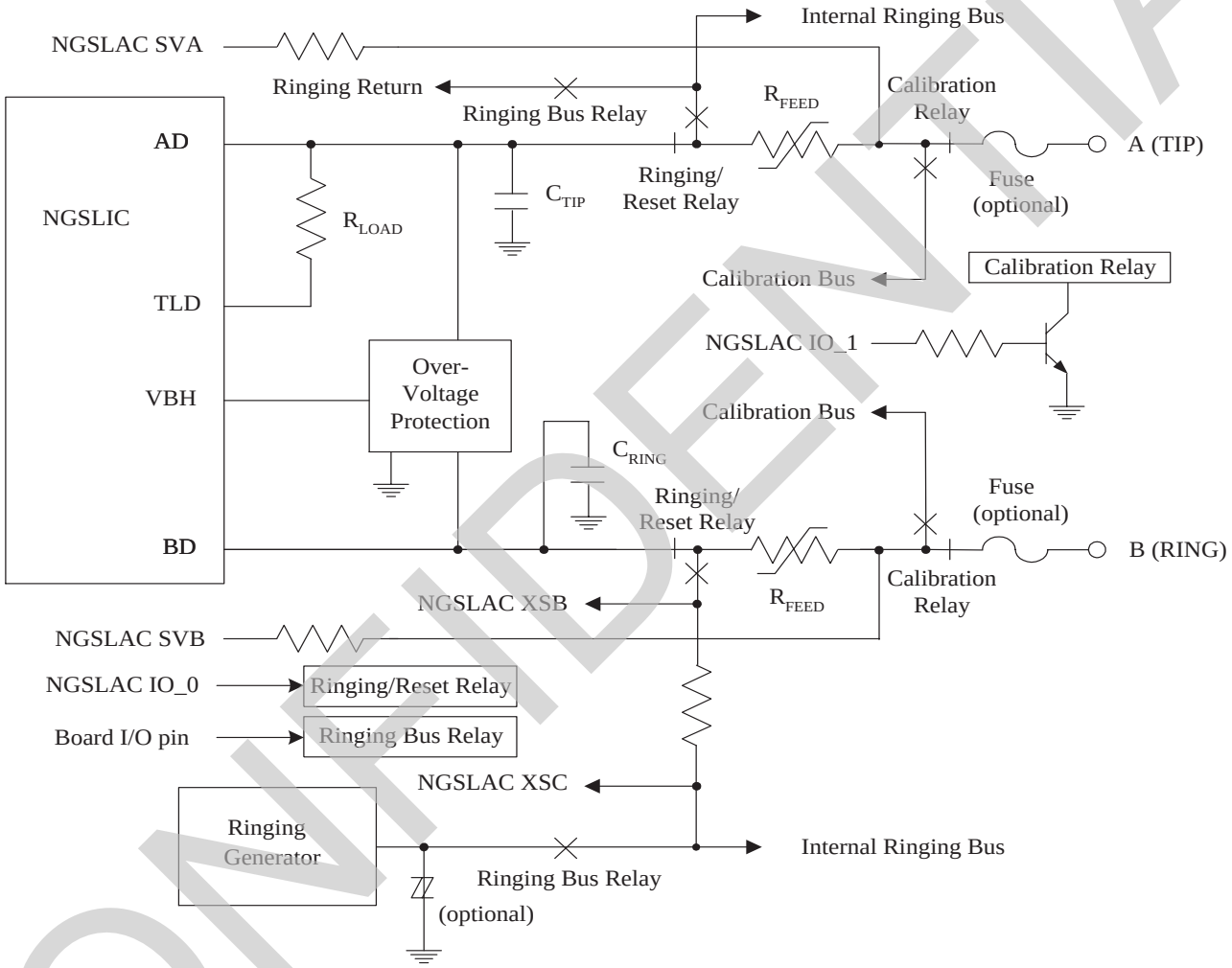
Software State	AD/BD	SVA/SVB	R_{load}	Ringing	TIP/RING	Message Waiting
VP_RELAY_NORMAL[1]	●	●			●	
VP_RELAY_NORMAL[2]		●		●	●	
VP_RELAY_TALK	●	●			●	
VP_RELAY_RINGING		●		●	●	
VP_RELAY_BRIDGED_TEST	●	●	●		●	
VP_RELAY_LAMP_ON[3]		●			●	●
VP_RELAY_RESET		●			●	
1. Non-ringing line state. 2. Ringing line state. 3. Line feed reverts to AD/BD via a diode in case of an off-hook, because the message waiting generator goes into current limit.						

Configuration F Topology (VP_TERM_FXS_RR_TI)

Features:

- POTS service with external ringing and a relay to connect to a Test-In bus for self-testing.
- Foreign voltages in excess of the SLIC power rail voltages can be measured when the PTCs are activated, if the fault current doesn't exceed the SLIC current drive capability, or by operating the ringing relay to disconnect the SLIC drivers from the external port. The last option is only available if the ringing bus can be made high impedance during the foreign voltage test.
- The Test-In Relay is used to disconnect the loop during self-testing.
- Self Test is performed using the per-channel test load resistor or a shared load connected to the Test-In bus.
- This configuration does not use a VBP supply, therefore some test restrictions apply.

Figure 6. Configuration F Topology



This configuration supports the relay states listed in Table 11. See the *VoicePath™ API-II Reference Guide* for details of the VpSetRelayState() function.

Connectivity for the various relay states is depicted in Table 12.

Table 11. Software States for Configuration F

Software State (VpRelayState)	Description
VP_RELAY_NORMAL	Ringing relay on or off based on line state, test load released
VP_RELAY_TALK	Ringing/Reset relay released, test load released
VP_RELAY_RINGING	Ringing relay active, test load released
VP_RELAY_BRIDGED_TEST	Ringing/Reset relay released, test load active
VP_RELAY_RESET[1]	Reset relay active, test load released, ringing bus relay active
VP_RELAY_TEST	Ringing/Reset relay released, test load released, Test-In relay activated
VP_RELAY_DISCONNECT	Ringing/Reset relay released, test load released, Test-In relay activated
VP_RELAY_SPLIT_TEST	Ringing/Reset relay released, test load active, Test-In relay activated
VP_RELAY_RINGING_TEST	Ringing/Reset relay active, test load released, Test-In relay activated
1. Note: The application developer must implement the VptlSysCaptureRingingBus() and the VptlSysReleaseRingingBus() functions in order to use the VP_RELAY_RESET state. The ringing bus relay is controlled by those two functions, not by the VpSetRelayState() function. Refer to the VoicePath™ API-II Test Library User's Guide for more details.	

Table 12. Configuration F Bus Connections

Software State	AD/BD	SVA/SVB	Rload	Ringing	Test-In Bus	TIP/RING
VP_RELAY_NORMAL[1]	●	●				●
VP_RELAY_NORMAL[2]		●		●		●
VP_RELAY_TALK	●	●				●
VP_RELAY_RINGING		●		●		●
VP_RELAY_BRIDGED_TEST	●	●	●			●
VP_RELAY_RESET		●				●
VP_RELAY_TEST	●	●			●	
VP_RELAY_DISCONNECT	●	●			●	
VP_RELAY_SPLIT_TEST	●	●	●		●	
VP_RELAY_RINGING_TEST		●		●	●	
1. Non-ringing line state. 2. Ringing line state.						

LINE TESTING

Device Level Test Restrictions

Line test restrictions at the device level are:

- One line test running per SLAC device at a time.

Line Test Package

Table 13 provides a complete list of the supported line test algorithms and their library names in the Basic Test software package. Table 14 provides a list of all the tests performed when the GR909-All Test is run. Table 15 provides a list of all the tests performed when the Combined Multi-Test is run.

Table 13. Basic Test Package Supported Line Tests

Algorithm Names	Description	VP-Test Library Names	Config.			
			C	D	E	F
Foreign DC Voltage Test	To measure the DC foreign voltage present in the loop while the line card is in a high impedance state. A low-pass filter is used to filter out any AC voltage present on the line.	VPTL_TID_OPEN_DC_VOLTAGE	•	•	•[2]	•[2]
Foreign AC Voltage Test	To measure the AC foreign voltage present in the loop. A high pass filter is used to filter out any DC voltage present on the line.	VPTL_TID_OPEN_AC_VOLTAGE	•	•	•[3]	•[3]
DC Loop Resistance – Forward or Reverse Polarity Measurement	To measure low loop impedance values generally less than 4 kΩ. Using a fixed positive or negative polarity test current.	VPTL_TID_DC_LOOP_RES	•	•	•	•
DC Loop Resistance with Offset Compensation Measurement	To measure low loop impedance values generally less than 4 kΩ. The test is performed with both the positive and negative polarity currents to eliminate possible current offset.		•	•	•	•
Three-Element Insulation Resistance Test	To measure the resistances connected between Tip and Ground, Ring and Ground, and Tip to Ring. The test can also measure the foreign DC voltage and current. The test can measure foreign voltage sources in excess of the SLIC power supply rails.	VPTL_TID_3ELE_RES	•	•	•[4]	•[4]
Four-Element Insulation Resistance Test	To measure the resistances connected between Tip and Ground, Ring and Ground, Tip to Ring, and Ring to Tip using dual polarities for the metallic test signal.	VPTL_TID_4ELE_RES	•	•	•[4]	•[4]
Master Socket Test	To detect the presence of an M-Socket used in Hong Kong and a passive test termination (PPA - Passiver Prüfabschluss) used in the German telephony network. An M-Socket termination diagram is presented in Figure 7. A PPA termination diagram is presented in Figure 8.	VPTL_TID_MSOCKET	•	•	•	•
Three-Element Capacitance Test	To measure the capacitances connected between Tip and Ground, Ring and Ground, and Tip to Ring. This test also measures foreign AC voltage. The test can measure foreign voltage sources in excess of the SLIC power supply rails.	VPTL_TID_3ELE_CAP	•	•	•	•
Receiver Off-Hook Test	To distinguish between a receiver taken off hook and a line short.	VPTL_TID_ROH	•	•	•	•
Distance to Open Test	To diagnose a line to locate a cable cut. Returns the distance in meters between the central office and the cable cut.	VPTL_TID_DISTANCE_TO_OPEN	•	•	•	•
Foreign AC Currents Test	To measure the AC current flowing in each lead when the line is set to a specific common mode voltage.	VPTL_TID_FOREIGN_AC_ CURRENT	•	•	•	•
Ringer Equivalency Number Test	To measure REN characteristics of regular or electronic phones.	VPTL_TID_REN	•	•	•[5]	•[5]
DTMF and Pulse Digit Measurement Test	To detect and measure a DTMF digit, pulse digit, or hook-switch flash.	VPTL_TID_DTMF_PULSE_ MSRMNT	•	•	•	•
Arbitrary Single Tone Measurement Test	To measure the frequency and level of an arbitrary single tone that may be present on the loop.	VPTL_TID_ARB_TONE	•	•	•	•

Table 13. Basic Test Package Supported Line Tests (Continued)

Algorithm Names	Description	VP-Test Library Names	Config.			
			C	D	E	F
Draw and Break Dial Tone Test	Apply an off-hook load and detect the presence of dial tone on the loop. Return the characteristics of the tones (amplitudes and frequencies).	VPTL_TID_DRAW_BREAK_DIALTONE	•[1]	•	•[1]	•
Ringing Self Test	To verify the capability of the line card circuitry to generate a ringing voltage at the desired amplitude and to perform ring trip upon an off-hook event.	VPTL_TID_RINGING_SELF_TEST	•[1]	•		•[7]
Ringing Monitor Test	To measure the ringing voltage while applying normal ringing on a terminating call.	VPTL_TID_RINGING_MONITOR_TEST	•	•	•	•
Howler Test	British, Australian and North American Howler Tone generation.	VPTL_TID_HOWLER_TEST	•	•	•	•
Fuse Test	To verify the integrity of the fuses on the Tip and Ring leads.	VPTL_TID_FUSE_TEST	•	•	•	•
Read Loop and Battery Conditions	Read the loop conditions and high, low and positive battery voltages.	VPTL_TID_LOOP_BAT_COND_TEST	•	•	•[6]	•[6]
GR909-All Test	To execute the complete list of GR-909 tests in less than 2 seconds.	VPTL_TID_GR909_ALL	•	•	•	•
Combined Multi-Test	To execute a series of voltage, resistance, and capacitance tests in a minimal amount of time on a good loop.	VPTL_TID_MULTI_TEST	•	•	•[2, 3,4]	•[2, 3,4]

1. Configuration C and E have no disconnect relay. If there is no other means to disconnect the line from the loop during inward looking test, Self Tests can only be performed in the factory. The published Self Test accuracies are given for production testing only when no loop is connected to the equipment port. If the Self Tests are performed in the field, the host application needs to interpret the data accordingly, taking into account any loop impedance present.

2. Minor functional difference on how test is performed and reduced range with Configuration E and F for Foreign DC Voltage Tests. Refer to VoicePath™ API-II Test Library User's Guide for details.

3. Reduced range with Configuration E and F for Foreign AC Voltage Tests. Refer to VoicePath™ API-II Test Library User's Guide for details.

4. Range reduction in low resistance measurements with Configuration E and F for Resistance Tests. Refer to VoicePath™ API-II Test Library User's Guide for details.

5. Some restrictions on the input parameter selection range apply with Configuration E and F due to the absence of a VBP supply. Refer to VoicePath™ API-II Test Library User's Guide for details.

6. Can not measure IMT and ILG currents when in the ringing mode.

7. Requires a test load and a relay on the Test-In bus. Apply a 2.55 KΩ, 0.25%, 1W, 50 ppm resistor across the Test-In bus.

Table 14. GR-909 Tests and their corresponding Test Library Names

GR-909 test names	Description	Test Library Names
Outward loop testing		
Hazardous potential test AC	To measure the foreign AC Voltage present in the loop. A high pass filter is used to filter out any DC voltage present on the line.	VPTL_TID_OPEN_AC_VOLTAGE
Foreign voltage test AC		
Hazardous potential test DC	To measure the foreign DC Voltage present in the loop while the card is in a high impedance state	VPTL_TID_OPEN_DC_VOLTAGE
Foreign voltage test DC		
Resistive fault test	To measure any resistive fault present between Tip and Ground, Ring and Ground, Tip and Ring.	VPTL_TID_3ELE_RES
Receiver off-hook test	To verify the difference between a receiver taken off-hook and a line short.	VPTL_TID_ROH
Ringer test	To measure the ringer equivalence number of a phone	VPTL_TID_REN
GR-909 tests	Performs all outward loop tests	VPTL_TID_GR909_ALL

Table 15. Combined Multi-Tests and their corresponding Test Library Names

Combined Multi-Test names	Description	Test Library Names
Outward loop testing		
Measure DC voltages	Measures Tip, Ring, and Differential DC voltages.	VPTL_TID_OPEN_DC_VOLTAGE
Measure AC voltages	Measures Tip, Ring, and Differential AC RMS voltages.	VPTL_TID_OPEN_AC_VOLTAGE
Measure Capacitances	Measures Tip-to-ground, Ring-to-ground, and Tip-to-Ring capacitances.	VPTL_TID_3ELE_CAP
Measure Resistances	Measures Tip-to-ground, Ring-to-ground, Tip-to-Ring, and Ring-to-Tip resistances.	VPTL_TID_4ELE_RES

Measurement Range and Accuracy

Table 16 presents measurement ranges and accuracies for the Configuration C & E topologies. Table 17 presents measurement ranges and accuracies for the Configuration D & F topologies. Accuracies are specified for the recommended sense resistor tolerance. Accuracies apply to the recommended application circuits and parts lists that are defined in the *NGCC Hardware Design Guide, Document ID 126583*. Refer to the notes following the tables for additional information.

Table 16. Configuration C & E Measurement Range and Accuracy[8]

			CONFIGURATION C & E			
			RSVA/RSVB ±0.5%, 100 ppm/ºC			
Test Library Function	**Specific Test**	**Notes/Parameter**	**From**	**To**	**Unit**	**Accuracy/ Specification**
VPTL_TID_OPEN_DC_VOLTAGE	Tip or ring voltage	Notes 1, 2, 5, 7	-1000	-400	V	±2.2% & ±3.0 V
			-400	400		±1.9% & ±1.0 V
			400	1000		±2.2% & ±3.0 V
		AC induction rejection	0	280	Vrms	> 40 dB
VPTL_TID_OPEN_AC_VOLTAGE	Tip or ring voltage	Notes 1, 2, 5, 7	0	280	Vrms	±1.9% & ±0.05 V
			280	700		±2.2% & ±0.2 V
		Frequency Range	50	200	Hz	
		Foreign DC rejection	-400	400	V	> 40 dB
	Differential voltage	Notes 1, 2, 5, 7	0	280	Vrms	±2.65% & ±0.05 V
			280	700		±3.1% & ±0.2 V
		Frequency Range	50	200	Hz	
		Common-mode Rejection	0	280	Vrms	< 2%
		Foreign DC rejection	-400	400	V	> 40 dB
VPTL_TID_DC_LOOP_RES	Test with offset compensation	Notes 2, 5, 10	0	4	kΩ	±6% & ±10 Ω
		Note 11	5	70	mA	±4.0% & ±2.0 mA
VPTL_TID_REN	Mechanical ringer test	Notes 2, 5	1	10	kΩ	±5% & ±20 Ω
			10	100	kΩ	±6%
		Signal Frequency Range	10	80	Hz	
	Electronic ringer test	With 500 Ω to 7500 Ω series resistor and >100 kΩ parallel resistor (Note 2)	0	4	µF	±6% & ±50 nF
VPTL_TID_3ELE_RES, VPTL_TID_4ELE_RES	Resistance to GND	Notes 2, 3, 5	1*	1000*	Ω	±4.0% & ±10 Ω
			1	10	kΩ	±4.0% & ±10 Ω
			10	30		±4.25%
			30	100		-4.75%, +5.4%
			100	150		-5.75%, +6.8%
			150	360		-10%, +14%
			360	1000		-23%, +36%
			1	2	MΩ	-65%, +100%
	Resistance A to B	Notes 2, 3, 5	1*	1000*	Ω	±4.0% & ±20 Ω
			1	10	kΩ	±4.0% & ±20 Ω
			10	30		±4.1%
			30	100		±4.0%
			100	150		±4.1%
			150	360		±4.3%
			360	1000		±6%
			1	5	MΩ	-20%, +40%
			5	10		-40%, +50%
	*The 1 to 1000 ohm range applies to Configuration C only					

Table 16. Configuration C & E Measurement Range and Accuracy[8] (Continued)

			CONFIGURATION C & E			
			RSVA/RSVB ±0.5%, 100 ppm/ºC			
Test Library Function	**Specific Test**	**Notes/Parameter**	**From**	**To**	**Unit**	**Accuracy/ Specification**
VPTL_TID_3ELE_RES	Foreign DC currents	IAE + IBE (Notes 2, 5, 6)	0	80	mA	±5% & ±1.2 mA
		AC current rejection	0	40	mA_{rms}	> 40 dB
VPTL_TID_3ELE_CAP	Capacitance to GND	Notes 2, 3, 5	0	100	nF	±4.1% & ±0.55 nF
			100	1000	nF	±4.1% & ±1.0 nF
			1	20	µF	±4.45%
			20	50	µF	±5.2%
	Capacitance A to B	Notes 2, 3, 5	0	100	nF	±4.1% & ±0.55 nF
			100	1000	nF	±4.15% & ±0.75 nF
			1	20	µF	±4.0%
			20	50	µF	±4.3%
		Signal Frequency Range	10	200	Hz	
VPTL_TID_FOREIGN_ AC_CURRENT		IAE + IBE (Notes 2, 5, 6)	0.1	50	mA_{rms}	±5% & ±0.01 mArms
		Frequency Range	50	200	Hz	
		DC current rejection	-60	60	mA	> 40 dB
VPTL_TID_DTMF_PULSE_ MSRMNT	Dial pulse test	Dial Speed	8	12	pps	±1.0%
		Break Interval	40	80	%	±1.0%
		Dial Speed	18	22	pps	±2.0%
		Break Interval	40	80	%	±2.0%
	DTMF test	DTMF Level (Notes 4, 5)	-20	0	dBm	±1.0 dB
		DTMF Level (Notes 4, 5)	-25	-20	dBm	±1.5 dB
		DTMF Frequency (Notes 4, 5)	600	2000	Hz	±2 Hz
VPTL_TID_ARB_TONE		Notes 4, 5, 9	-40	0	dBm	±0.5 dB
			300	3400	Hz	±2 Hz
VPTL_TID_DRAW_BREAK_ DIALTONE	Self Test	Notes 4, 5, 9	-40	0	dBm	±0.5 dB
			300	800	Hz	±2 Hz

Table 17. Configuration D & F Measurement Range and Accuracy[8]

			CONFIGURATION D & F			
			RSVA/RSVB ±0.5%, 100 ppm/ºC			
Test Library Function	**Specific Test**	**Notes/Parameter**	**From**	**To**	**Unit**	**Accuracy/ Specification**
VPTL_TID_OPEN_DC_VOLTAGE	Tip or ring voltage	Notes 1, 2, 5, 7	-1000	-400	V	±2.2% & ±3.0 V
			-400	400		±1.9% & ±0.05 V
			400	1000		±2.2% & ±3.0 V
		AC induction rejection	0	280	Vrms	> 40 dB
VPTL_TID_OPEN_AC_VOLTAGE	Tip or ring voltage	Notes 1, 2, 5, 7	0	280	Vrms	±1.9% & ±0.05 V
			280	700		±2.2% & ±0.2 V
		Frequency Range	50	200	Hz	
		Foreign DC rejection	-400	400	V	> 40 dB
	Differential voltage	Notes 1, 2, 5, 7	0	280	Vrms	±2.65% & ±0.05 V
			280	700		±3.1% & ±0.2 V
		Frequency Range	50	200	Hz	
		Common-mode Rejection	0	280	Vrms	< 2%
		Foreign DC rejection	-400	400	V	> 40 dB
VPTL_TID_DC_LOOP_RES	Test with offset compensation	Notes 2, 5, 10	0	4	kΩ	±6% & ±10 Ω
		Note 11	5	70	mA	±4% & ±2 mA
VPTL_TID_REN	Mechanical ringer test	Notes 2, 5	1	10	kΩ	±5% & ±20 Ω
			10	100	kΩ	±6%
		Signal Frequency Range	10	80	Hz	
	Electronic ringer test	With 500 Ω to 7500 Ω series resistor and >100 kΩ parallel resistor (Note 2)	0	4	µF	±6% & ±50 nF
VPTL_TID_3ELE_RES, VPTL_TID_4ELE_RES	Resistance to GND	Notes 2, 3, 5	1*	1000*	Ω	±4% & ±10 Ω
			1	10	kΩ	±4% & ±10 Ω
			10	30		±4.25%
			30	100		±4.0%
			100	150		±4.0%
			150	360		±4.15%
			360	1000		±5.1%
			1	5	MΩ	-12%, +15%
			5	10		-20%, +35%
			10	20		-33%, +100%
	Resistance A to B	Notes 2, 3, 5	1*	1000*	Ω	±4% & ±20 Ω
			1	10	kΩ	±4% & ±20 Ω
			10	30		±4.35%
			30	100		±4.0%
			100	150		±4.0%
			150	360		±4.15%
			360	1000		±5.1%
			1	5	MΩ	-12%, +15%
			5	10		-20%, +35%
			10	20		-33%, +100%
	* The 1 to 1000 ohm range applies to Configuration D only					

Table 15. Configuration D & F Measurement Range and Accuracy[8] (Continued)

			CONFIGURATION D & F			
			RSVA/RSVB ±0.5%, 100 ppm/ºC			
Test Library Function	**Specific Test**	**Notes/Parameter**	**From**	**To**	**Unit**	**Accuracy/ Specification**
VPTL_TID_3ELE_RES	Foreign DC currents	IAE + IBE (Notes 2, 5, 6, 10)	0	80	mA	±5% & ±0.2 mA
		AC current rejection	0	40	mA_{rms}	> 40 dB
VPTL_TID_3ELE_CAP	Capacitance to GND	Notes 2, 3, 5	0	100	nF	±4.1% & ±0.2 nF
			100	1000	nF	±4.1% & ±0.9 nF
			1	20	µF	±4.45%
			20	50	µF	±5.2%
	Capacitance A to B	Notes 2, 3, 5	0	100	nF	±4.1% & ±0.25 nF
			100	1000	nF	±4.15% & ±1.1 nF
			1	20	µF	±4.0%
			20	50	µF	±4.3%
		Signal Freq. Range	10	200	Hz	
VPTL_TID_FOREIGN_ AC_CURRENT		IAE + IBE (Notes 2, 5, 6)	0.1	50	mA_{rms}	±5% & ±0.01 mArms
		Freq. Range	50	200	Hz	
		DC current rejection	-60	60	mA	> 40 dB
VPTL_TID_DTMF_PULSE_ MSRMNT	Dial pulse test	Dial Speed	8	12	pps	±1.0%
		Break Interval	40	80	%	±1.0%
		Dial Speed	18	22	pps	±2.0%
		Break Interval	40	80	%	±2.0%
	DTMF test	DTMF Level (Notes 4, 5)	-20	0	dBm	±1.0 dB
		DTMF Level (Notes 4, 5)	-25	-20	dBm	±1.5 dB
		DTMF Frequency (Notes 4, 5)	600	2000	Hz	±2 Hz
VPTL_TID_ARB_TONE		Notes 4, 5, 9	-40	0	dBm	±0.5 dB
			300	3400	Hz	±2 Hz
VPTL_TID_DRAW_BREAK_ DIALTONE	Self Test	Notes 4, 5, 9	-40	0	dBm	±0.5 dB
			300	800	Hz	±2 Hz
	Inward test	Notes 4, 5	-20	0	dBm	±1.0 dB
			300	800	Hz	±2 Hz

Notes:

1. *The total voltage range is ±1000 V for the sum of AC and DC signals and may be further limited by the protection devices.*
2. *Absolute and relative tolerances are additive.*
3. *Accuracies only apply to a real resistor or to a real capacitor of the exact value of the test load. Resistance and Capacitance measurement accuracies are given for a single element present. The presence of an impedance in any of the other two branches may cause >50 times this impedance to appear in the branch under test and will degrade the observed accuracy. This is also true for the branches that are open. When performing the 3 element measurement the test will measure all 3 branches, whether the branches are open or not.*
4. *Accuracies are given for FFT sizes of 1024 or more.*
5. *Accuracies are given for testing in the absence of interference from a foreign AC or DC voltage.*
6. *The total current range is ±80 mA for the sum of the AC and DC signals.*
7. *The specified tolerance for RSVA and RSVB is ±0.5% with a temperature coefficient of resistance of 100 ppm/ºC. Stated performance is only validated and guaranteed for the ±0.5%, 100 ppm/ºC resistor. If a looser tolerance resistor is used, DC voltage and AC voltage measurement accuracies need to be relaxed. For instance, if a resistor with a ±1% tolerance and a 200 ppm/ºC temperature coefficient of*

resistance is used, then widen the listed VPTL_TID_OPEN_DC_VOLTAGE and VPTL_TID_OPEN_AC_VOLTAGE accuracies by 0.2%. If non-standard configurations are used, the customer must undertake validation with due diligence.

8. *Additional notes with regards to stated accuracies. Accuracies are set at 99% of the estimated distribution including all BOM component tolerances as documented in the NGCC Hardware Design Guide, Doc ID 126583. Tolerance for any overcurrent protection PTC component is ±10%.*
9. *The accuracy figures provide the tolerances to be applied to the nominal transmit path frequency response computed by WinSLAC for the AC profile and the signal source impedance used during the test.*
10. *Using the two-step method with offset cancellation.*
11. *The achievable current will be limited by the driver output voltage as a function of the load under test.*

Termination and Signature Network Diagrams

Figure 7. M-Socket Termination

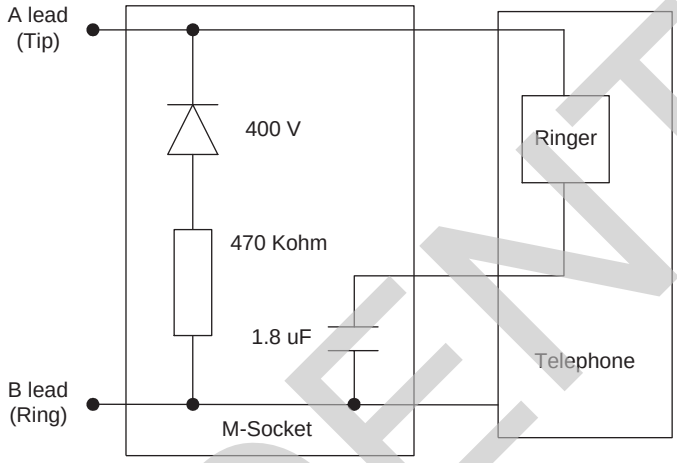
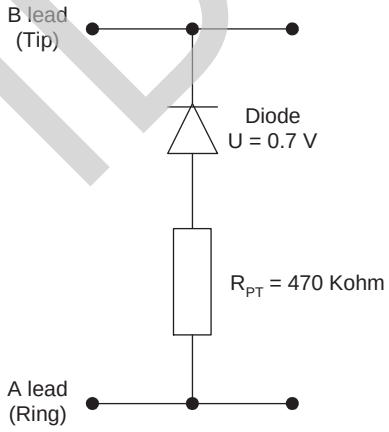


Figure 8. PPA Termination



REVISION HISTORY

Revision 1 to 2

- Removed Call Control Software Package.

Revision 2 to 3

- Added Le79258 Octal External Ringing SLAC device (ZL792588) to Software Package.

Revision 3 to 4

- Change Le79258 to read ZL79258.
- Page 6, modified Host Bus Interface and Hardware Architecture descriptions.
- Added Basic Test to Software Termination Type VP_TERM_FXS_RR.
- Add Software Termination Type VP_TERM_FXS_RR_TI.
- Page 15 - 18, modified VPTL_TID_OPEN_DC_VOLTAGE, VPTL_TID_OPEN_AC_VOLTAGE, VPTL_TID_DC_LOOP_RES, VPTL_TID_REN, VPTL_TID_3ELE_RES, VPTL_TID_4ELE_RES, VPTL_TID_3ELE_RES, VPTL_TID_3ELE_CAP, and VPTL_TID_FOREIGN_AC_CURRENT accuracies.
- Page 19, modified notes 6 and 8.

Revision 4 to 5

- Added VP_TERM_FXS_RR_MW termination type.
- Table 16 and 17, added Note 2 to VPTL_TID_REN test.

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