Le88010

Single Channel VoicePort™ SLAC™ Device
VE880 Series
Datasheet

APPLICATIONS

- **Voice-Enabled DSL Modems**
- **Voice Over IP/ATM**
- **Integrated Access Devices (IAD)**
- **Smart Residential Gateways (SRG) and Routers**
- **Set-Top Box with PSTN Line Interface**
- **PBX Trunk Interface**
- **FXO Interfaces**

FEATURES

- **In Combination with a DAA, Provides a Complete Phone Line Termination-to-Digital Interface Solution**
  - — Fully programmable SLAC device
  - — Disconnect, Ringing signal, Line-in-use and Line polarity detection,
  - — Line supervision for parallel devices connecting to subscriber line
  - — Small footprint package - 44-pin QFN
  - — Minimal external discrete components required
- **Compatible with Solid State or Transformer DAA Interfaces**
- **High-Speed, Pin-Selectable PCM/MPI or GCI Interface**
- **Microprocessor Interface**
- **GCI Interface Option**
- **Programmability**
  - — Two-wire AC impedance
  - — Input/Output mode selection for one relay driver and five general purpose digital I/O pins.
  - — Adapts to all ringing frequencies
  - — Disconnect, line polarity and line-in-use thresholds
  - — DTMF tone generators
  - — Dial pulse and DTMF cadence
- **Special Feature Support**
  - — DTMF tones
  - — Dial pulses
  - — Caller ID pass-through
  - — Numeric address signaling
  - — On-hook transmission
- **Integrated 150 mW 3-V or 5-V Relay Driver**
  - — Supports lifeline POTnS in DSL IAD applications

Document **ID # 081201** **May 2015**

ORDERING INFORMATION

Device	Package Type[1]	Packing[2]
Le88010BQC	44-pin QFN (Green)	Tray

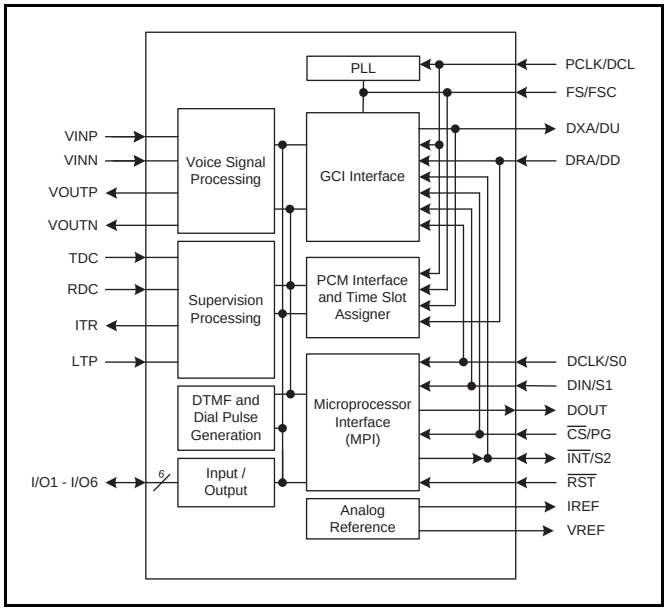
1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

The Legerity Le88010 VoicePort™ SLAC™ device, in combination with an analog DAA, implements all the voice functions necessary to properly terminate and monitor the customer premises side of a PSTN line and provide linear or G.711 A- or µ-Law encoded voice output over a standard PCM or GCI highway. The Le88010 device is ideal for use in voice enabled DSL modems that implement lifeline POTS and support PBX functionality.

This device reduces system level cost, space, and power by achieving a high level of voice integration and adds programmability of transmission and signaling features. Designers benefit by having a simple, cost effective, low power and dense, interface design without sacrificing features or functionality.

VOICEPORT™ SLAC™ BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The Le88010 device implements a single channel telephone line termination. When used in a voice over broadband application, with the addition of an external line interface (DAA), the Le88010 simulates the functions of a telephone when connected to the CPE end of a subscriber line. These include line seizure support, AC impedance matching, DTMF and dial pulse generation.The Le88010 detects the presence of ringing signal and signals when an additional telephone connected to the subscriber line has gone off hook. The device selectively interfaces with a PCM or GCI backplane and can be controlled over the MPI or GCI interface.

DETAILED FEATURES OF THE LE88010 VOICEPORT™ SLAC™

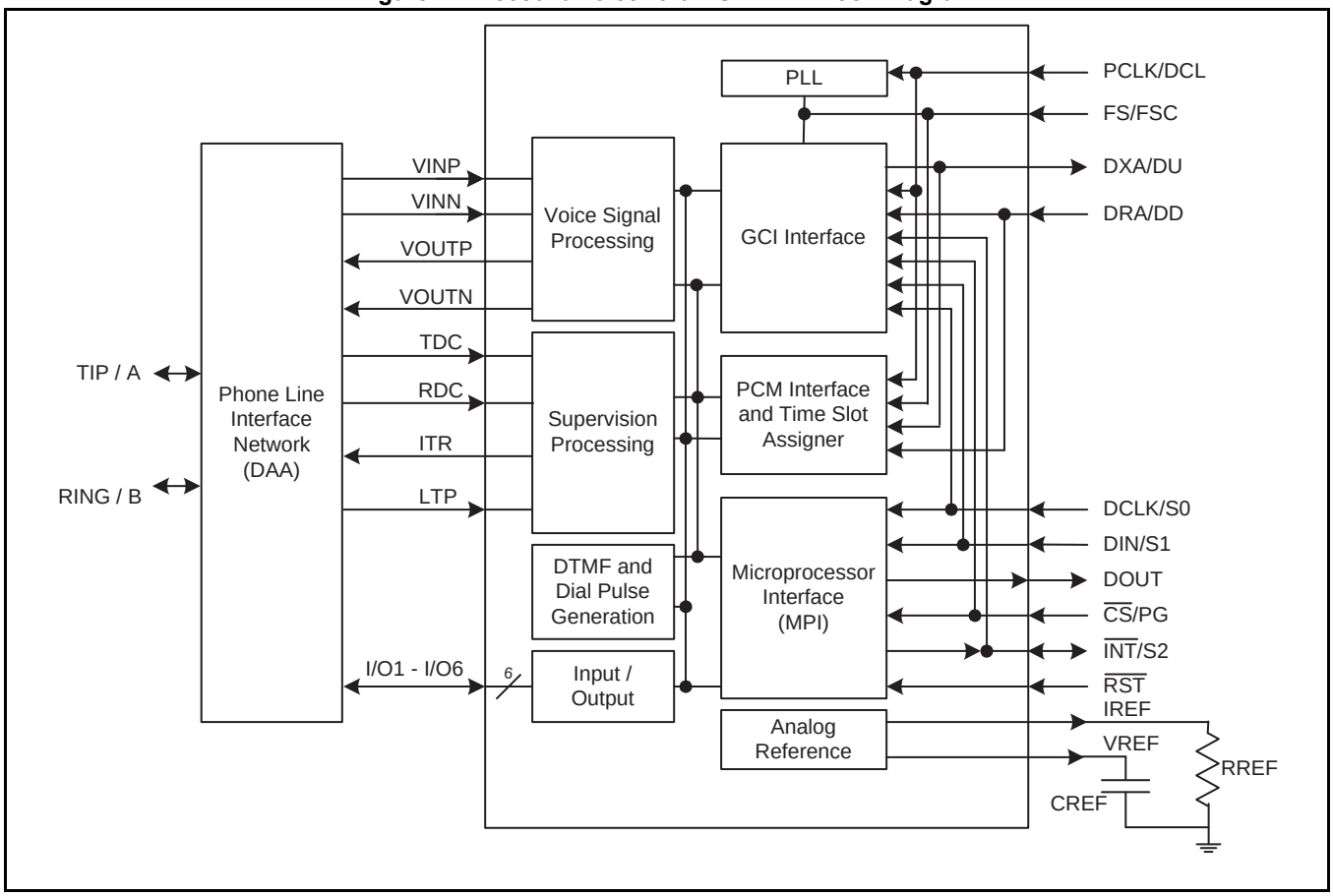
The Le88010 VoicePort SLAC supports the following features:

- Single chip solution provides a 4-wire analog interface, a digital signal processor and PCM highway interface
- Meets FCC Part 68 interconnection requirements
- Single hardware design meets worldwide requirements through software programming of:
  - Line seizure relay driver for use with transformer type line interfaces
  - Loop-supervision detection thresholds
  - Loop supervision debounce
  - Two-wire AC impedance synthesis
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Transmit and receive equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
  - DTMF and dial pulse cadencing
- On-hook transmission
- Flexible dialing signals
  - DTMF tone generation
  - Dial pulse generation
- Only 3.3 V supply needed
- MPI/PCM interface
  - Supports most required PCM clock frequencies from 1.536 MHz to 8.192 MHz
- GCI interface
  - Supports 2.048 MHz or 4.096 MHz DCL
- Monitors two-wire interface voltages for presence of ringing, line polarity and parallel phone off-hook.
- Built-in voice-path test modes
- Integrated self-test features
- Monitors two-wire interface voltages for subscriber line diagnostics
- Can monitor Tip and Ring independently
- Internal relay driver and five general purpose I/O pins
- Small physical size in 7 x 7 mm QFN
- –40°C to 85°C operation

BLOCK DESCRIPTIONS

The device includes a PLL to generate the necessary clocks for the internal processing functions, digital interfaces implemented in the PCM, MPI and GCI blocks, digital I/O, analog references, voice signal processor, supervision, DTMF and dial pulse generation blocks.

Figure 1. Le88010 VoicePort™ SLAC™ Block Diagram



Digital Interfaces

The Le88010 device offers two digital interface options. The first is PCM/MPI mode, in which separate serial control and voice data interfaces are provided. Voice data is interfaced via a PCM highway with time slot assignment capability, and control information is communicated over the MicroProcessor Interface. The second is GCI mode, in which a single serial interface supports both voice data and control.

The two modes are mutually exclusive and have different advantages and disadvantages. The PCM/MPI mode is most flexible and allows a wide range of DCLK (MPI data clock) and PCLK (PCM data clock) frequencies. PCM/MPI mode also allows use of the $\overline{\text{INT}}$ interrupt pin to signal pending interrupts to the external controller. GCI mode offers the advantage that it uses only 4 signals (FSC, DCL, DU, DD) to carry voice and control data. PCM/MPI mode uses twice as many signals (FS, PCLK, DXA, DRA for voice data and CSL, DCLK, DIN, DOUT for control data) to carry the same information. GCI mode has several disadvantages, however: only 2.048 MHz and 4.096 MHz DCL frequencies are allowed; the control interface is slow (250 µS/byte maximum throughput); and interrupt handling is more complex due to the lack of an interrupt pin. Multifunction pins are implemented to support these different modes while keeping the pin count low.

PCM and GCI Mode Selection

The Le88010 device enters PCM/MPI or GCI modes based on the conditions outlined in Table 1, on page 7.

The PCM / $\overline{\text{GCI}}$ select pin ($\overline{\text{CS}}$/PG) is used in combination with the DCLK pin to determine which mode the device is in on power up. If PG is held low and DCLK is held static, GCI mode is entered after two frames following power up or hardware reset. GCI mode will be exited at any time if PG is pulled high or a clock is detected on DCLK.

If PG is High then PCM/MPI mode is entered following power up. At this point, the mode can be changed to GCI if the GCI conditions are met. However, once a command is sent over the MPI interface, GCI mode cannot be entered without resetting the device.

Table 1. PCM/GCI Mode Selection

From mode	To mode	Requirement
Power On or Hardware Reset	PCM	$\overline{CS}$/PG = 1 *or* DCLK has ac clock present
Power On or Hardware Reset	GCI	$\overline{CS}$/PG = 0 *and* DCLK does not have ac clock present
GCI	PCM	$\overline{CS}$/PG = 1 *or* DCLK has ac clock present
PCM	GCI	No commands yet sent in PCM state *and* $\overline{CS}$/PG = 0 (for more than 2 FS) *and* DCLK does not have ac clock present

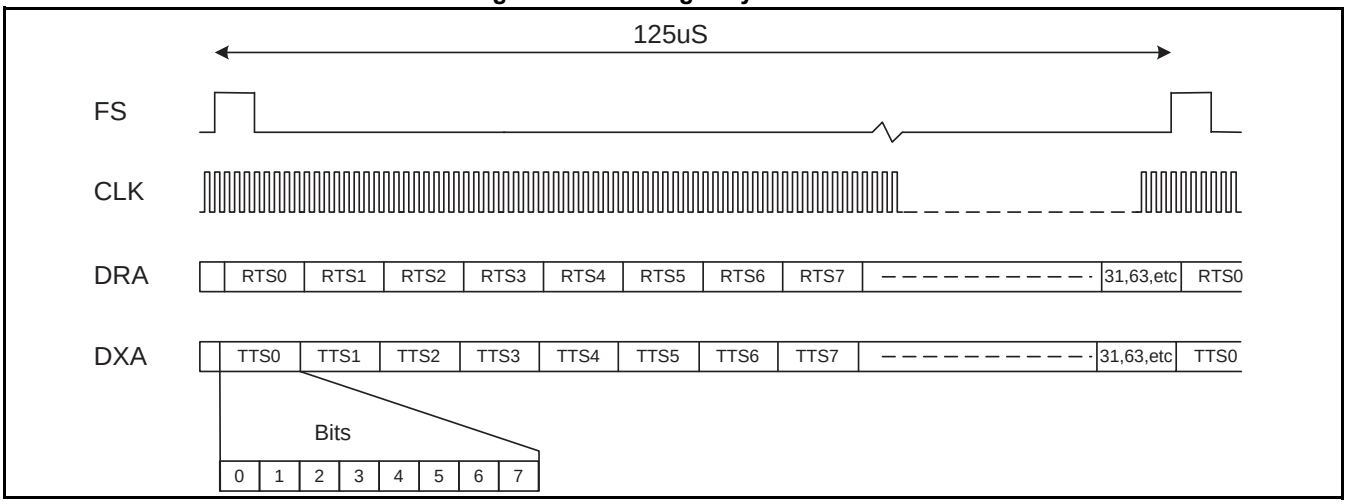
These methods are used to ensure the device operates in the desired mode at all times.

PCM/MPI Interface and Time Slot Assigner

This is a synchronized serial mode of communication between the system and the Le88010 device. In PCM mode, data can be transmitted/received on a serial PCM highway. This highway uses FS and PCLK as reference.

Data is transmitted out of the DXA pin and received on the DRA pin. The Le88010 device transmits/receives 8-bit (A-law/µ-law) compressed voice data and 16-bit two's complement linear voice data. Data is transmitted/received in 8-bit time slots. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The Frame Sync (FS) pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the Le88010 device, the frequency of the FS signal is 8 kHz. The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 49. For each channel, voice data compression and type of coding is selected by the C/L (Compressed/Linear) and A/µ-law bits in command *60/61h Write/Read Operating Functions*, on page 54.

Figure 2. PCM Highway Structure



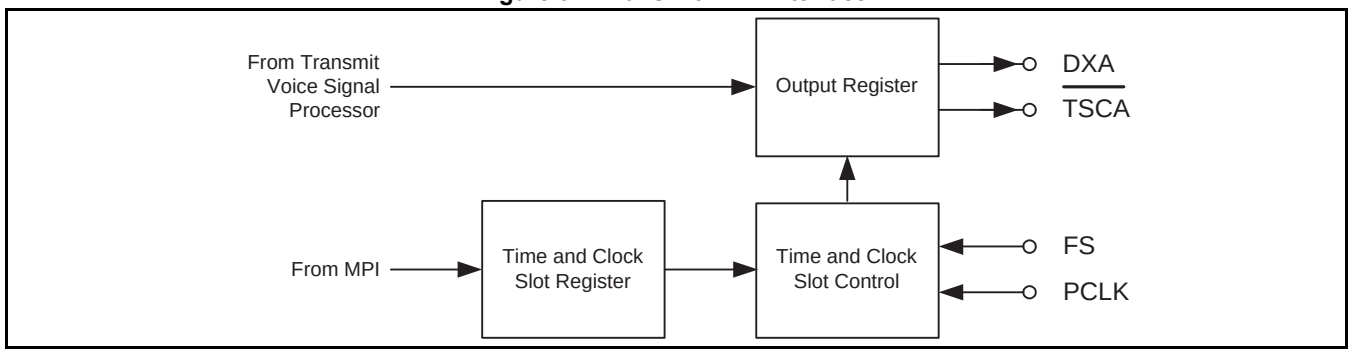
The Le88010 device command *44/45h Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge*, on page 49 allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Figure 2 shows the PCM highway time slot structure.

Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (A-law/µ-law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic (Figure 3) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK. The clock edge on which the data is transmitted is selected by the XE bit in the Transmit and Receive Clock Slot Register (Command 44h/45h).

Command *40/41h Write/Read Transmit Time Slot*, on page 49 allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots (using a PCLK of 8.192 MHz) in each frame. The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 49, this means that for compressed data the number of 8-bit time slots can vary between 24 and 128, while linear mode supports between 12 and 64 16-bit time slots. Note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Figure 5, on page 9 illustrates data flow on the PCM highway.

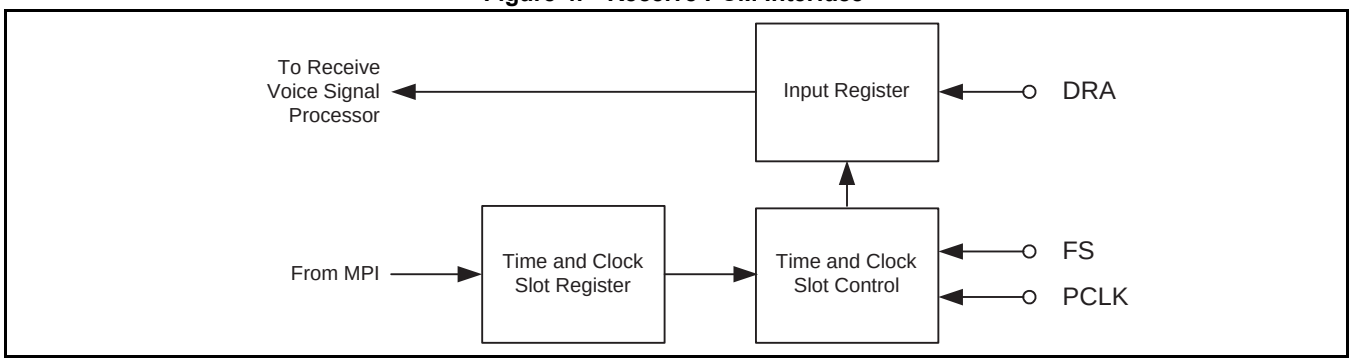
Figure 3. Transmit PCM Interface



Receive PCM Interface

The receive PCM interface logic (Figure 4) controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/ µ-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

Figure 4. Receive PCM Interface



Command *42/43h Write/Read Receive Time Slot*, on page 49 allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots (using a PCLK of 8.192 MHz) in each frame. The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 49, this means that for compressed data the number of 8-bit time slots can vary between 24 and 128, while linear mode supports between 12 and 64 16-bit time slots. Note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Figure 5, on page 9 illustrates data flow on the PCM highway.

Signaling on the PCM Highway

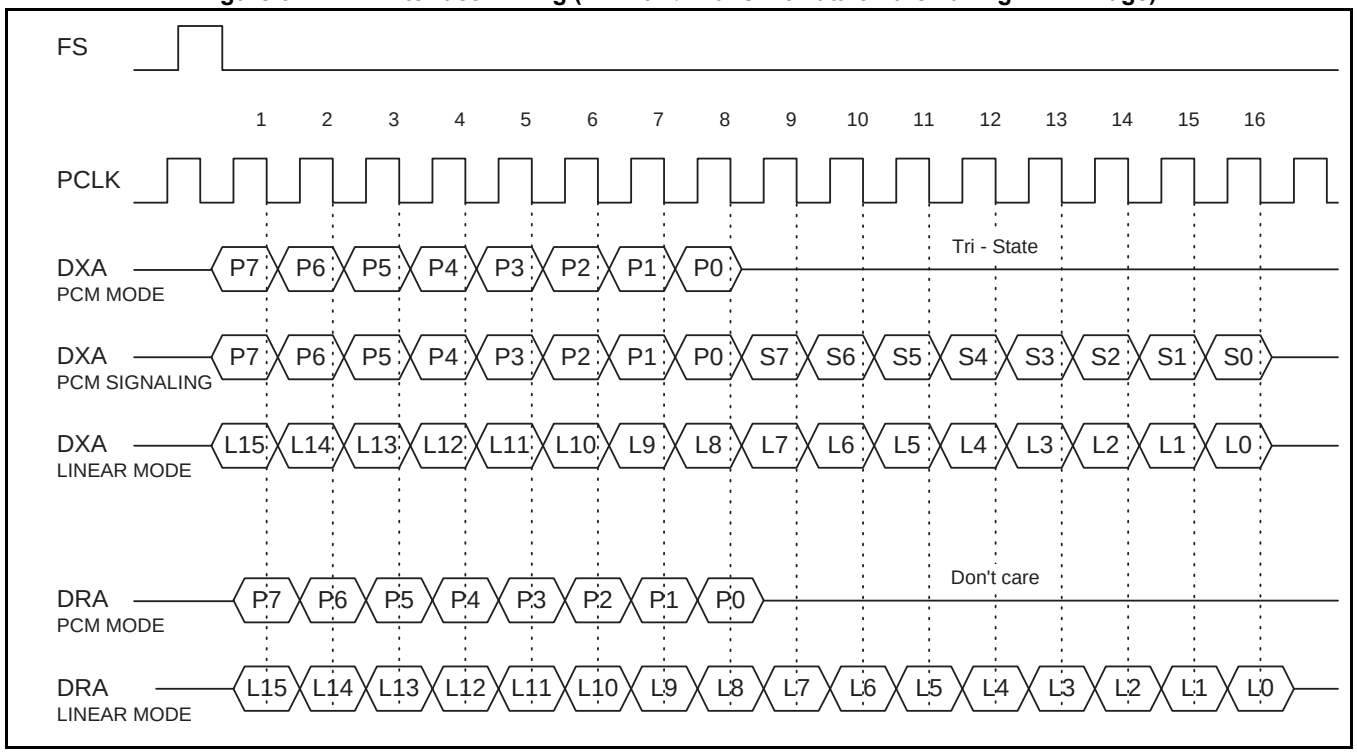
Signaling information can be sent on the PCM output if A- or µ-Law companding is selected and the SMODE bit in command *46/47h Write/Read Device Configuration Register*, on page 49 is set. In this case an extra time slot of signaling data is transmitted every frame immediately after the PCM voice data (see Figure 5, on page 9) and is transmitted whether or not the voice channel is active. The signaling data is defined in Table 2.

Table 2. PCM Highway Real Time Signaling Data Definition

S7	S6	S5	S4	S3	S2	S1	S0
CFAIL	POH	POL	IO2	CAD	DIS	RNGDT	LIU

Masking or unmasking of the interrupts in the interrupt mask register does not affect the real time signaling data.

Figure 5. PCM Interface Timing (XE = 0 ⇒ Transmit Data on the Falling PCLK Edge)



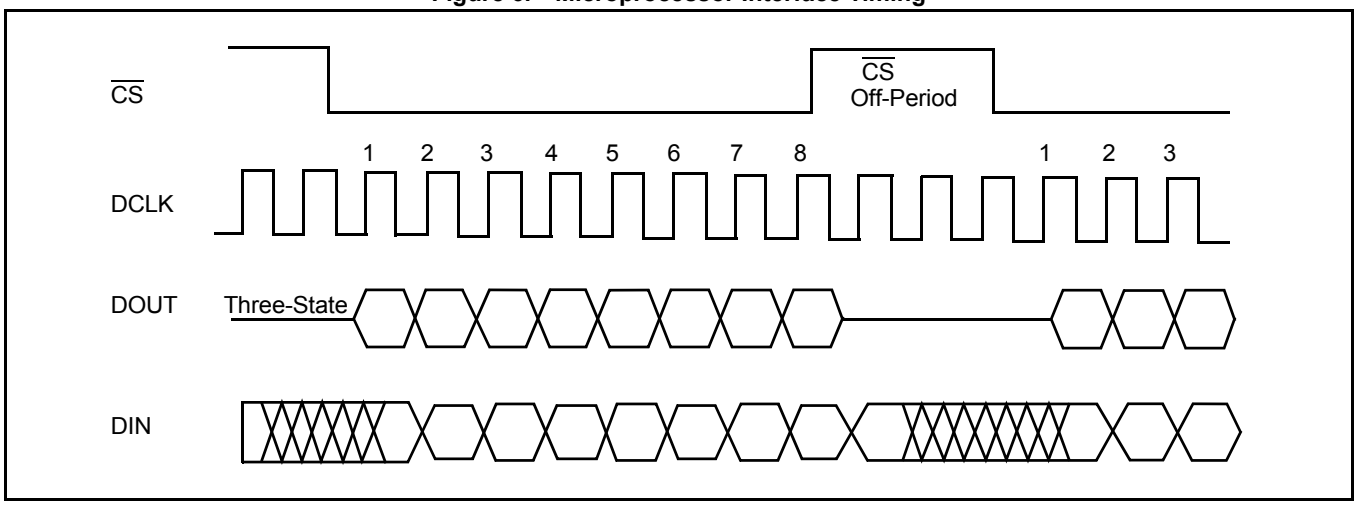
MICROPROCESSOR INTERFACE (MPI)

The microprocessor interface (MPI) block communicates with the external host microprocessor over a serial interface. It passes user control information to the other blocks, and it passes status information back to the external host.

The MPI physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), a chip select ($\overline{CS}$) and an interrupt signal ($\overline{INT}$) (see Figure 6, on page 10). The serial input consists of 8-bit commands that can be followed with additional bytes of input data, or can be followed by the Le88010 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The Le88010 device will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified. Note that the Voice Channel Enable bit, EC in command *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 50 can be used to control access to voice channel specific registers within the device.

Figure 6. Microprocessor Interface Timing



An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le88010 devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in the High state indefinitely. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a High level. If the system controller has a single bi-directional serial data pin, the DOUT pin of the Le88010 device can be connected to its DIN pin.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes Low, data will be present at the DOUT pin even if DCLK has no activity.

Interrupt Servicing in MPI Mode

The Le88010 device has a well-defined interrupt structure. All the interrupts in the Le88010 device can be masked. Interrupts are caused only when a status bit is unmasked and the status bit is subsequently set or toggles (depending on the interrupt).

The Le88010 device generates interrupts in response to a number of line supervision events. When an interrupt is generated, its status is placed in *4D/4Fh Read Signaling Register*, on page 50. Multiple interrupts can be reported in the signaling register. When the first interrupt occurs, the interrupt pin, $\overline{INT}$, will be pulled Low to signal the external microprocessor that an interrupt has occurred. When the external microprocessor has serviced the interrupts by reading the signaling register and clearing the interrupt (Command 4Fh) or *CDh Read Transmit PCM/Test Data*, on page 63 if ATI is set, the $\overline{INT}$ pin will go High. An interrupt is generated whenever its corresponding status bit changes (1 to 0 or 0 to 1) and its mask bit is unmasked. Therefore, the software application is responsible for keeping track of the its previous status and deciding the transition type (rising edge transition or falling edge transition). The interrupt pin drive mode can be programmed to be 3.3-V CMOS push/pull or open drain. Signaling status can also be polled without upsetting any pending interrupt status by using command 4Dh.

The following status bits can cause an interrupt to occur:

CFAIL:	PCM clock (PCLK) or 8 kHz frame sync (FS) failure
POH:	Parallel off Hook has been detected
POL:	Polarity of line voltage has changed
IO2:	Input 2 Status. The input value at IO2 has changed
CAD:	Cadencer interrupt when programmed on period is completed
DIS:	Line Disconnected status
RNGDT:	Ringing Detect
LIU:	Line In Use (Significant when on hook)

General Circuit Interface (GCI)

In GCI mode, this block carries both control and data on the same serial bus, replacing both MPI and PCM functionality. When the $\overline{CS}$/PG device pin is connected to DGND and DCLK/S0 is static (not toggling), GCI operation is selected. The Le88010 device conforms to the GCI standard where data for eight GCI packets are combined into one serial bit stream. A GCI packet contains the control and voice data for the analog channel of the Le88010 device. The Le88010 device sends Data Upstream out of the DU pin and receives Data Downstream on the DD pin. Data clock rate and frame synchronization information goes to the Le88010 device on the DCL (Data Clock) and FSC (Frame Sync.) input pins, respectively.

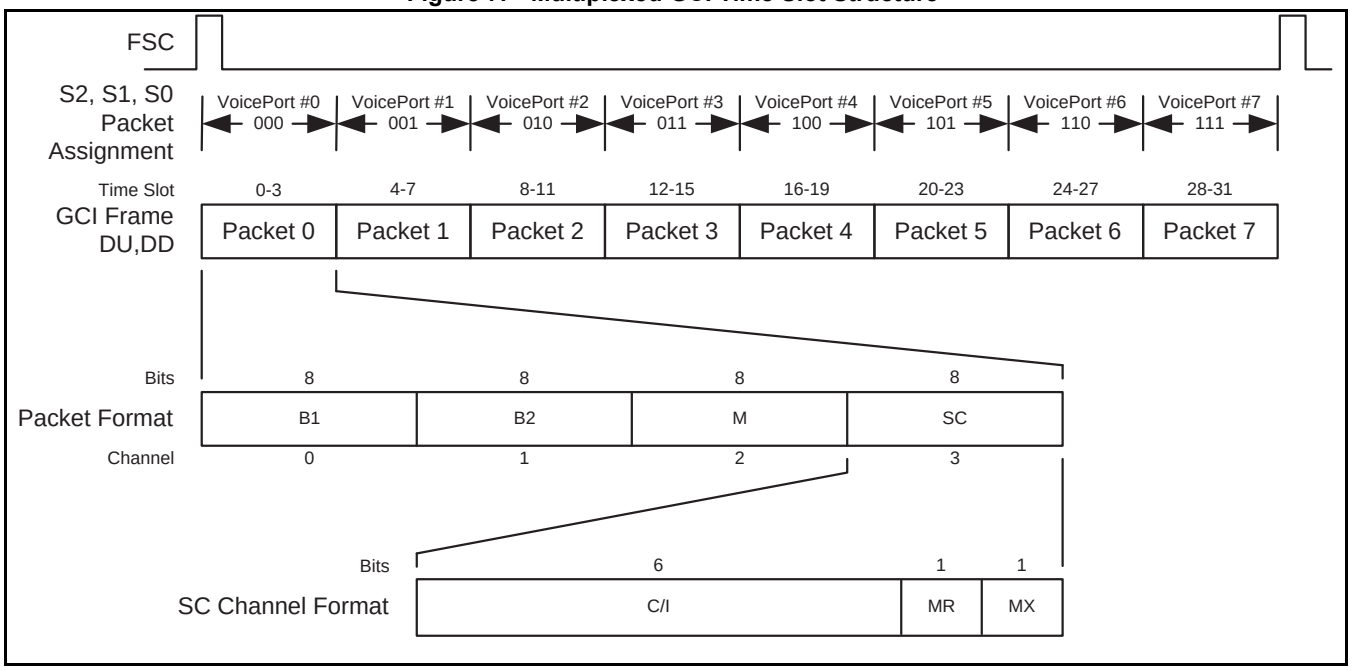
GCI Format and Command Structure

The GCI interface provides communication of both control and voice data between the GCI highway and subscriber Voice Ports over a single pair of pins on the Le88010 device. A complete GCI frame is sent upstream on the DU pin and received downstream on the DD pin every 125 µs. Each frame consists of eight 4-byte GCI packets that contain voice and control information for 8 channels. The overall structure of the GCI frame is shown in Figure 7.

The 4-time slot GCI packets contain the following:

- Two voice-data channels
  - B1 provides compressed PCM data for the Voice Channel
  - B2 is unused
- One Monitor (M) channel for reading and writing control data and coefficients to the chip set in combination with the MX and MR bits in the Signaling and Control channel
- One Signaling and Control (SC) channel containing a 6-bit Command/Indicate (C/I) field for real time control information and a two-bit field with Monitor Receive and Monitor Transmit (MR and MX) bits for handshaking functions linked to the Monitor channel. All principal signaling (real-time critical) information is carried on the C/I channel

Figure 7. Multiplexed GCI Time Slot Structure



In the packet control block (shown in Figure 8), the Frame Sync (FSC) pulse identifies the beginning of the Transmit and Receive frames and all GCI packets are referenced to it. Voice (B1), C/I, and Monitor data are sent to the Upstream Multiplexer where they are combined and serially shifted out of the DU pin in the selected GCI packet time slots. The Downstream Demultiplexer uses the same packet control block information to demultiplex the incoming GCI packet into separate voice (B1), C/I, and Monitor channels.

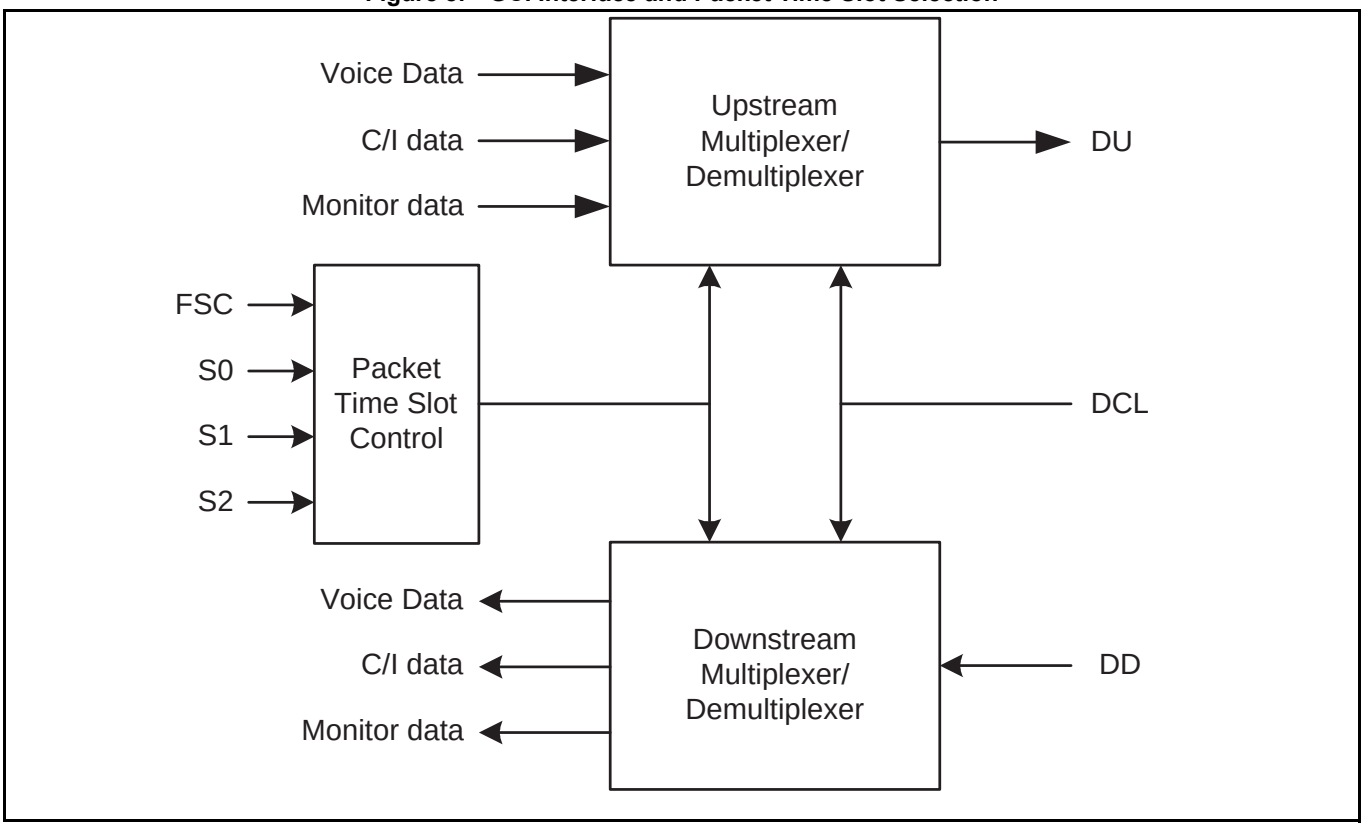
The external clock applied to the DCL pin must be either 2.048 MHz or 4.096 MHz. The Le88010 device determines the incoming clock frequency and adjusts internal timing automatically to accommodate single or double clock rates. Correct clock detection can be determined by reading the CSEL bits in *46/47h Write/Read Device Configuration Register*, on page 49. Upstream and Downstream Data is always transmitted at a 2.048 MHz data rate.

The Le88010 device supports access to all eight GCI packets (8 analog channels). The S0, S1 and S2 GCI Packet Assignment pins on the Le88010 device are encoded as shown in Table 3.

Table 3. GCI Packet Assignment Codes

$\overline{\text{INT}}$/S2	DIN/S1	DCLK/S0	GCI Packet
DGND	DGND	DGND	0
DGND	DGND	DVDD	1
DGND	DVDD	DGND	2
DGND	DVDD	DVDD	3
DVDD	DGND	DGND	4
DVDD	DGND	DVDD	5
DVDD	DVDD	DGND	6
DVDD	DVDD	DVDD	7

Figure 8. GCI Interface and Packet Time Slot Selection



Signaling and Control (SC)

The downstream and upstream SC channels are continuously sending state control and loop supervision data every frame to and from the Le88010 device in the C/I field. This allows the upstream processor to have immediate access to the VoicePort line status.

The MR and MX bits are used for handshaking during data exchange on the monitor channel.

The format of the downstream control (C) field is shown in Table 4. The Le88010 device receives the most significant bit first.

Table 4. Down Stream SC Channel Definition

D7	D6	D5	D4	D3	D2	D1	D0
0	IO3	IO2	IO1	SS1	SS0	MR	MX

SS1-SS0: System State

00: Shutdown
01: Idle (Supervision enabled, Codec deactivated)
10: Active. (Supervision enabled, Codec activated)
11: Shutdown

See *56/57h Write/Read System State*, on page 53 for more description of the system states.

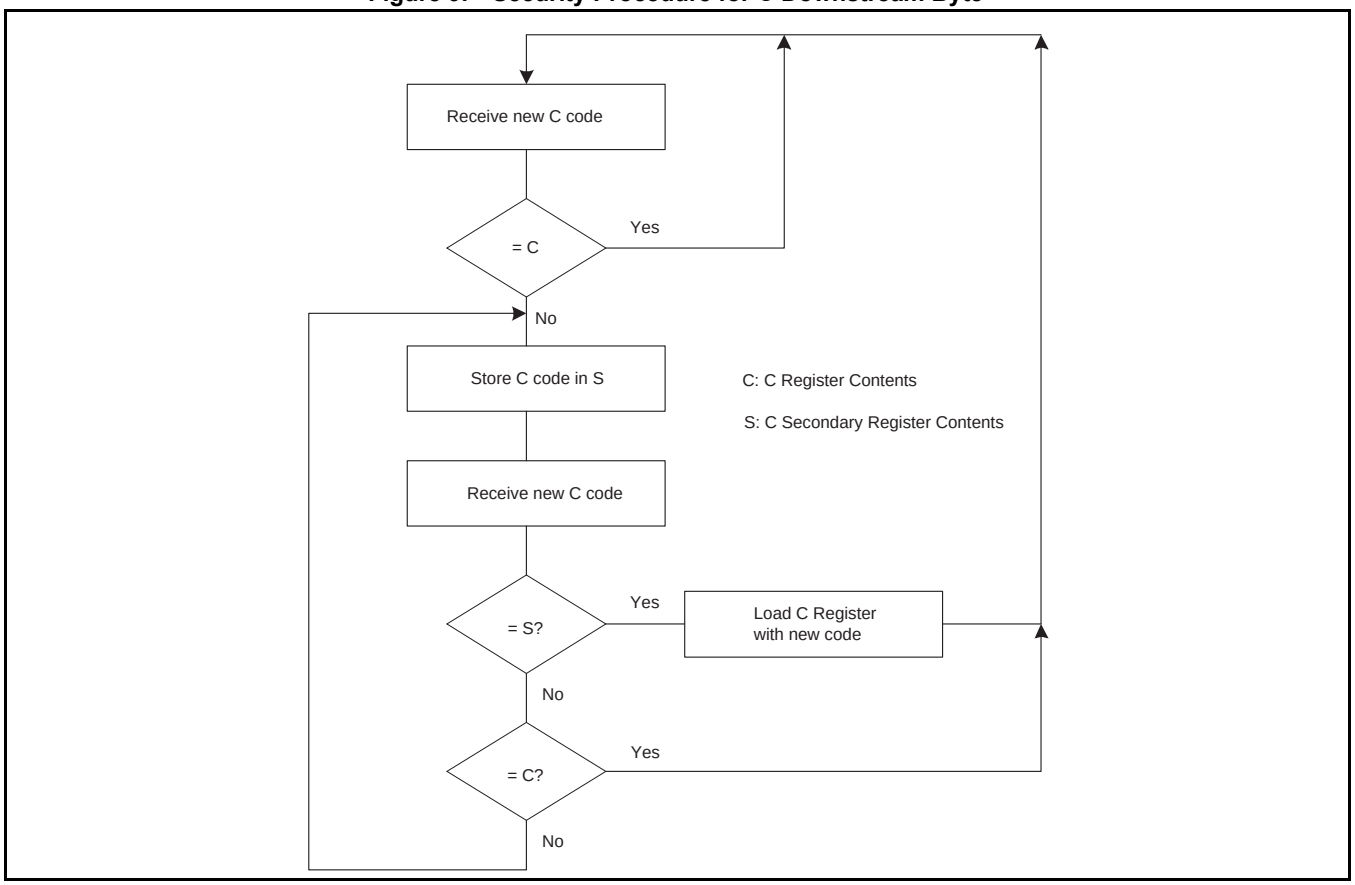
IO1 - IO3: I/O pin output latch bits

See *54/55h Write/Read Input/Output Direction Register*, on page 53 for configuring these pins as outputs and available output configurations.

Figure 9 shows a flow chart describing the transmission protocol for the downstream channel, which provides a high level of security for the C field data exchange. Whenever the received pattern of C bits 6 through 1 is different from the pattern currently in the C input register, the new pattern is loaded into a secondary C register, and a latch is set. When the next pattern is received (in the following frame) while the latch is set, the following rules apply:

- If the received pattern corresponds to the pattern in the secondary register, the new pattern is loaded into the C register, and the latch is reset.
- If the received pattern is different from the pattern in the secondary register and different from the pattern currently in the C register, the newly received pattern is loaded into the secondary C register, and the latch remains set.
- If the received pattern is the same as the pattern currently in the C register, the C register is unchanged, and the latch is reset.

Figure 9. Security Procedure for C Downstream Byte



The format of the upstream indication (I) field is shown in Table 5. The Le88010 device transmits the I field most significant bit first each frame.

Table 5. Upstream SC Channel

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	SLCX	RNGDT	LIU	MR	MX

SLCX — Summary output of the Signaling Register

- 1: One or more of the unmasked bits in the Signaling Register has toggled.
- 0: None of the unmasked bits in the Signaling Register has toggled. This is a logic “or” of POH, CFAIL, IO2, CAD, DIS, POL, RNGDT and LIU. This bit is reset when command 4Fh read and clear interrupt from the *4D/4Fh Read Signaling Register*, on page 50 is issued

RNGDT: — Ringing Detect

- 0: RInging not detected
- 1: Ringing Detected

LIU: — Line in Use (Significant when on hook)

- 0: Line not in use (line voltage greater than TLIU threshold for longer than DLIU)
- 1: Line in use (line voltage less than the TLIU threshold for longer than DLIU)

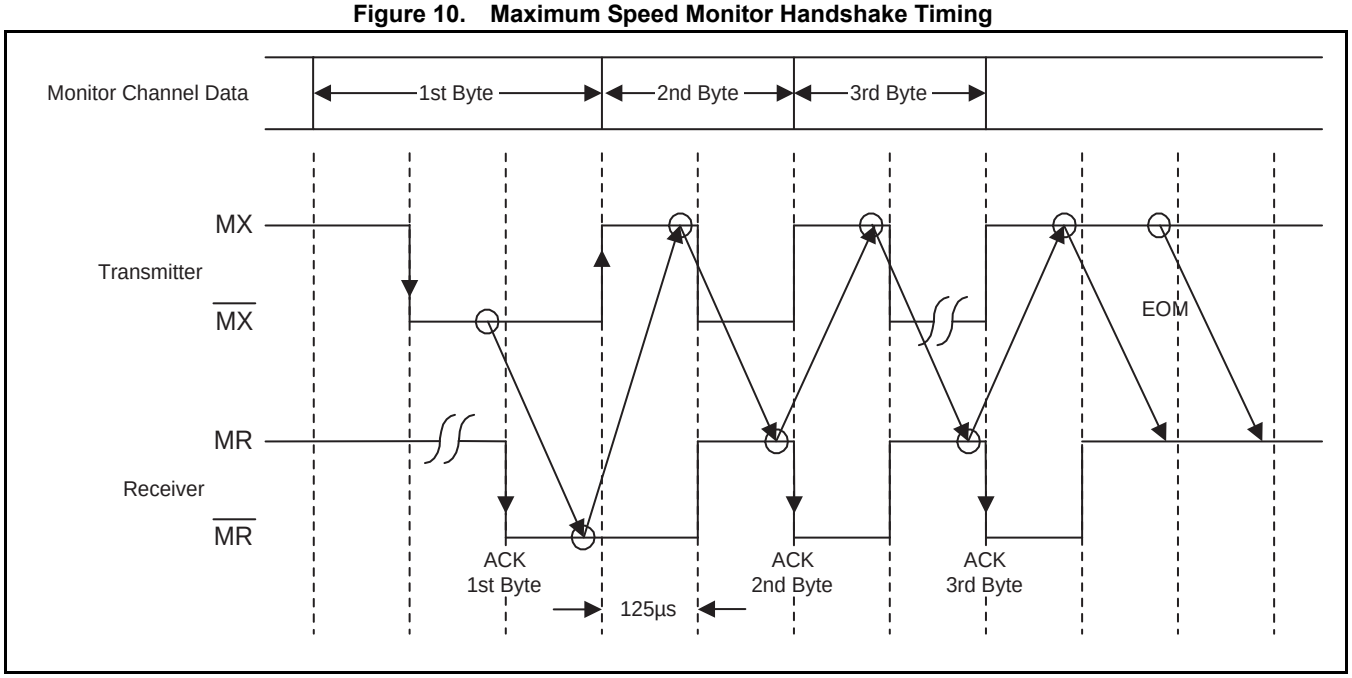
Data from the loop supervision circuitry (with applicable debouncing) is latched by a derivative of Frame Sync every 125 µs. This real-time latched data is transmitted upstream in the I field every frame (125 µs). Note that it is not the data in the Signaling Register. Hence masking or unmasking of the RNGDT and LIU interrupts in the interrupt mask register will not affect the RNGDT and LIU data in the SC channel.

Monitor Channel Protocol

The Monitor (M) channel (see Figure 10) loads the Le88010 device internal device registers, reads the status of the device and the contents of the internal registers, and provides supplementary signaling. Information is transferred on the Monitor Channel using the MR and MX bits of the third (SC) channel to provide a reliable method of data exchange between the higher level processor and the Le88010 device (see Figure 10).

The monitor channel is the third channel in the 4-channel packet sent and received every 125 µs. A monitor command consists of one address byte and one or more command bytes followed by additional bytes of input data. The command can be followed by the Le88010 device sending data bytes upstream via the DU pin.

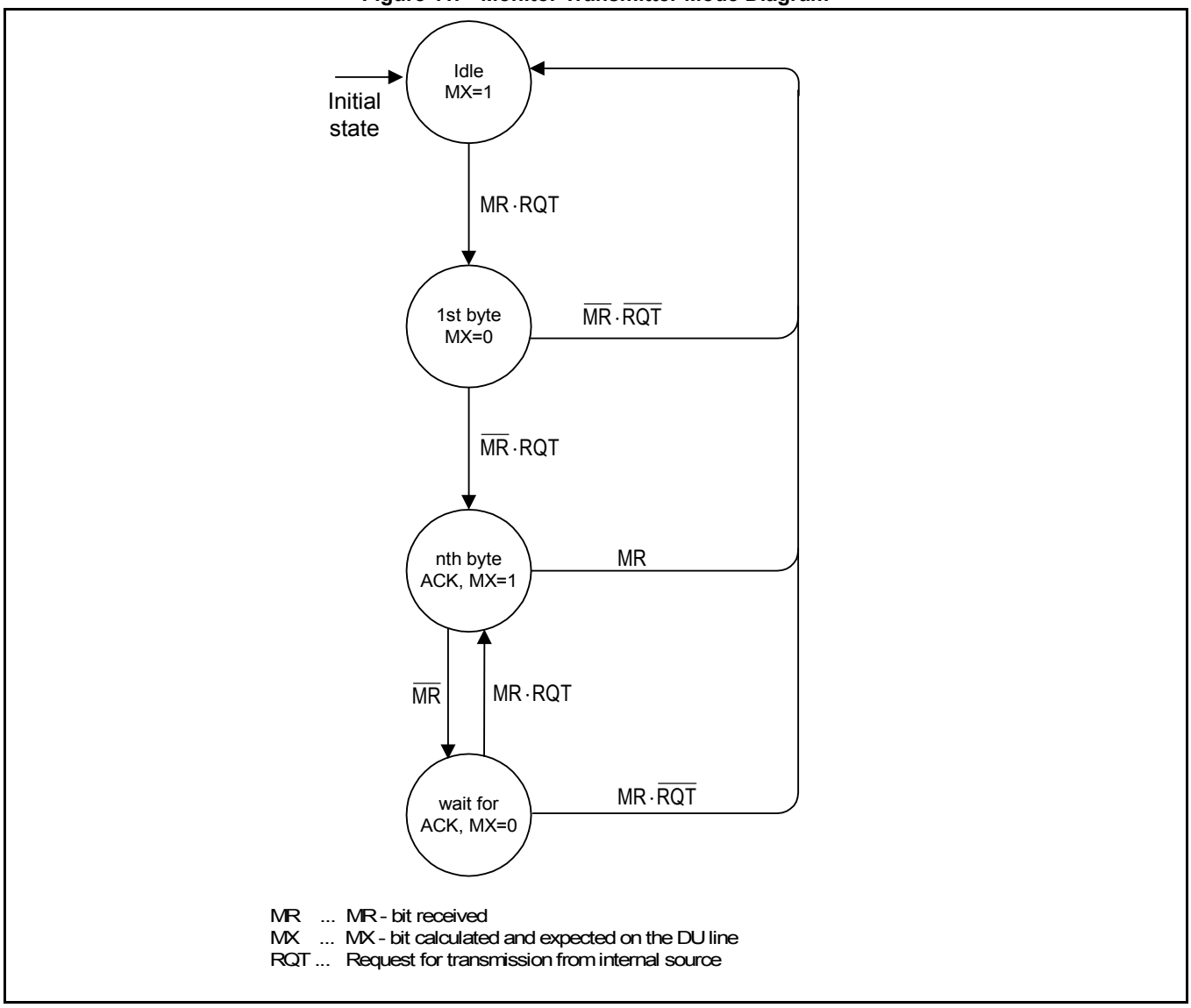
Figure 10. Maximum Speed Monitor Handshake Timing



- An inactive (High) MX and MR pair bit for two or more consecutive frames shows an idle state on the monitor channel and the end of message (EOM).
- Figure 10 shows that transmission is initiated by the transition of the transmitter MX bit from the inactive to the active state. The transition coincides with the beginning of the first byte sent on the monitor channel. The receiver acknowledges the first byte by setting MR bit to active and keeping it active for at least one more frame.
- The same data must be received in two consecutive frames in order to be accepted by the receiver.
- The same byte is sent in each of the succeeding frames until either a new byte is transmitted, the message ends, or an abort occurs. Any abort command resets any pending commands in the Le88010 device. The device remains in the previous configuration and is ready to receive a new command.
- Any false MX or MR bit received by the receiver or transmitter leads to a request-for-abort or an abort, respectively.
- To obtain maximum data transfer speed, the transmitter anticipates the falling edge of the receiver's acknowledgment as shown in Figure 10.

Figure 11 and Figure 12 are state diagrams that define the operation of the monitor transmitter and receiver sections in the Le88010 device.

Figure 11. Monitor Transmitter Mode Diagram



Programming with the Monitor Channel

The Le88010 device uses the monitor channel for the transfer of status or mode information to and from higher level processors. The higher level processor is synchronized to the Le88010 device using the time slot straps S0 and S1.

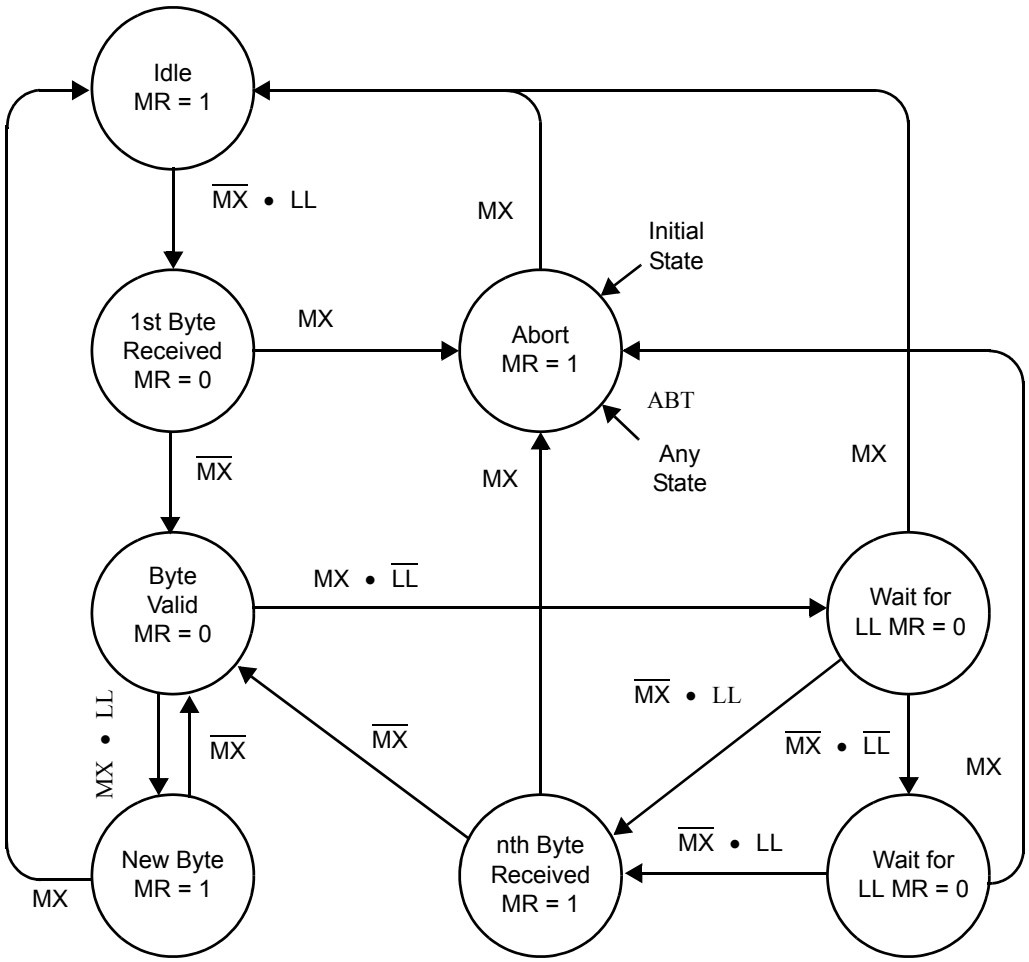
The messages transmitted in the monitor channel have different structures. The first byte of monitor channel data in the GCI format indicates the address of the device either sending or receiving the data. All monitor channel messages to/from the Le88010 device begin with this address byte:

Bit	7	6	5	4	3	2	1	0
Address	1	0	0	0	0	0	0	C

C

0: Address for channel identification command
1: Address for all other commands

Figure 12. Monitor Receiver Mode Diagram



Transmission in the GCI monitor channel starts with an address byte followed by a command byte. If the command byte specifies a write, from 1 to 14 additional data bytes can follow (see Table 6). If the command byte specifies a read, additional data bytes can follow. The Le88010 device responds to the read command by sending out the original address byte and up to 14 bytes upstream that contain the information requested by the upstream controller. Generic byte transmission sequence over the GCI monitor channel is shown in Table 6.

Table 6. Monitor Byte Transmission Sequence

GCI Monitor Channel	
Downstream	**Upstream**
ADDRESS Control byte, write Data byte 1* • Data byte m* ADDRESS Control byte, read m ≤ 14	 Data byte 1 • Data Byte n n ≤ 14

Channel Identification Command (CIC)

When the monitor channel address byte is 80H, a command of 00H is interpreted by the Le88010 device as a two-byte Channel Identification Command (CIC).

The format for this command is shown next.:

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Address Byte	1	0	0	0	0	0	0	0
Command Byte	0	0	0	0	0	0	0	0

Immediately after the last bit of the CIC command is received, the Le88010 device responds with the two-byte channel ID code indicating an analog transceiver device type in bits 6 and 7 of byte 2, with the following configuration options.:

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Byte 1	1	0	0	0	PCN4	PCN3	PCN2	PCN1
Byte 2	1	0	0	0	0	1	1	0

PCN[4:1] Product Code Number

06h Le88010 device

When the Le88010 device has completed transmission of the channel ID information, it sends an EOM (MX = 1 for two successive frames) on the upstream C/I channel. The Le88010 device also expects an EOM to be received on the downstream C/I channel before any further message sequences are received.

Input / Output Block

This block controls general-purpose pins that can be configured by the user as inputs, outputs, or relay drivers. Six CMOS-compatible I/O pins (I/O1 through I/O6) are provided. I/O1 can act either as a standard digital input, as a CMOS output, or can be configured as a 5-V tolerant open drain relay driver. When configured as such, it is capable of directly driving a 150-mW 3-V or 5-V relay and has an integrated catch circuit. I/O1 is normally used to control on- or off-hook status in the DAA. I/O2 - I/O6 are standard 3.3 V digital I/O pins. I/O2 can also generate an interrupt when configured as an input and the input state changes. When operated as an input, I/O4 can be routed to the supervisory period discriminator under MPI selection to perform ring detection on an externally generated ringing indication. All I/O pins can be accessed using Command *52/53h Write/Read Input/Output Data Register,* on page 52. The direction of the I/O pins (input or output) and output type is specified by programming *54/55h Write/Read Input/Output Direction Register,* on page 53.

Voice Signal Processor

This block performs digital signal processing for the transmission and reception of voice. It includes G.711 compression/ decompression, filtering, gain scaling and DTMF generation. This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

All programmable digital filter coefficients can be calculated using the Microsemi WinSLAC™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

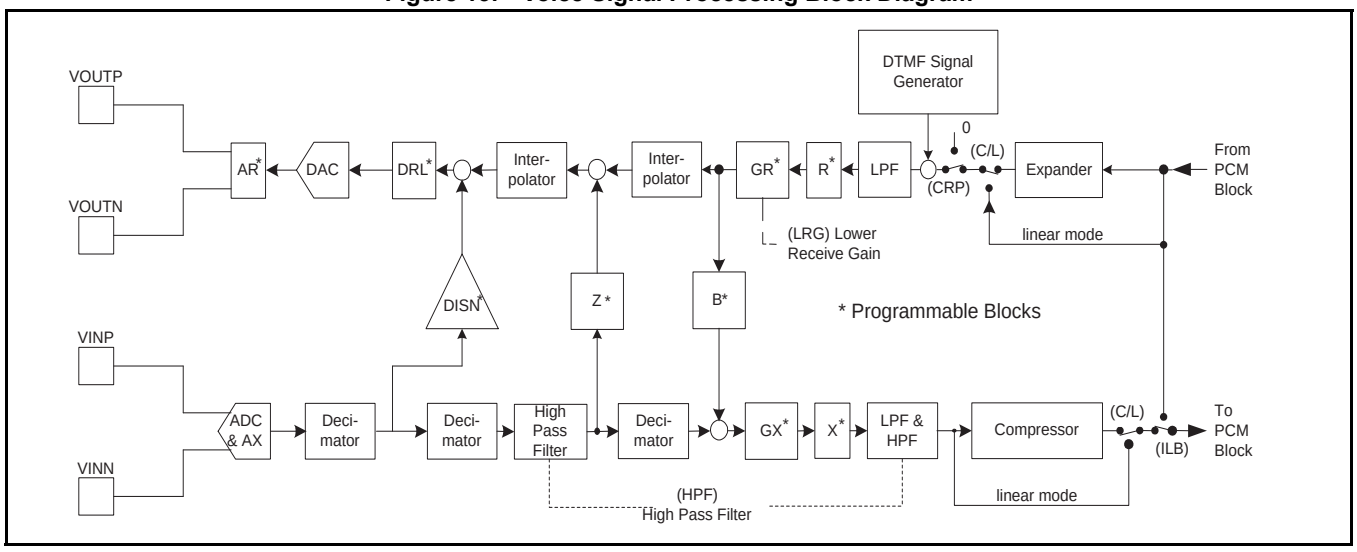
Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the Le88010 device for the system. Figure 13 shows the Le88010 device signal processing and indicates the programmable blocks and how this section interfaces with the high voltage line driver and line sensing circuits.

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance
- Flexibility

Figure 13. Voice Signal Processing Block Diagram



Two-Wire Impedance Matching

Two feedback paths in the voice signal processor can modify the two-wire input impedance presented by the attached phone line interface (DAA) by providing a programmable feedback path from the A/D path input (VINP - VINM) to the D/A path output (VOUTP - VOUTM).

The DISN path is comprised of the voice A/D and its first stage of decimation, a Digital Impedance Scaling Network (DISN), and the voice DAC. The 8-bit DISN synthesizes a portion of the ac impedance and is used to modify the impedance set by the external line interface network. See *CA/CBh Write/Read Digital Impedance Scaling Network (DISN)*, on page 63.

The Z filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. The DISN and Z-Filter enable the user to synthesize virtually all required telephony device input impedances. See *98/99h Write/Read Z Filter FIR Coefficients*, on page 60. and *9A/9Bh Write/Read Z Filter IIR Coefficients*, on page 60.

Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the D/A (R) and A/D (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter. See *8A/8Bh Write/Read R Filter Coefficients*, on page 59. and *88/89h Write/Read X Filter Coefficients*, on page 58

Transhybrid Balancing

The voice signal processor's programmable B filter is used to adjust transhybrid balance The filter has a single pole IIR section (BIIR) and an eight-tap FIR section (BFIR), both operating at 16 kHz. See *86/87h Write/Read B Filter FIR Coefficients*, on page 57. and *96/97h Write/Read B Filter IIR Coefficients*, on page 60

Gain Adjustment

The transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. See *50/51h Write/Read Voice Path Gains*, on page 52. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. See *80/81h Write/Read GX Filter Coefficients*, on page 56.

The receive path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. See *82/83h Write/Read GR Filter Coefficients*, on page 57. DRL is a digital loss block of 0 dB or 6.02dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. See *50/51h Write/Read Voice Path Gains*, on page 52.This provides a net loss in the range of 0 to 18 dB.

Transmit Signal Processing

In the transmit path (A/D), the AC analog input signal is sensed by the VINP and VINN pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or µ-law), and made available to the PCM block. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections with coefficients stored in the coefficient RAM. The B, X, and GX filters can also be operated from an alternate set of default coefficients stored in ROM. See *60/61h Write/Read Operating Functions*, on page 54. In the transmit path, with default coefficients, the coded transmit PCM signal is in phase with the analog signal measured from VINP to VINN.

The high-pass filter rejects low frequencies such as 50 Hz or 60 Hz, and may be disabled.

Receive Signal Processing

In the receive path (D/A), the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto the VOUTP and VOUTN pins. The DRL, DISN, Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM, while AR is an analog amplifier. The Z, R, and GR filters can also be operated from an alternate set of default coefficients stored in ROM. See *60/61h Write/Read Operating Functions*, on page 54. In the receive path, with default coefficients, the analog signal measured from VOUTP to VOUTN is in phase with the coded receive PCM signal.

Programmable Filters

The filter coefficients that the user sends to the voice ALU are in a form known as Canonical Signed Digits (CSDs). The coefficients take the following general form:

$$h = I0 + C1 \bullet 2^{-m1} \bullet (1 + C2 \bullet 2^{-m2} \bullet (1 + I3 \bullet C3 \bullet \ (2^{-m3} \bullet (1 + I4 \bullet C4 \bullet 2^{-m4}))))$$

where: cj = –1 or +1 (represented as 1 or 0 in user programming)

mj = 0, 1, 2,... or 7 (user programming)

I0 = 1 for GX; I0 = 0 for all other coefficients

I4 = 1 for 4 • CSD coefficients; I4 = 0 otherwise

I3 = 1 for 3 and 4 CSD coefficients; I3 = 0 for 2 CSD coefficients

Calculating Coefficients with WinSLAC™ Software

The WinSLAC™ software is a program that models the Le88010 device, the line conditions, and the external phone line interface (DAA) components to calculate the coefficients of the programmable filters and predict important transmission performance plots.

The following parameters relating to the desired line conditions and the external components are provided as input to the program:

- Line impedance or the balance impedance of the line is specified by the local telephone system.
- Desired two-wire impedance that is to appear at the line card terminals of the exchange.

- Tabular data for templates describing the frequency response or attenuation distortion limits of the design.
- Relative analog signal levels for both the transmit and receive two-wire signals.
- Component values for the AC model of the external Phone Line Interface or DAA circuit.
- Two-wire return loss template that is usually specified by the local telephone system.
- Four-wire return loss template that is usually specified by the local telephone system.

The output from the WinSLAC program includes the coefficients of the AR, AX, DRL, DISN, GR, GX, Z, R, X, and B filters as well as transmission performance plots of stability, input impedance, two-wire return loss, receive and transmit path frequency responses, and four-wire return loss.

The coefficients are formatted in a way that allows easy integration with the VoicePath™ API software or VP Script demonstration software.

Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in ITU-T Recommendation G.711. A-law or µ-law operation is programmed using command *60/61h Write/Read Operating Functions*, on page 54. Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Linear code is also selected using Command 60/61h. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

VoicePath™ Test States and Operating Conditions

The Le88010 device supports testing by providing test states and special operating conditions as shown in Figure 13, on page 19 (see *70/71h Write/Read Operating Conditions*, on page 55).

Cutoff Transmit Path (CTP): When CTP = 1, DXA is High impedance and the transmit time slot does not exist. This state takes precedence over the Interface Loopback (ILB).

Cutoff Receive Path (CRP): When CRP = 1, the receive signal is forced to 0 just ahead of the low pass filter (LPF) block. This state blocks the 1 kHz receive tone (TON). The signal generators can still be used to send signals in the receive path.

High Pass Filter disable (HPF): When HPF = 1, all of the high pass and notch filters in the transmit and receive paths are disabled.

Lower Receive Gain (LRG): When LRG = 1, an extra 6.02 dB of digital loss is inserted into the receive path.

Interface Loopback (ILB): When ILB = 1, data from the TSA receive time slot is looped back to the TSA transmit time slot. Any other data in the transmit path is overwritten.

1 kHz Receive Tone (TON): When TON = 1, a 1 kHz digital mW is injected into the receive path, replacing any receive signal from the TSA.

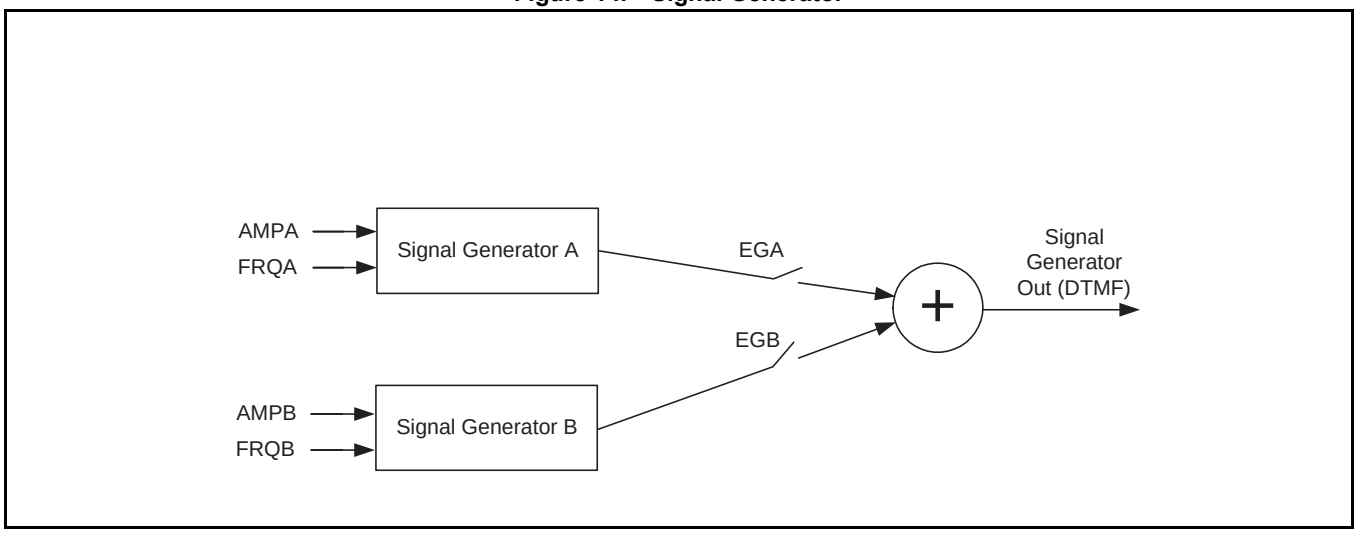
DTMF Signal Generation

Two digital signal generators are available (see Figure 14) that are summed into the receive path, as shown in Figure 13. They are configured with commands *D2/D3h Write/Read Signal Generator A and B Parameters*, on page 64 and controlled with command *DE/DFh Write/Read Signal Generator Control*, on page 65 in combination with the cadencer configuration in *E0/E1h Write/Read Cadence Timer*, on page 66.

Signal generators A and B are typically used for DTMF generation.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system. The amplitude accuracy and spectral purity are limited only by the voice DAC.

Figure 14. Signal Generator



Supervision Processing

The Le88010 device has three main system states.

Shutdown

Shutdown is the power-up and hardware reset state of the device. The voice codec is disabled and all supervision is disabled.

Idle (Supervision Enabled, Codec deactivated)

Supervision enabled. To reduce power dissipation, voice transmission is disabled but supervision circuitry is enabled.

Active (Supervision Enabled, Codec activated)

The Active state is used for on-hook or off-hook transmission, or measurement. Both the voice codec and the supervision circuits are enabled. On and Off hook control is provided by the IO1 output.

In the Idle or Active states, the following supervision functions are supported based on the currents sensed at the TDC and RDC pins through the RST and RSR sense resistors. All of the detector thresholds are defined in terms of the voltage at the TIP / RING side of the sense resistors.

Polarity of Line Voltage Detection

The Polarity of line voltage (POL) bit is found in command *4D/4Fh Read Signaling Register*, on page 50. POL = 0 indicates the line voltage polarity is Normal (Tip more positive than Ring). POL = 1 indicates the line voltage polarity is Reversed (Ring more positive than Tip). An interrupt is generated by transitions of the POL bit if MPOL is reset in *6C/6Dh Write/Read Interrupt Mask Register*, on page 55. The TDIS threshold in command *C2/C3h Write/Read Loop Supervision Parameters*, on page 62 defines the magnitude that the line voltage must exceed in the opposite polarity before a change in polarity will be indicated.

Parallel Phone Off-hook Detection

The Parallel phone Off-Hook detector bit (POH) in command *4D/4Fh Read Signaling Register*, on page 50 is used to detect the disturbance in the line caused by a parallel phone going off hook while the Le88010 device is off-hook on the same line. In this case, a transient is created on the line as the metallic voltage decreases due to the lower resistance. A current, proportional to the metallic line voltage (sensed by pins TDC and RDC), is fed out of the ITR pin. An external RC network connected to ITR responds to a sudden line voltage change by applying a pulse to LTP, the line transient pulse input pin. A line transient causes a comparator in the Le88010 to output a POH pulse. As this signal reports a transient event, for these events to be reliably reported, the MPOH bit in *6C/6Dh Write/Read Interrupt Mask Register*, on page 55 should be unmasked to ensure these events are latched in the signaling register. A POH event is only reported if the Le88010 is already in the off-hook state (IO1 bit is high). Note that a polarity reversal while off hook will also generate a POH event.

Line Disconnect Detection

The line Disconnected (DIS) bit in command *4D/4Fh Read Signaling Register*, on page 50 provides an indication that the line has DC feed present. DIS = 0 indicates the line has DC feed present (Line voltage greater than the TDIS threshold for longer than DDIS). DIS = 1 indicates the line has DC feed removed or is disconnected (Line voltage less than the TDIS threshold for longer than DDIS). The TDIS threshold and the DDIS debounce period are programmed in command *C2/C3h Write/Read Loop Supervision Parameters*, on page 62. The default debounce period is designed to avoid disconnected indications during polarity

reversal or incoming ringing. An interrupt is generated if MDIS is unmasked (reset) in the *6C/6Dh Write/Read Interrupt Mask Register,* on page 55 when this event occurs.

Line-In-Use Detection

The Line-In-Use detector bit (LIU) in command *4D/4Fh Read Signaling Register,* on page 50, monitors the absolute value of the tip to ring voltage, as sensed by TDC and RDC. LIU = 0 indicates the line is not in use (Line voltage greater than the TLIU threshold for longer than DLIU). LIU = 1 indicates the line is in use (Line voltage less than the TLIU threshold for longer than DLIU). When LIU = 0 the line can be seized to make an outgoing call, when LIU = 1 the line is not available for seizure. The TLIU detection threshold and DLIU debounce period are programmed in command *C2/C3h Write/Read Loop Supervision Parameters,* on page 62. An interrupt is generated if MLIU is unmasked (reset) in the *6C/6Dh Write/Read Interrupt Mask Register,* on page 55 when the line voltage crosses the threshold for longer than the debounce period. Line in use will also be indicated when the Le88010 device is off-hook.

Ringing Presence Detector

The Ringing presence Detect bit, RNGDT, in command *4D/4Fh Read Signaling Register,* on page 50, detects the ringing envelope and includes programmable ringing frequency and amplitude discrimination. RNGDT = 0 indicates ringing is not present (Average line voltage is less than TLIU or line frequency outside the programmed TMINP to TMAXP range). RNGDT = 1 indicates that a ringing signal is present (Average line voltage is greater than TLIU and line frequency within the programmed TMINP to TMAXP range). Due to the period discrimination, the RNGDT bit follows the cadence of ringing delayed by approximately two ringing frequency cycles.

This period detector is configured by setting the TMINP and TMAXP fields in command *C2/C3h Write/Read Loop Supervision Parameters,* on page 62. Only AC Tip to Ring signals going above and below zero volts by more than the value set in TDIS will have their period examined. Typical settings for TDIS reject audio and metering signals on the loop. The period discrimination rejects mains interference and dial pulse signals from potentially causing false ringing indication.

The Line-In-Use detector threshold TLIU can be used to qualify ringing waveforms to have sufficient amplitude to be valid ringing signals by the ringing detect bit or it can be set to a low value to permit any valid ringing frequency to be valid ringing. The TLIU is normally set to a low threshold for ringing detection to permit ringing cadence monitoring.

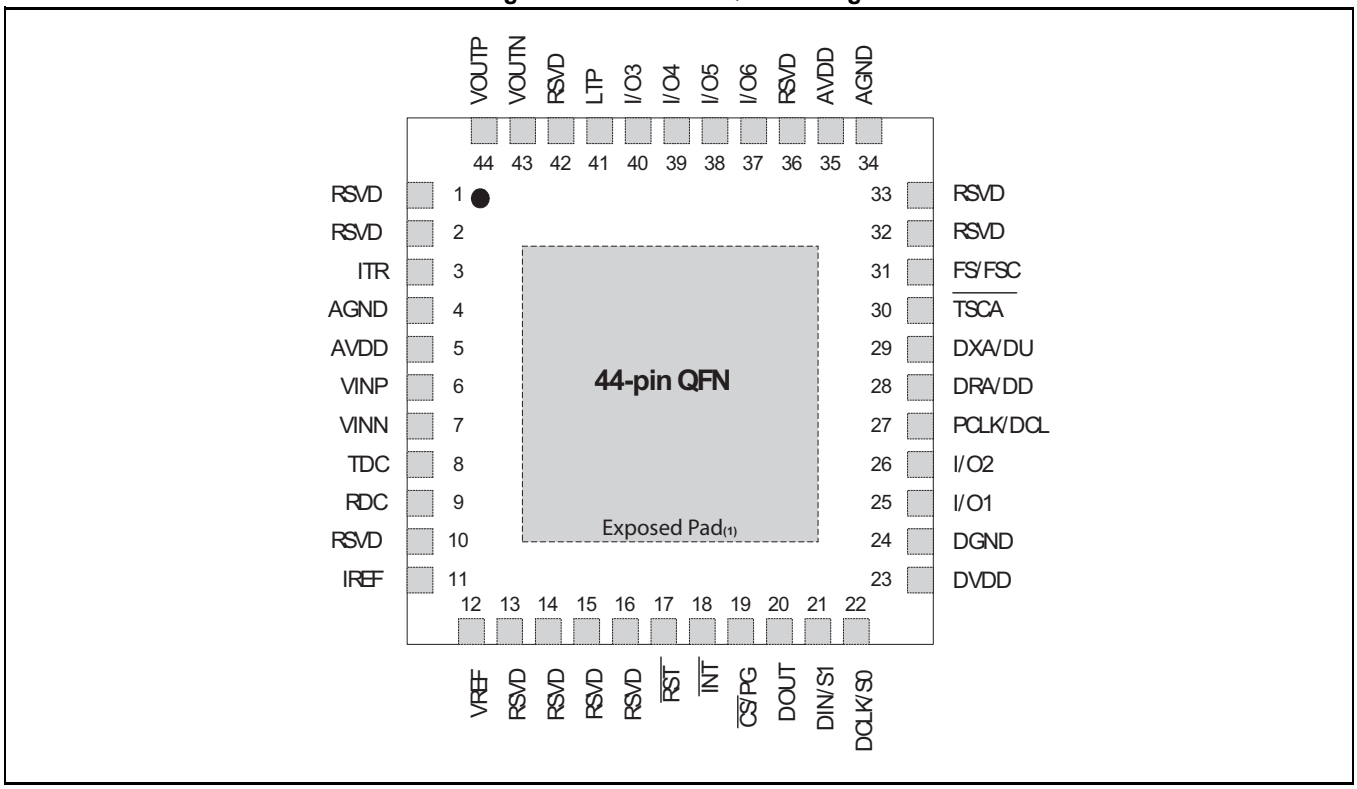
An interrupt is generated if MRNGDT is unmasked (reset) in the *6C/6Dh Write/Read Interrupt Mask Register,* on page 55. RNGDT interrupts occur when ringing starts and again when ringing ends.

Analog Reference Circuits

The analog reference circuit generates a reference voltage and reference current for use by internal circuits. The reference current is generated through the external resistor RREF and the external capacitor, CREF, provides filtering on the reference voltage.

CONNECTION DIAGRAMS

Figure 15. Le88010 QFN Package



Notes:

1. *The exposed pad is at ground potential. Care should be taken to avoid any electrical contact between the exposed pad and any traces on the printed circuit board other than analog ground.*

PIN DESCRIPTIONS

NAME	Type	Description
AVDD/ DVDD	Power	Analog and digital power supply inputs. AVDD and DVDD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board.
AGND/ DGND	Power	Separate analog and digital grounds are provided to allow noise isolation; however, the grounds are connected inside the part, and must also be connected together on the circuit board.
$\overline{CS}$/PG	Input	Chip Select/PCM-GCI. The $\overline{CS}$/PG input along with the DCLK/S0 input are used to determine the operating state of the programmable PCM/GCI interface. On power up, the device will initialize to GCI mode if $\overline{CS}$/PG is low *and* there is no toggling (no high to low or low to high transitions) of the DCLK/S0 input. The device will initialize to the PCM/MPI mode if either $\overline{CS}$ is high *or* DCLK is toggling. Once the device is in PCM/MPI mode, it is ready to receive commands through its serial interface pins, DIN, DOUT and DCLK. Once a valid command has been sent through the MPI serial interface, GCI mode cannot be entered unless a hardware reset is asserted or power is removed from the part. If a valid command has not been sent since the last hardware reset or power up, then GCI mode can be re-entered (after a delay of one PCM frame) by holding $\overline{CS}$/PG low and keeping DCLK static. While the part is in GCI mode, $\overline{CS}$/PG going high or DCLK toggling will immediately place the device in PCM/MPI mode. In the PCM/MPI mode, the Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The device coefficient registers selected by the write or read command must be enabled by writing a 1 to the EC bit in the Channel Enable Register. See the Channel Enable Register and Command 4A/4Bh for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High.
DCLK/S0	Input	Data Clock. In addition to providing both a data clock input and an S0 GCI address input, DCLK/S0 acts in conjunction with $\overline{CS}$/PG to determine the operational mode of the system interface, PCM/MPI or GCI. See $\overline{CS}$/PG for details. In the PCM/MPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the device. The maximum clock rate is 8.192 MHz.
	Input	Select Bit 0. In GCI mode, S0 is one of two inputs (S0, S1) that is decoded to determine on which GCI channel the device transmits and receives data.
DIN/S1	Input	Data Input. In the PCM/MPI mode, control data is serially written into the device via the DIN pin, most significant bit first. The Data Clock determines the data rate.
	Input	Select Bit 1. In GCI mode, S1 is the second of two inputs (S0, S1) that is decoded to determine on which GCI channel the device transmits and receives data.
DOUT	Output	Data Output. Control data is serially written from the device via the DOUT pin, most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted, which allows DIN and DOUT to be directly tied together in systems which use a single line for data input and output.
DRA/DD	Input	PCM Data Receive. In the PCM/MPI mode, the PCM data is serially received on the DRA port during the user-programmed time slot. Data is always received with the most significant bit first. For compressed signals, 1 byte of data is received every 125 µs at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 µs at the PCLK rate.
	Input	GCI Data Downstream. In GCI mode, the B1, B2, Monitor and SC channel data is serially received on the DD input. The device requires one of the eight GCI channels for operation. Which of 4 GCI Channels (out of the eight possible), is determined by the S0 and S1 inputs. Data is always received with the most significant bit first. 4 bytes of data is received every 125 µs at the 2.048 Mbit/s data rate.

NAME	Type	Description (Continued)
DXA/DU	Outputs	PCM Data Transmit. In the PCM/MPI mode, the transmit data is sent serially out on the DXA port during the user-programmed time slot. Data is always transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling mode) bursts at the PCLK rate. DXA is high impedance between time slots, while the device is in the Inactive mode with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on.
	Output	GCI Data Upstream. In the GCI mode, the B1, B2, Monitor and SC channel data is serially transmitted on the DU output. Which GCI channel the device uses is determined by the S0 and S1 inputs. Data is always transmitted with the most significant bit first. 4 bytes of data is transmitted every 125 µs at the 2.048 Mbit/s data rate.
EPAD	Power	Exposed pad substrate connection. This pad is at ground potential and, because of the low device power dissipation, need not be soldered to external circuit board clad.
FS/FSC	Input	Frame Sync. In the PCM/MPI mode, the Frame Sync (FS) pulse is an 8 kHz signal that identifies Time Slot 0 and Clock Slot 0 of a system's PCM frame. Individual time slots are referenced to this input, which must be synchronized to PCLK.
	Input	Frame Sync. In GCI mode, the Frame Sync (FSC) pulse is an 8 kHz signal that identifies the beginning of GCI channel 0 of a system's GCI frame. The device can access channels 0 to 3 based on the setting of the S0, S1 inputs. FSC must be synchronized to DCL.
I/O1	I/O	General purpose digital Input/Output (Can directly drive a 150 mW 3-V or 5-V relay)
I/O2, I/O3, I/O4, I/O5 I/O6	I/O	Low power, general purpose digital Input/Output
$\overline{INT}$	Output	Interrupt. $\overline{INT}$ is an active Low output signal, which is programmable as either 3V CMOS-compatible or open drain. The $\overline{INT}$ output goes Low any time one of the input bits in the Real Time Data register changes state and is not masked. It also goes Low any time new transmit data appears if this interrupt (ATI) is armed. $\overline{INT}$ normally remains Low until the appropriate register is read via the microprocessor interface unless ATI is set, or the device receives either a software or hardware reset. The individual bits in the Real Time Data register can be masked from causing an interrupt by using MPI Command 6C/6Dh.
IREF	Input	Current Reference. An external resistor R_{REF} connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip.
ITR	Output	Tip-Ring sense. Outputs a current proportional to the difference between currents flowing into TDC and RDC. Feeds LTP via an external R-C network.
LTP	Input	Line transient pulse input. A pulse indicating a step change in tip-ring line voltage feeds this pin. An external R-C differentiation network connects from the ITR pin to this pin.
PCLK/DCL	Input	PCM Clock. The PCM clock determines the rate at which data is serially shifted in and out on the PCM highway and provides the clock reference for the internal PLL
	Input	GCI Data Clock. In GCI mode, DCL is either 2.028 MHz or 4.096 MHz and an integer multiple of the FSC frequency. The internal PLL is automatically configured to run from this clock in GCI mode
RDC	Input	Ring lead DC Sense. A resistor is connected from this pin to the Ring lead.
$\overline{RST}$	Input	Device Hardware Reset. A logic Low signal at this pin resets the device to its default state.
RSVD	Open	Reserved. Make no connection to this pin.
TDC	Input	Tip lead DC Sense. A resistor is connected from this pin to the Ring lead.
VINN	Input	Negative AC voice signal sense input.
VINP	Input	Positive AC voice signal sense input.

NAME	Type	Description (Continued)
VOUTN	Output	Voice D/A channel negative AC voltage output
VOUTP	Output	Voice D/A channel positive AC voltage output
VREF	Output	Analog Voltage Reference. The VREF output is provided in order for an external capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF and the output resistance are given in *Electrical Characteristics*, on page 28.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Storage Temperature	–55° C < T_A < +125° C
Ambient Temperature, under Bias	–40° C < T_A < +85° C
Ambient relative humidity (non condensing)	5 to 95%
DGND with respect to AGND	-0.4 V to +0.4 V
AVDD with respect to AGND	–0.4 V to + 4.0 V
AVDD with respect to DVDD	–0.4 V to + 4.0 V
DVDD with respect to DGND	–0.4 V to + 4.0 V
AGND with respect to DGND	–0.05 V to + 0.05 V
Digital pins with respect to DGND	–0.4 V to the smaller of +4.0 V or DVDD + 0.4 V
I/O1 with respect to DGND	–0.4 V to the smaller of +5.5 V or DVDD + 2.37 V
I/O1 current sink to DGND	70mA
Latch up immunity (any pin)	± 100 mA
Maximum power dissipation, T_A = 85° C (See notes)	TBD W
Thermal Data: In 44-pin QFN package	θ_{JA} 23.5° C/W
Thermal Data: In 44-pin QFN package	θ_{JC} TBD° C/W
ESD Immunity (Human Body Model)	1.5 kV minimum

Package Assembly

These 'green' package devices are assembled with enhanced environmentally compatible lead (Pb), halogen and antimony free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer Pb-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly. Refer to IPC/JEDEC J-Std-020B table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Microsemi guarantees the performance of this device over commercial (0ºC to 70ºC) and industrial (-40ºC to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40° C < T_A < +85° C
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Analog Supply AVDD	+3.3 V ± 5% DVDD ± 50 mV
Digital Supply DVDD	+3.3 V ± 5%
VB Supply for Le88 device	-99 V to -10 V
VB Supply for Le88 device	-150 V to -10 V
DGND	0 V
AGND with respect to DGND	±10 mV
BGND with respect to AGND/DGND	±100 mV
I/O1	DGND to +5.25 V
Voltage Reference Capacitor: VREF to AGND	0.68 µF ± 20%
Current Reference Resistor: IREF to AGND	75 kΩ ± 1%
Digital Pins	DGND to 3.465 V
Analog Pins	AGND– 0.3 V to AVDD + 0.3 V

ELECTRICAL CHARACTERISTICS

Test Conditions

Unless otherwise noted, test conditions are as follows:

- Typical values are for TA = 25º C and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in Operating Ranges, except where noted
- Test circuit is as shown in Figure 33, on page 43.
- AC load resistance R_L = 600 Ω
- 0 dBm (600 Ω) = 0.7746 Vrms.
- Default (unity) gain in GX, GR, X, R, DRL, AX and AR blocks
- Default coefficients in DISN, Z and B filters

Supply Currents and Power Dissipation

- Device or package power does not include power delivered to the load

Le88010 Operational State	Condition	I_{DD} mA Typ	Package Power mW Typ	Note
Shutdown	Hardware reset	3.7	13	1.
Idle Supervision Enabled, deactivated	On-Hook	9.2	31	1.
Active Supervision Enabled, activated	On or Off-Hook 0dBm into 600 Ω	18.0	60	1.

Notes:

1. Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.

DC Characteristics.

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Digital Input Low voltage	–	–	0.8	V	–
V_{IH}	Digital Input High voltage	2.0	–			–
I_{IL}	Digital Input leakage current	–7	–	+7	µA	–
I_{AIL}	Analog input leakage current	–1	–	+1		–
V_{HYS}	Digital Input hysteresis	0.16	0.25	0.34	V	–
V_{OL}	Digital Output Low voltage I/O1 (I_{OL} = 50 mA) I/O2 through I/O6 (I_{OL} = 4 mA) I/O2 through I/O6 (I_{OL} = 8 mA) Other digital outputs (I_{OL} = 2 mA)	–	–	0.8 0.4 0.8 0.4	V	1.
V_{OH}	Digital Output High voltage I/O1, I/O2 through I/O6 (I_{OH} = 4 mA) I/O1, I/O2 through I/O6 (I_{OH} = 8 mA) Other digital outputs (I_{OH} = 400 µA)	V_{CCD} – 0.4 V V_{CCD} – 0.8 V 2.4	–	–		1.
I_{OL}	Digital Output leakage current (Hi-Z state) 0 < V < DVDD	–7	–	+7	µA	–
V_{REF}	VREF output open circuit voltage (I_{VREF} = +/- 100 µA)	1.43	1.5	1.57	V	–
C_{IREF}	IREF pin maximum load capacitance	–	–	20	pF	–
C_I	Digital Input capacitance	–	–	10		–
C_O	Digital Output capacitance	–	–	10		–
$PSRR_1$	AVDD, DVDD Power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	40	–	–	dB	–
Z_{IN}	VINP, VINN input resistance	150	250	350	KΩ	–
I_{OUT}	VOUTP, VOUTN current drive into 150Ω to VREF	-6.8	–	+6.8	mA	–

Detector Threshold and Measurement Accuracy

See commands *A6/A7h Write/Read Converter Configuration*, on page 61 and *C2/C3h Write/Read Loop Supervision Parameters*, on page 62 for measurement thresholds, ranges and resolution.

Description	Test Conditions	Min	Typ	Max	Unit	Note
Disconnect Threshold	default, TDIS = 011b	TBD	4.2	TBD	V	–
Line In Use Threshold	default, TLIU = 010b	TBD	38	TBD	V	5.,3.
Metallic AC coupled voltage	Converter Configuration = 00h	-3	–	+3	%	
Tip voltage to ground	Converter Configuration = 04h	-1.5 V - 3%	–	+1.5 V + 3%	V	5.,3.
Ring voltage to ground	Converter Configuration = 05h	-1.5 V - 3%	–	+1.5 V + 3%	V	5.,3.
Metallic DC line voltage	Converter Configuration = 06h	-2.5 V - 3%	–	+2.5 V + 3%	V	5.,3.
Voice DAC (Full loopback)	Converter Configuration = 0Ah	-4	–	+4	%	5.,3.
Tip voltage to ground, low scale	Converter Configuration = 0Dh	-0.5V - 3%	–	+0.5V + 3%	V	5.,3.
Ring voltage to ground, low scale	Converter Configuration = 0Eh	-0.5V - 3%	–	+0.5V + 3%	V	5.,3.

Notes:

1. *The I/O1 output is resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.*
2. *See command C2/C3h Write/Read Loop Supervision Parameters, on page 62 for full scale and default values.*
3. *For DC measurements these limits require that the high pass filters are disabled in the operating conditions register and the residual A/D offset is removed by reading the no connect value (Converter Configuration 0Bh) and subtracting it from the measured value. DISN should be cut off (00h), the analog Voice Path Gains set to unity (00h) and the operating functions register set to linear mode (80h)*

Transmission Characteristics

Description	Test Conditions	Min	Typ	Max	Unit	Note
VINP - VINM input overload level	Active state, GX = AX = 0 dB	3.4	–	–	Vpk	6.
VINP or VINM overload level	Single-ended, Active state	1.7	–	–	Vpk	6., 7.
VINP - VINM 0 dBm0 reference level	Active state, A-Law and Linear modes	–	1.675	–	Vrms	6.
	Active state, µ-Law mode	–	1.669	–	Vrms	6.
VOUTP - VOUTM 0 dBm0 reference level	Active state, A-Law and Linear modes	–	1.005	–	Vrms	6.
	Active state, µ-Law mode	–	0.997	–	Vrms	6.
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz AR = AX = GR = GX = DRL = 0dB DISN, R, X, B and Z filters disabled	–0.25	–	+0.25	dB	
Attenuation distortion	300 to 3000 Hz	–0.125	–	+0.125	dB	5., 1.
Single frequency distortion		–	–	–46		2.
Second harmonic distortion, D-A	GR = 0 dB	–	–	–55		5.
Idle channel noise, Differential mode VOUTP - VOUTN DXA, Digital out	 DRA, Digital input = 0 A-law DRA, Digital input = 0 µ-law VINP - VINN = 0 VAC A-law VINP - VINN = 0 VAC µ-law	–	–	 -78 12 -68 16	 dBm0p dBrnC0 dBm0p dBrnC0	 3. 3. 3. 3.
Idle channel noise, Single-ended VOUTP/N - VREF DXA, Digital out	 DRA, Digital input = 0 A-law DRA, Digital input = 0 µ-law VINP = VINN = VREF A-law VINP = VINN = VREF µ-law	–	–	 -78 12 -68 16	 dBm0p dBrnC0 dBm0p dBrnC0	 3.,7. 3.,7. 3.,7. 3.,7.
End-to-end absolute group delay	B = Z = 0; X = R = 1	–	–	678	µs	4.

Notes:

1. *See Figure 16 and Figure 17.*
2. *0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
3. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
4. *The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
5. *This parameter is guaranteed by characterization or correlation to other tests.Typical values not tested in production.*
6. *Overload level is defined when THD = 1%.*
7. *For single-ended input, connect VINN to VREF and use VINP as input or connect VINP to VREF and use VINN as input*

Attenuation Distortion

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 16 and Figure 17. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

Figure 16. Transmit Path Attenuation vs. Frequency

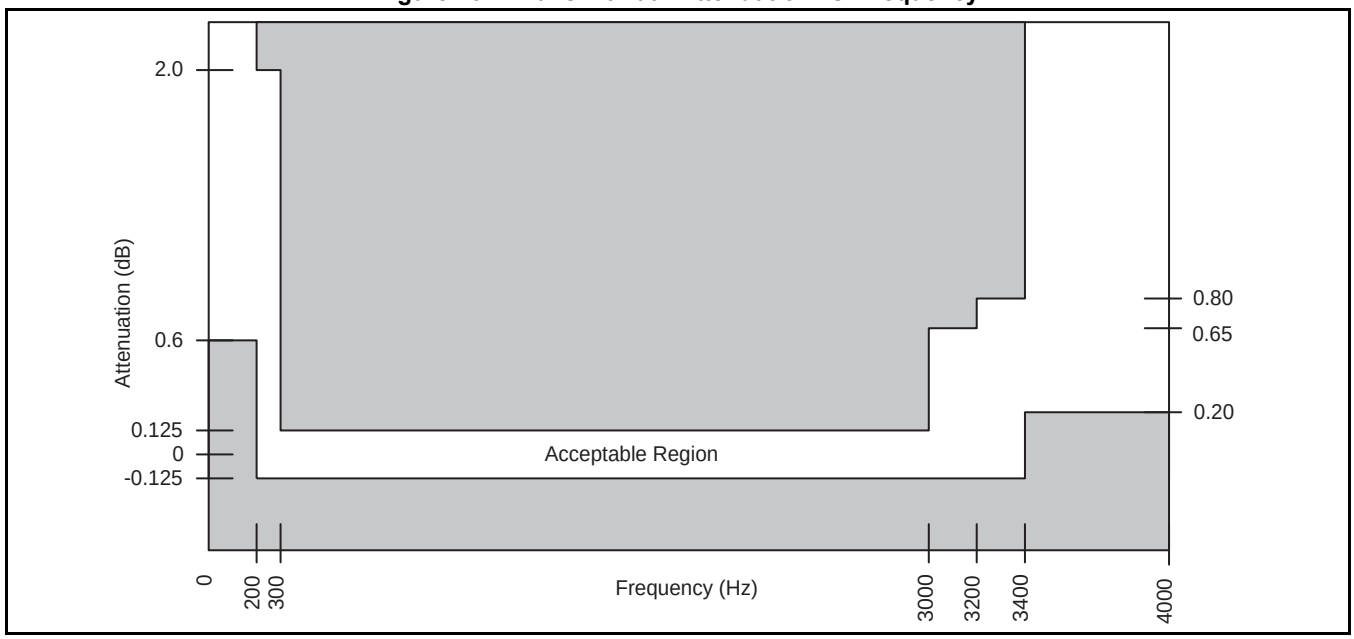
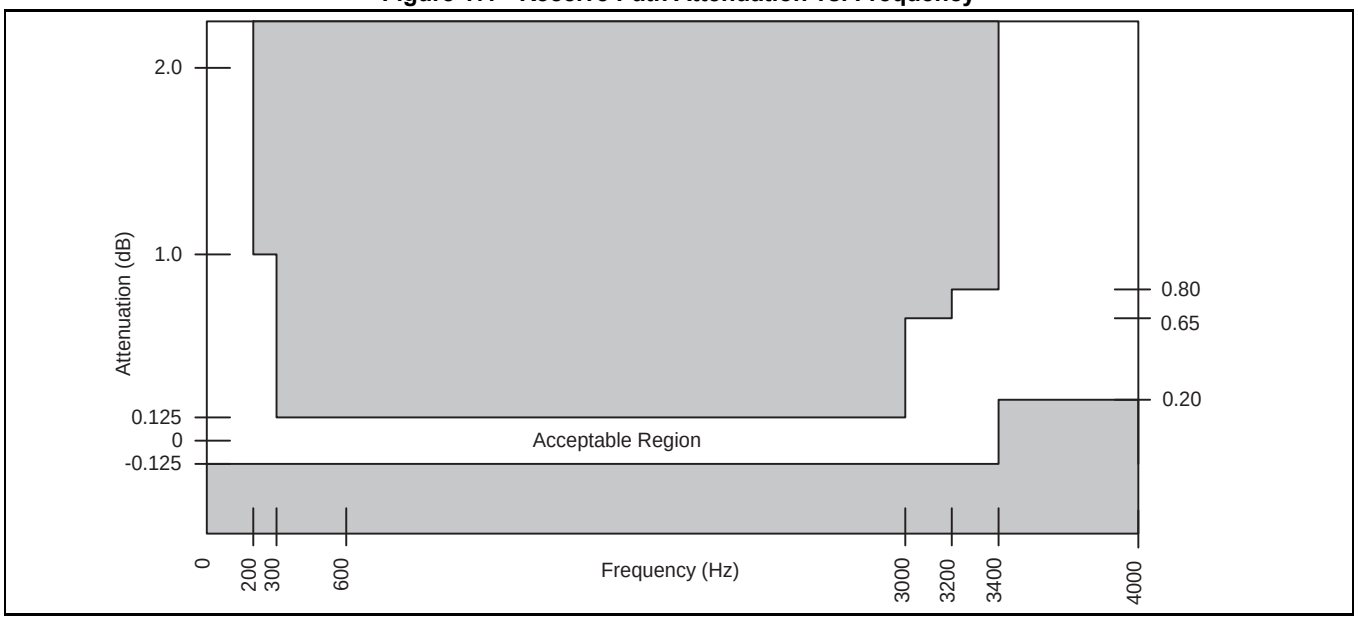


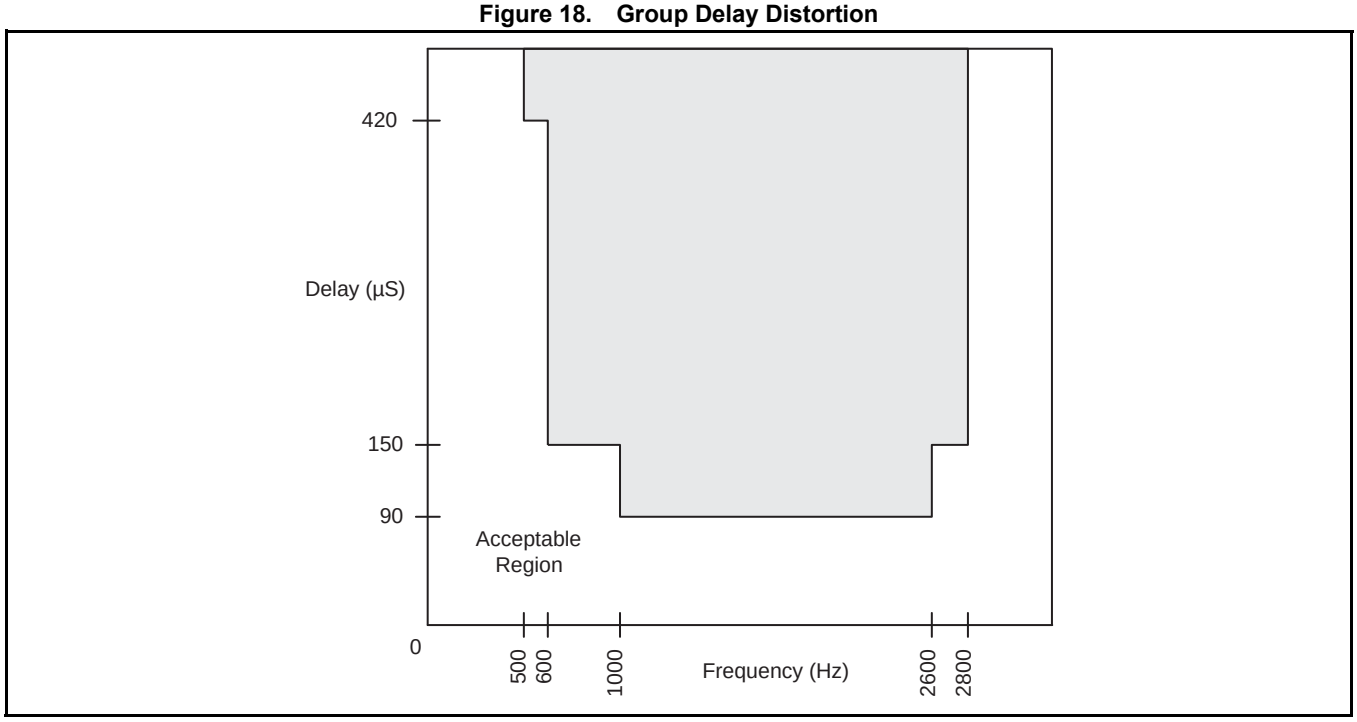
Figure 17. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 18. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Figure 18. Group Delay Distortion



Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 19 (A-law) and Figure 20 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 19. A-law Gain Linearity with Tone Input (Both Paths)

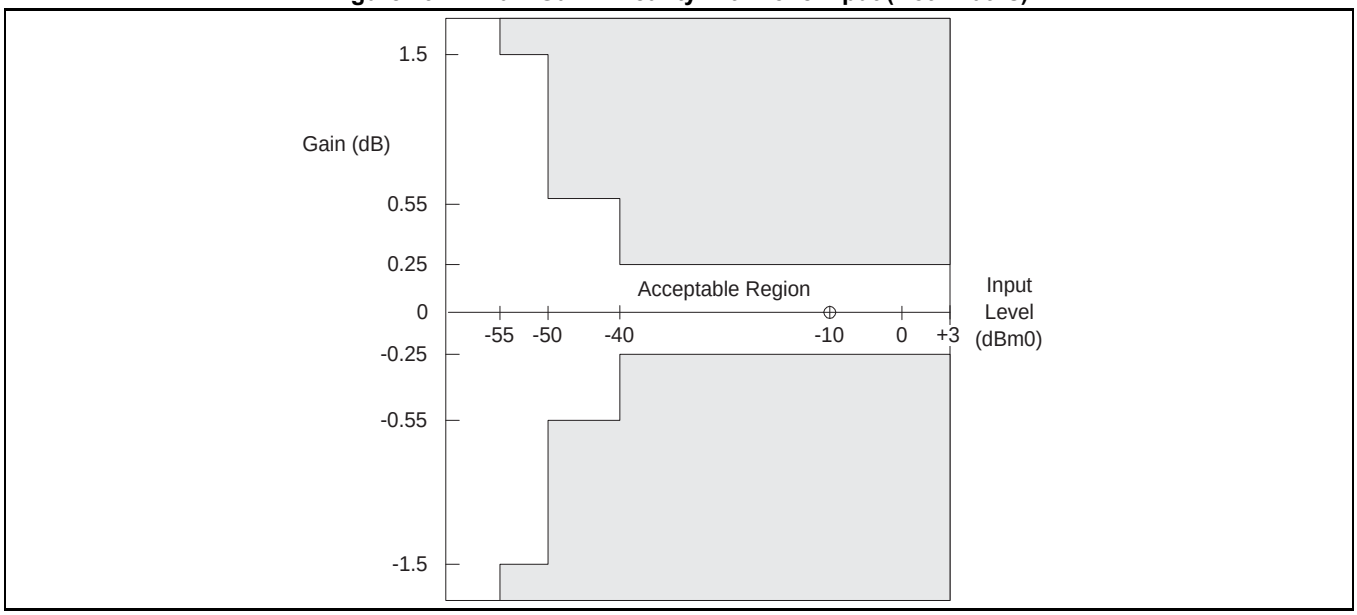
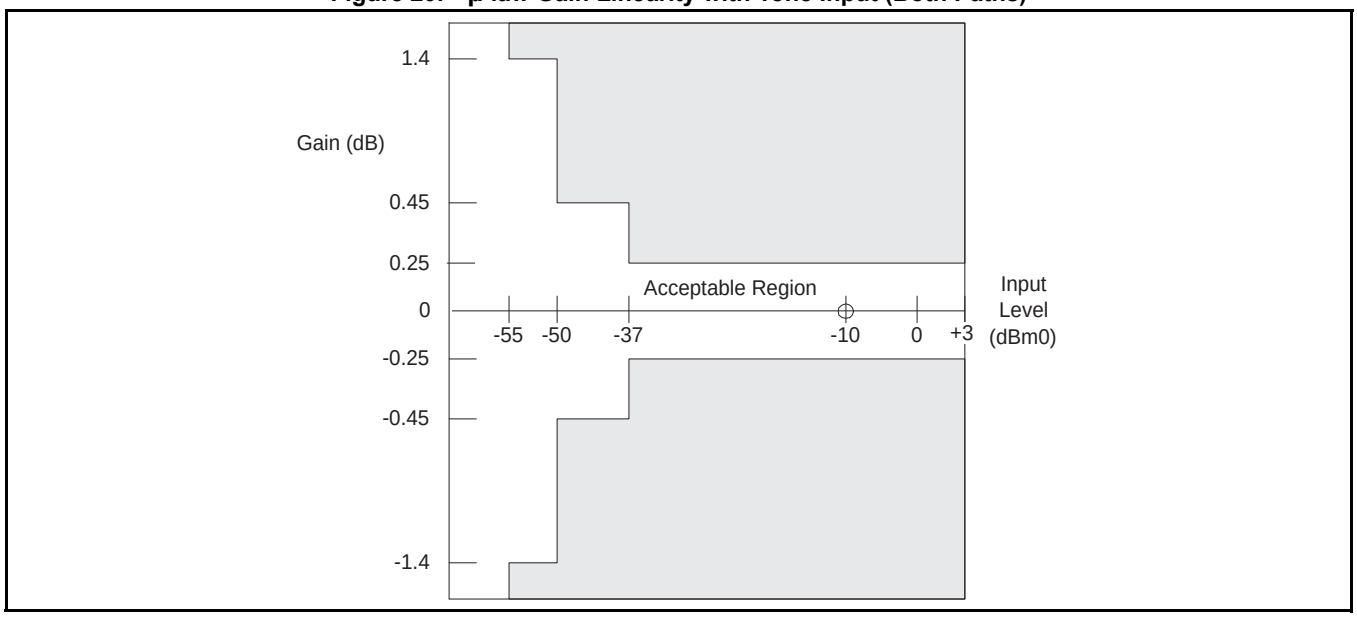


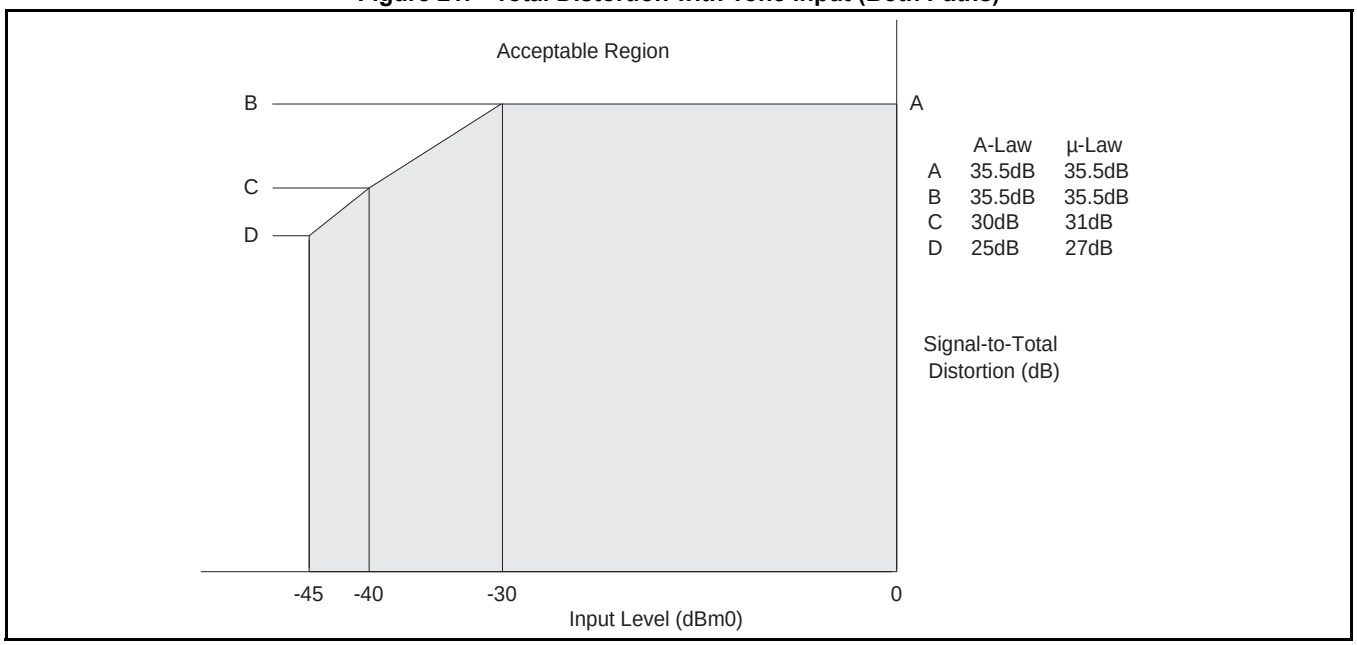
Figure 20. μ-law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 21 for either path when the input signal is a sine wave with a frequency of 1014 Hz.

Figure 21. Total Distortion with Tone Input (Both Paths)

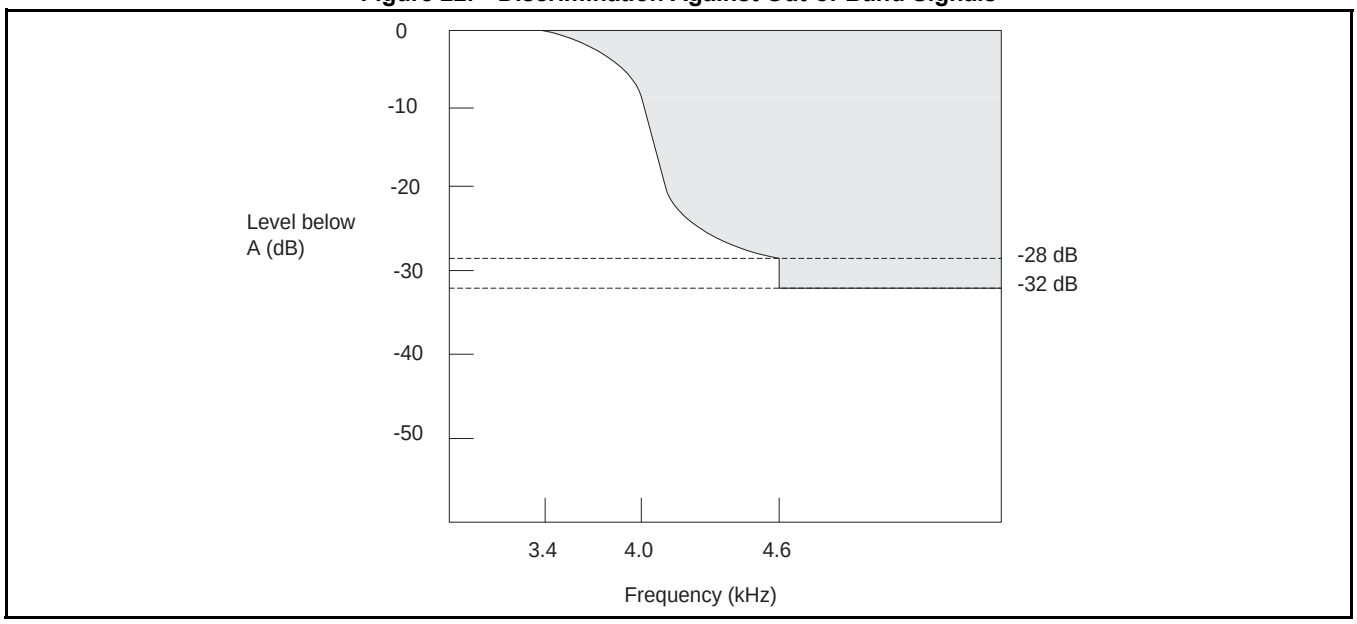


Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 22
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 22. Discrimination Against Out-of-Band Signals



Notes:

1. The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

Discrimination Against 12- and 16-kHz Metering Signals

Spurious Out-of-Band Signals at the Analog Output

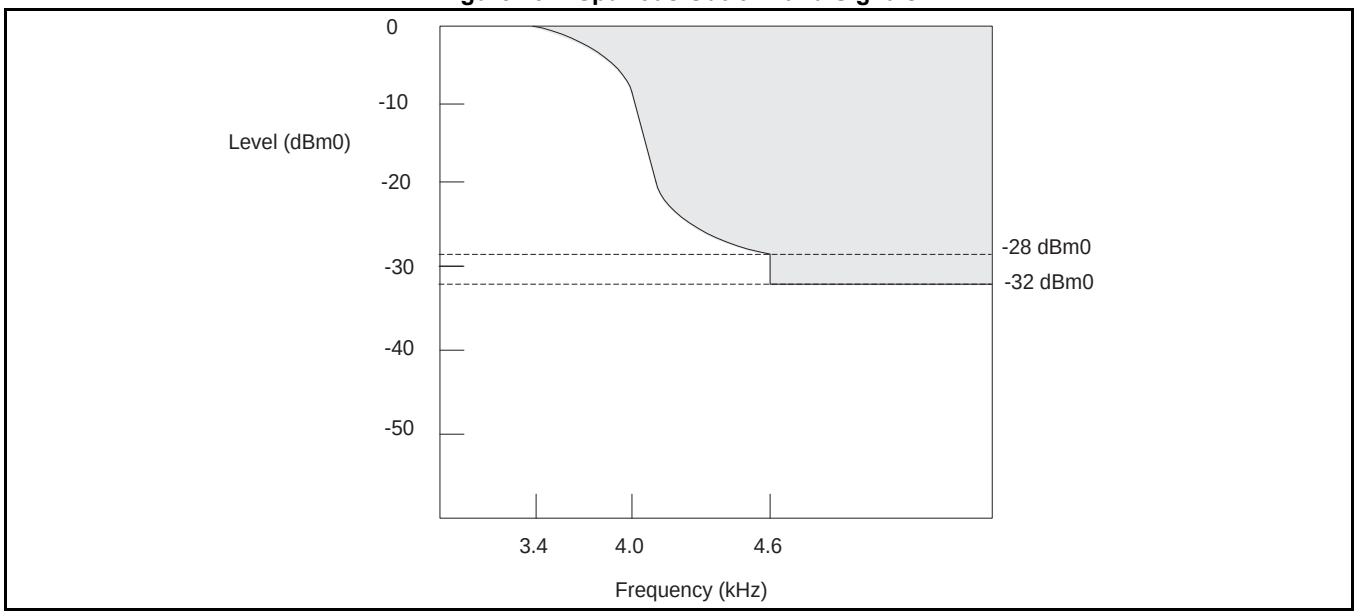
With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 23, on page 35. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

Figure 23. Spurious Out-of-Band Signals

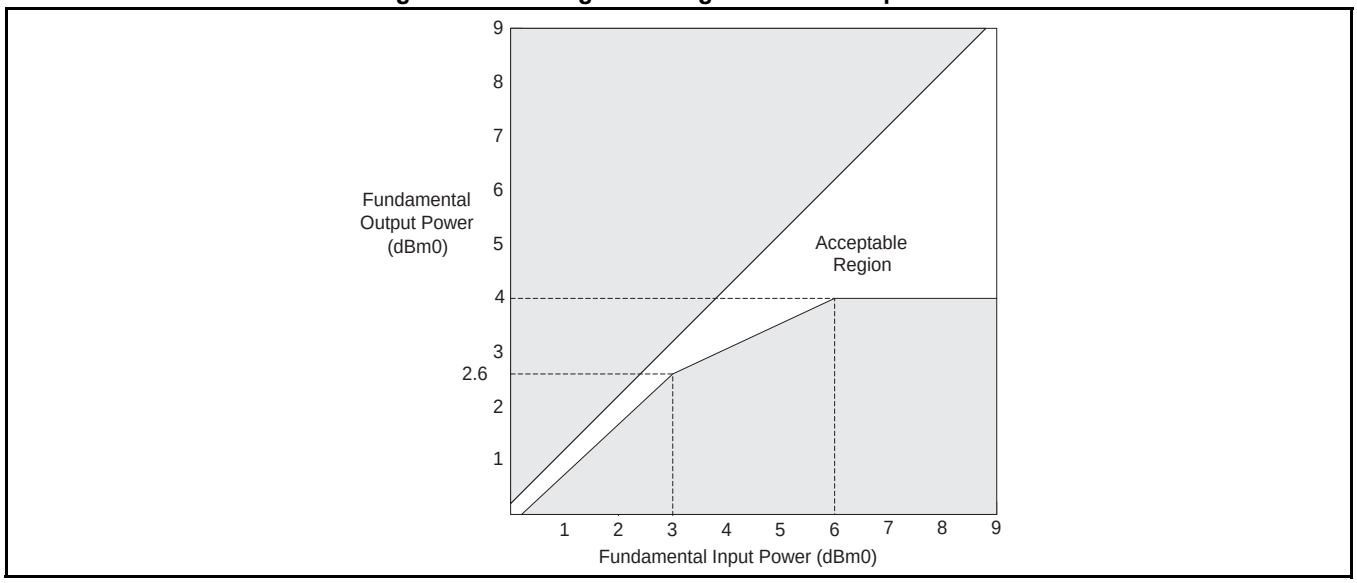


Overload Compression

Figure 24 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1.2 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1.2 dB
3. Digital voice output of one VoicePort device connected to digital voice input of a second VoicePort device.
4. Measurement analog-to-analog.

Figure 24. Analog-to-Analog Overload Compression



SWITCHING CHARACTERISTICS AND WAVEFORMS

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 115-pF load.

Microprocessor Interface

(See Figure 25 and Figure 26, on page 37 for the microprocessor interface timing diagrams.)

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122	–	–	ns	–
2	t_{DCH}	Data clock HIGH pulse width	48	–	–		–
3	t_{DCL}	Data clock LOW pulse width	48	–	–		–
4	t_{DCR}	Rise time of clock	–	–	25		–
5	t_{DCF}	Fall time of clock	–	–	25		–
6	t_{ICSS}	Chip select setup time, Input mode	30	–	t_{DCY} –10		–
7	t_{ICSH}	Chip select hold time, Input mode	0	–	t_{DCH} –20		–
8	t_{ICSL}	Chip select pulse width, Input mode	–	$8t_{DCY}$	–		–
9	t_{ICSO}	Chip select off time, Input mode	2500	–	–		1.
10	t_{IDS}	Input data setup time	25	–	–		–
11	t_{IDH}	Input data hold time	20	–	–		–
12	t_{OLH}	I/O1 through I/O6 output latch valid	–	–	2500		–
13	t_{OCSS}	Chip select setup time, Output mode	30	–	t_{DCY} –10		–
14	t_{OCSH}	Chip select hold time, Output mode	0	–	t_{DCH} –20		–
15	t_{OCSL}	Chip select pulse width, Output mode	–	$8t_{DCY}$	–		–
16	t_{OCSO}	Chip select off time, Output mode	2500	–	–		1.
17	t_{ODD}	Output data turn on delay	–	–	50		2.
18	t_{ODH}	Output data hold time	3	–	–		–
19	t_{ODOF}	Output data turn off delay	–	–	50		–
20	t_{ODC}	Output data valid	–	–	50		–
21	t_{RST}	Reset pulse width	50	–	–	µs	–

Notes:

1. *If CFAIL = 1 (Command 55h), GX, GR, Z, B1, X, R, and B2 coefficients must not be written or read without first deactivating all channels or switching them to default coefficients; otherwise, a chip select off time of 5 µs is required.*
2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*

Figure 25. Microprocessor Interface (Input Mode)

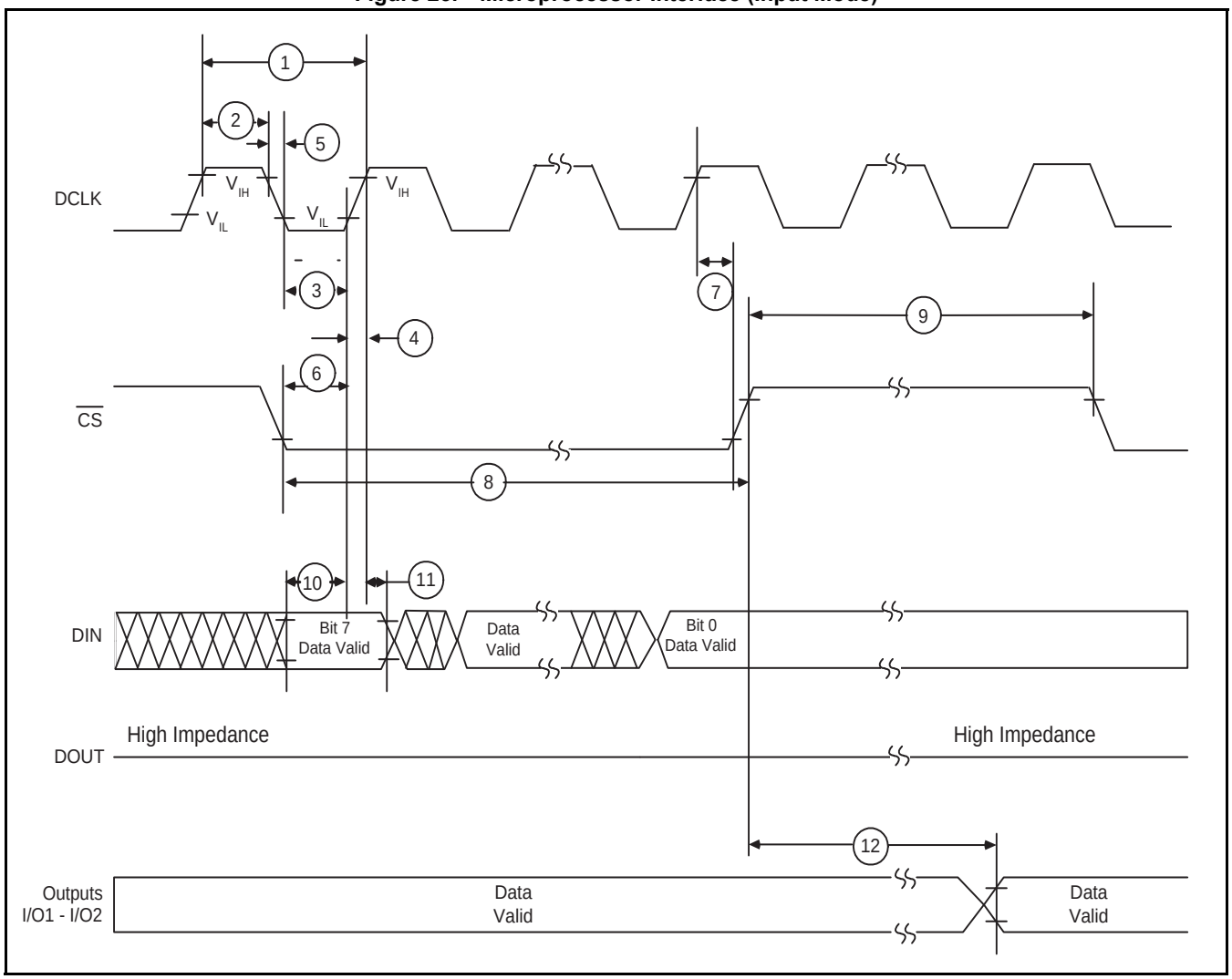
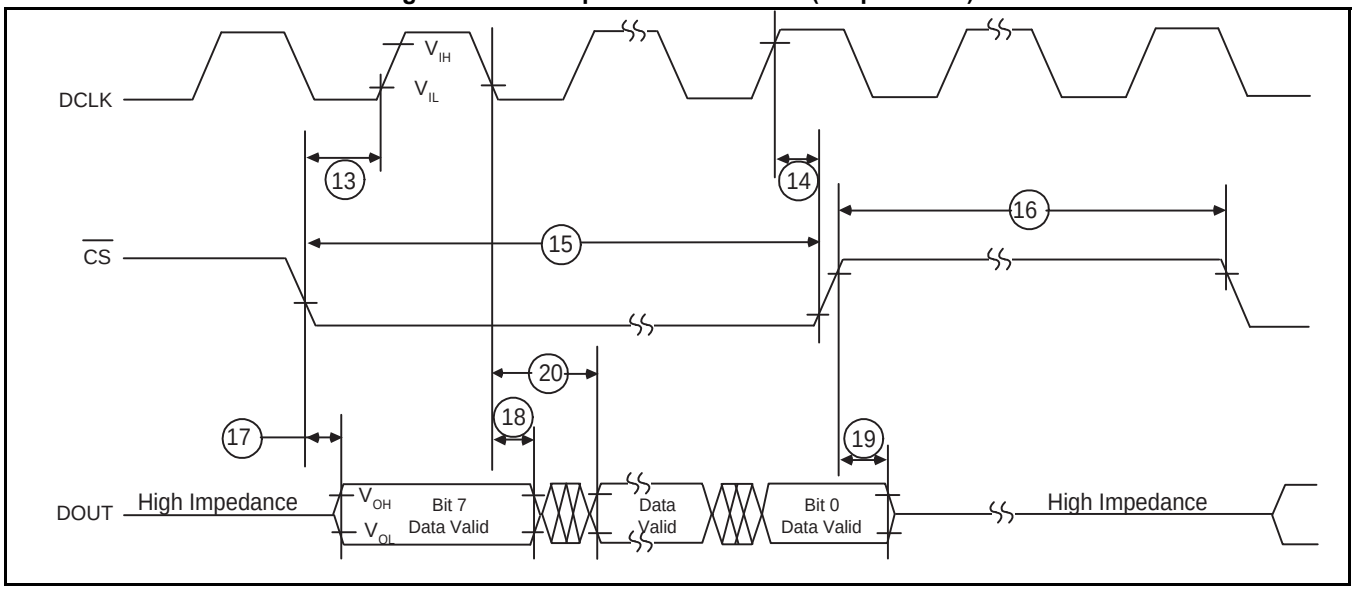


Figure 26. Microprocessor Interface (Output Mode)



PCM Interface

PCLK shall not exceed 8.192 MHz. (
See Figure 27 through Figure 29 for the PCM interface timing diagrams.)

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	122	–	651	ns	1.
23	t_{PCH}	PCM clock HIGH pulse width	48	–	–		–
24	t_{PCL}	PCM clock LOW pulse width	48	–	–		–
25	t_{PCF}	Fall time of clock	–	–	15		–
26	t_{PCR}	Rise time of clock	–	–	15		–
27	t_{FSS}	FS setup time	25	–	t_{PCY}–30		–
28	t_{FSH}	FS hold time	50	–	–		–
29	t_{FST}	PCM or frame sync jitter time	–50	–	50		1.
32	t_{DXD}	PCM data output delay	5	–	70		–
33	t_{DXH}	PCM data output hold time	5	–	70		–
34	t_{DXZ}	PCM data output delay to high Z	10	–	70		–
35	t_{DRS}	PCM data input setup time	25	–	–		–
36	t_{DRH}	PCM data input hold time	5	–	–		–

Notes:

1. *The PCLK frequency must be an integer multiple of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8-kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.536MHz and the maximum frequency is 8.192 MHz.*
2. *If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*

Figure 27. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

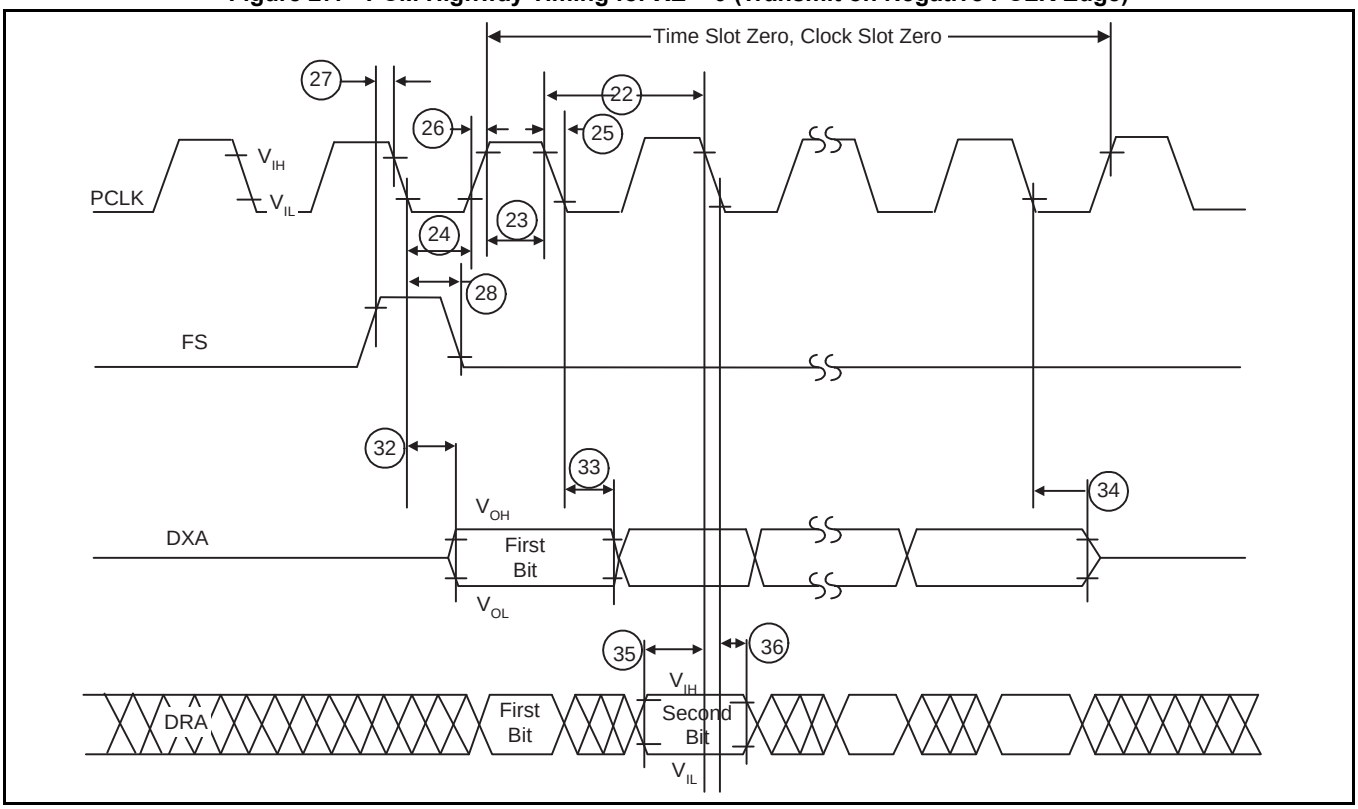


Figure 28. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

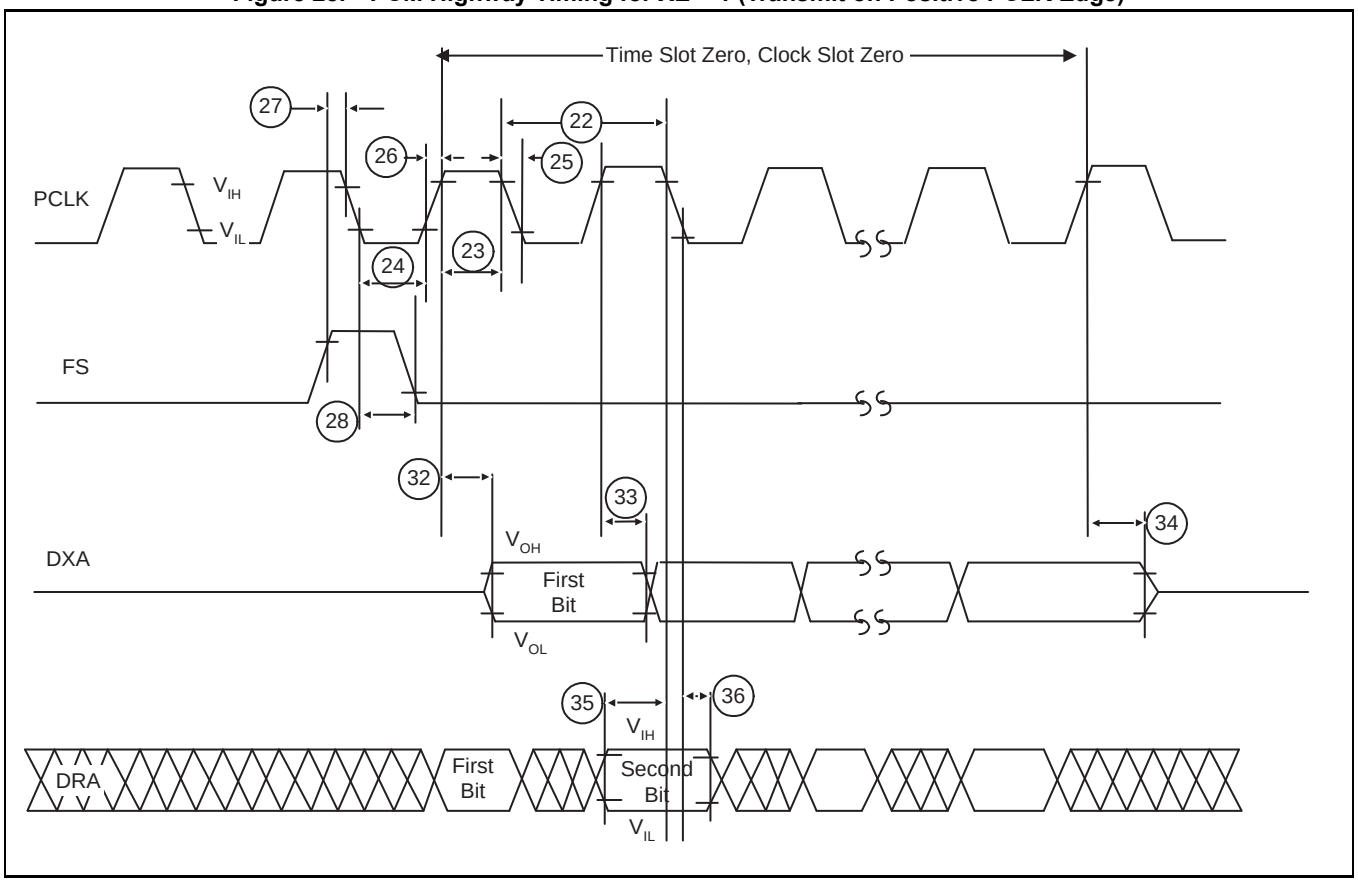


Figure 29. PCM Clock Timing

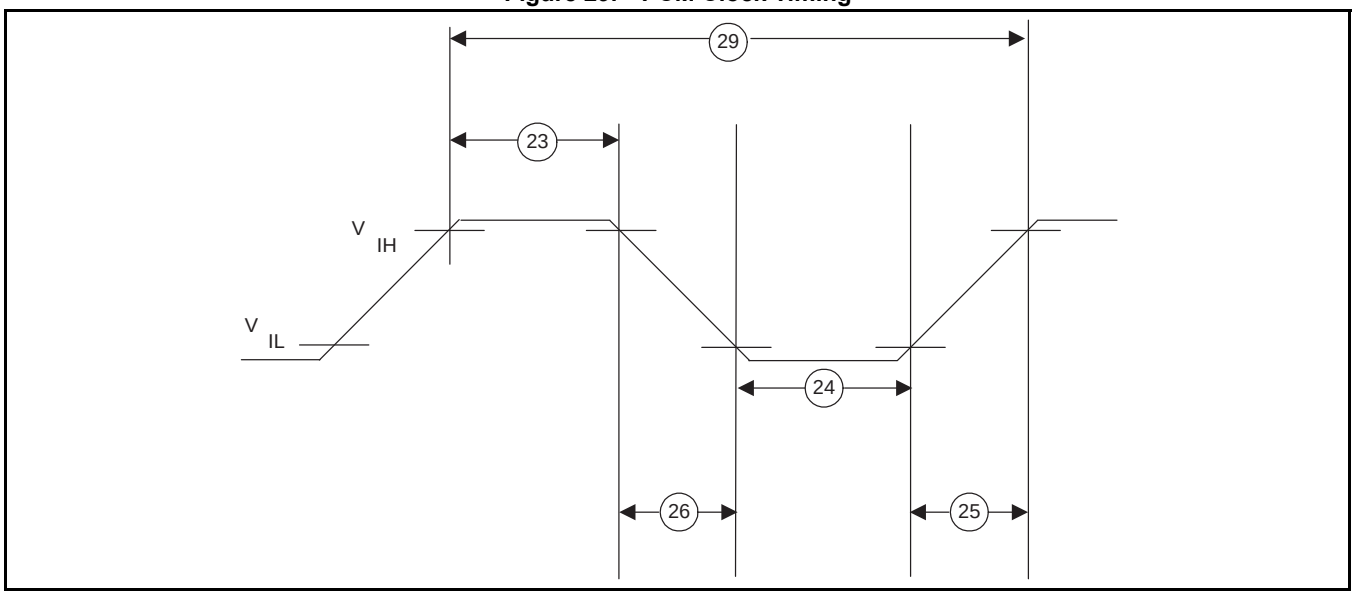
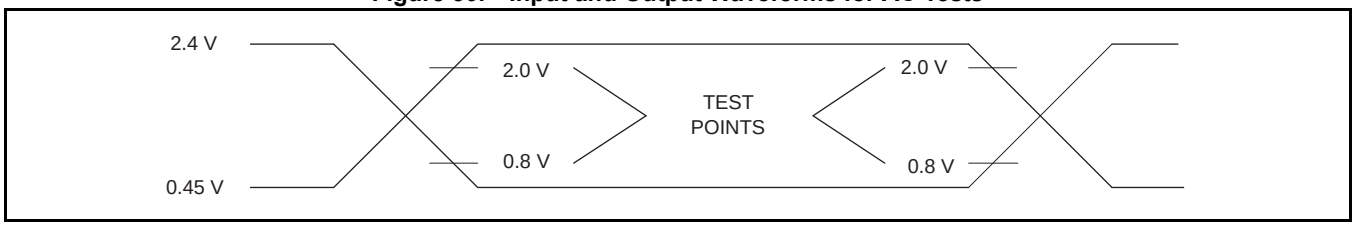


Figure 30. Input and Output Waveforms for AC Tests



GCI Timing

(See Figure 31 and Figure 32 for the GCI interface timing diagrams.)

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
37	J_{DCL}	DCL Jitter	–	–	50	ns	1.
38	t_R, t_F	Rise/fall time	–	–	60		–
39	t_{DCL}	Period, F_{DCL} = 2048 kHz	488.23	488.28	488.33		–
		F_{DCL} = 4096 kHz	244.11	244.14	244.17		–
40	t_{WH}, t_{WL}	Pulse width	90	–	–		–
41	t_{SF}	Setup time	70	–	t_{DCL}–50		–
42	t_{HF}	Hold time	50	–	–		–
43	t_{WFH}	High pulse width	130	–	–		–
44	t_{DDC}	Delay from DCL edge	–	–	100		–
45	t_{DDF}	Delay from FS edge	–	–	150		–
46	t_{SD}	Data setup	twH+20	–	–		–
47	t_{HD}	Data hold	50	–	–		–

Notes:

1. If DCL has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.

Figure 31. 4.096 MHz DCL Operation

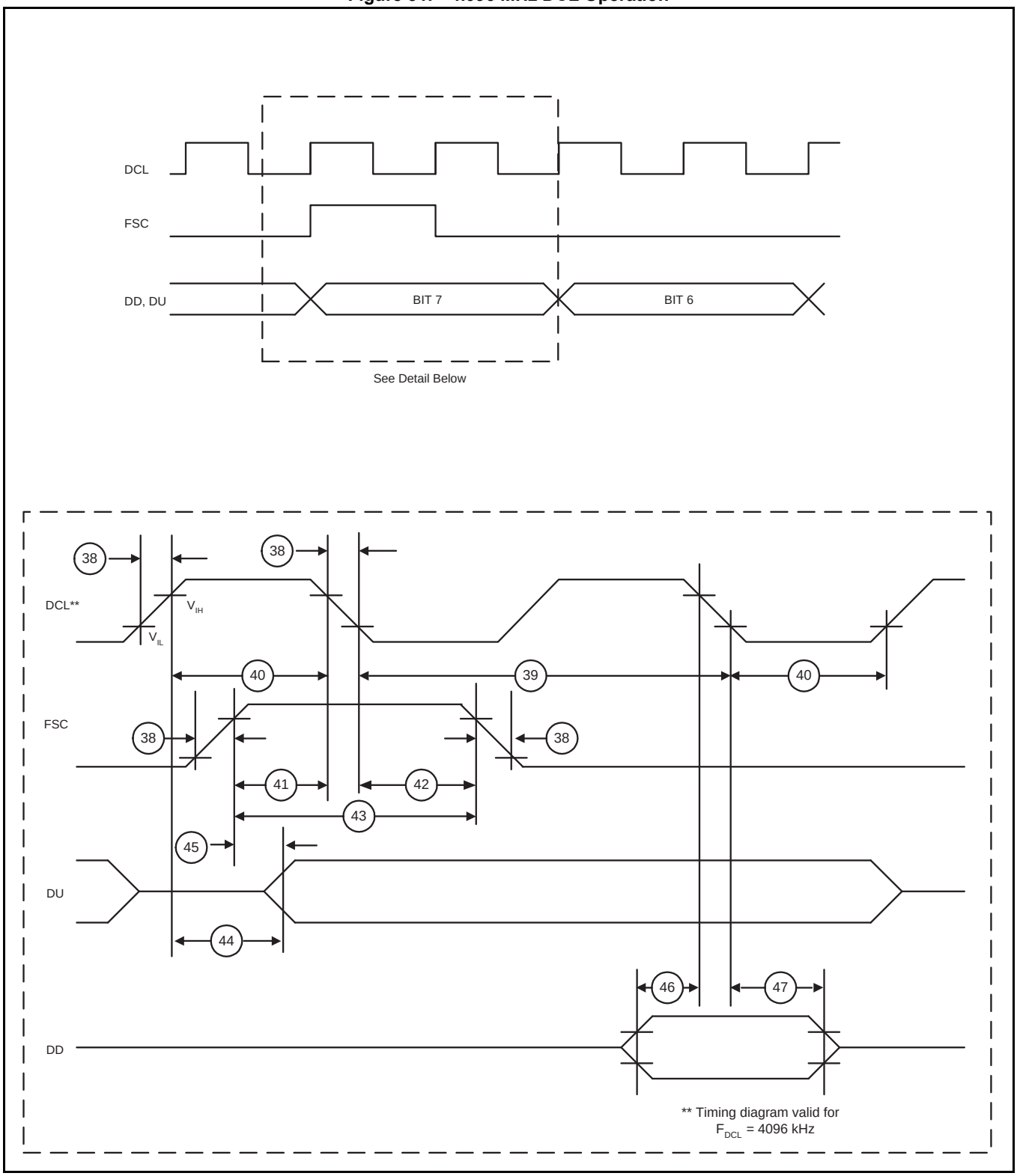
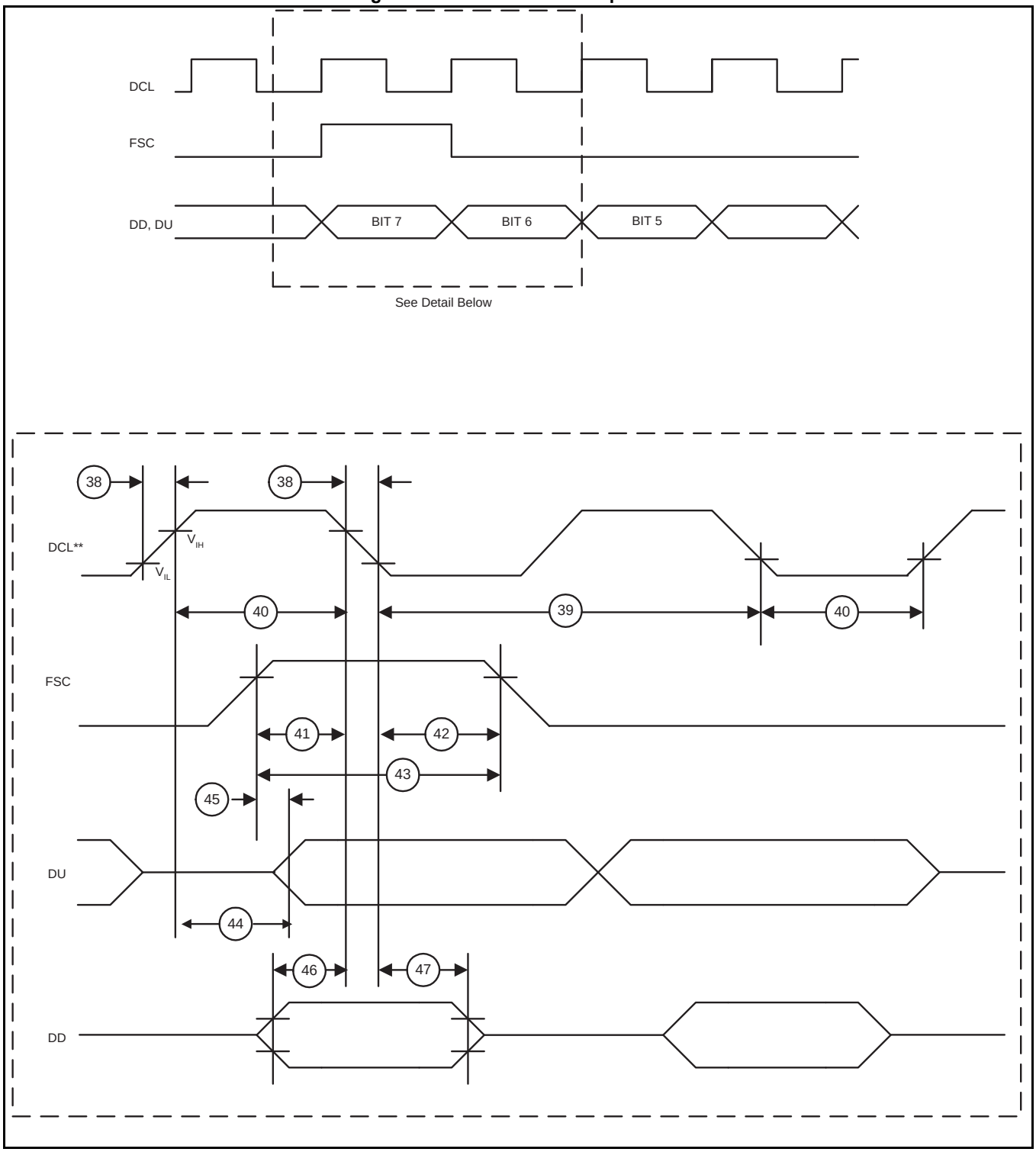
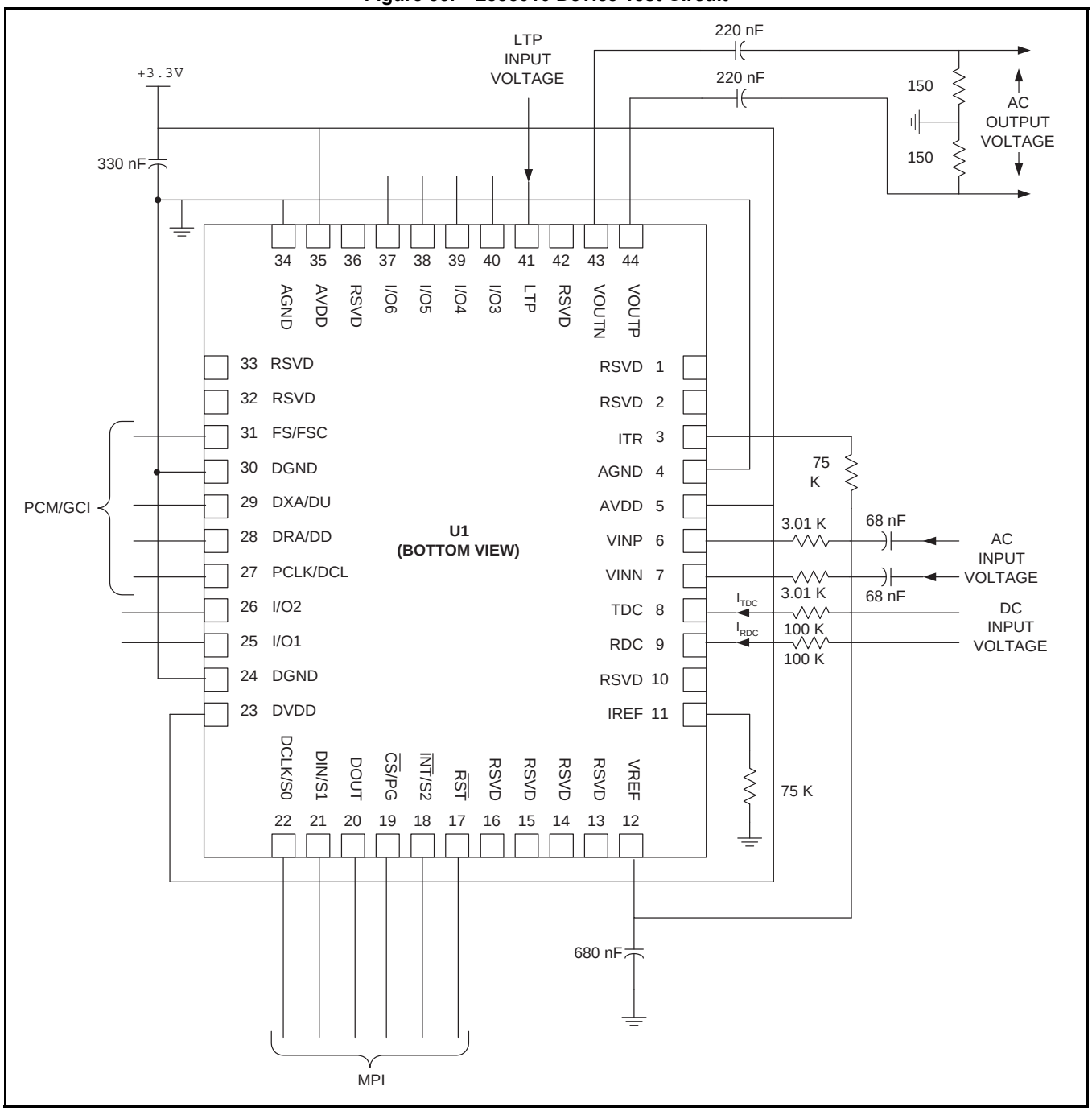


Figure 32. 2.048 MHz DCL Operation



TEST CIRCUIT

Figure 33. Le88010 Device Test Circuit



APPLICATIONS

The Le88010 device interfaces between a digital highway (PCM/MPI or GCI) and the telephone line in combination with a phone line interface (DAA). The Le88010 device provides access to time-critical information, such as incoming ringing detection, line polarity reversal and line disconnected via a single read operation. When various country or transmission requirements must be met, the Le88010 device can be reprogrammed to meet the required transmission characteristics.

Several Le88010 devices can be tied together in one bus interfacing to a common PCM or GCI interface. The Le88010 device is controlled through the microprocessor or GCI interface.

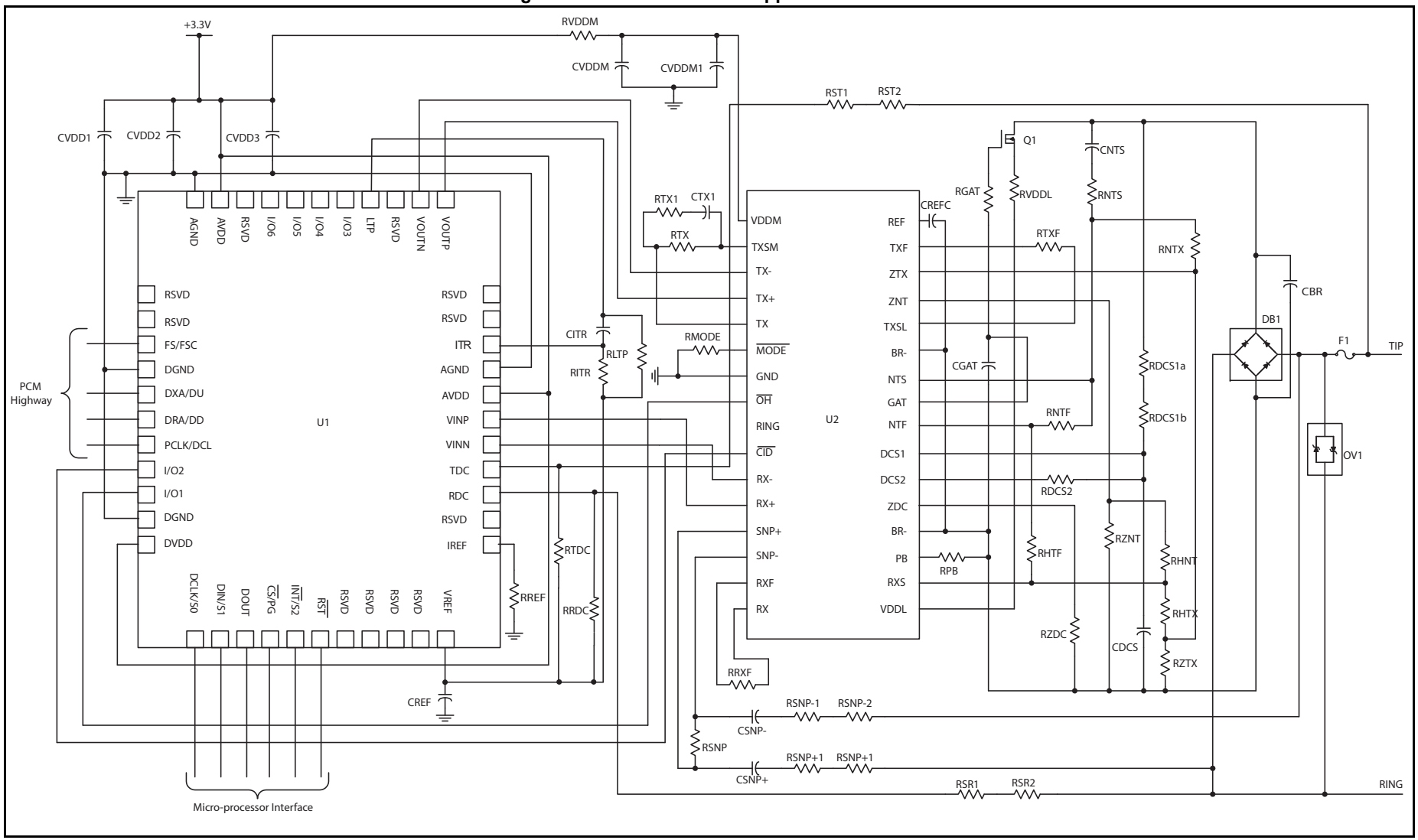
Le88010 VoicePort™ SLAC™ Parts List

The following list defines the parts and part values required to meet target specifications based on the application circuits shown in Figure 34

Table 7. VoicePort™ SLAC™ Parts List

Item	Qty.	Type	Value	Tol.	Rating	Package	Comments
CBR	1	ceramic cap	0.01uF	10%	300V	0805	AVX 12067C103KAT1A
CGAT	1	ceramic cap	100pF	10%	16V	0603	Tecate CMC016101KY0603T
CNTS	1	ceramic cap	0.1uF	10%	100V	1206	Tecate CMC100104KX1206T
CSNP-, CSNP+	2	ceramic cap	220pF	5% 1% Match	2000V	1808	Tecate CMC-2K0/221JN1808T#1-10
CVDDM	1	ceramic cap	10uF	10%	10V	1206	Tecate CMC010106KX51206T
CVDD1, CVDD2, CVDD3, CVDDM1, CTX1, CREFC	6	ceramic cap	0.1uF	10%	16V	0603	Panasonic ECJ-1VB1C104K
CREF	1	ceramic cap	680nF	10%	10V	0603	Panasonic ECJ-1VC1A684K
CITR	1	ceramic cap	47nF	10%	6.3V	0603	Panasonic ECJ-1VB0473M
CDCS	1	ceramic cap	27nF	10%	50V	0603	Panasonic ECJ-1VB1H273K
U1	1	VoicePort SLAC	–	–	–	44-QFN	Legerity Le88010
U2	1	LITELINK	–	–	–	DIP32 SOIC	Clare CPC5621
F1	1	1206	1A	–	–	1206	Littlefuse 429.001
DB1	1	BR_RECT	0.8A	–	600V	SSMT	Shindengen S1ZB60
OV1	1	TRAN SUPP	VAR13	–	–	DO-214AA	Teccor P3100SC
Q1	1	PWR MOS	–	–	350V	SOT223	Clare CPC5602C
RST1, RST2, RSR1, RSR2	4	CHIP RES	5.1Meg	1%	1/4W	1206	Yageo 9C12063A5104FKFT
RREF	1	CHIP RES	75K	1%	1/16W	0603	Panasonic ERJ-3EKF7502V
RTX1	1	CHIP RES	200K	1%	1/16W	0603	Panasonic ERJ-3EKF2003V
RDCS1a, RDCS1b	2	CHIP RES	6.49Meg	1%	1/16W	0603	IMS RCI-0603-6494F
RDCS2	1	CHIP RES	1.69Meg	1%	1/16W	0603	IMS RCI-0603-1694F
RGAT	1	CHIP RES	47	1%	1/16W	0603	IMS RCI-0603-47R0F
RHNT, RMODE	2	CHIP_RES	DNP	1%	1/16W	0603	IMS RCI-0603-1002F
RHTF	1	CHIP RES	143K	1%	1/16W	0603	IMS RCI-0603-1433F
RHTX	1	CHIP RES	340K	1%	1/16W	0603	IMS RCI-0603-3403F
RNTF	1	CHIP_RES	309K	1%	1/16W	0603	IMS RCI-0603-3093F
RNTS	1	CHIP_RES	1M	1%	1/16W	0603	IMS RCI-0603-1004F
RITR, RLTP	2	CHIP_RES	75K	1%	1/16W	0603	IMS RCI-0603-7502F
RNTX	1	CHIP_RES	154K	1%	1/16W	0603	IMS RCI-0603-1543F
RPB	1	CHIP RES	68.1	1%	1/16W	0603	IMS RCI-0603-68R1F
RRXF	1	CHIP RES	130K	1%	1/16W	0603	IMS RCI-0603-1303F
RSNP	1	CHIP RES	1.5M	1%	1/16W	0603	AVX CR10155GT
RSNP-1,RSNP+1 RSNP-2,RSNP+2	4	CHIP RES	1.82M	1%	1/8W	1206	IMC RCI-1206-1824F
RTX	1	CHIP RES	80.6K	1%	1/16W	0603	IMC RCI-0603-8062F
RTXF	1	CHIP RES	60.4K	1%	1/16W	0603	IMS RCI-0603-6042F
RVDDL	1	CHIP RES	2	5%	1/16W	0603	AVX CR102R0JT
RVDDM	1	CHIP RES	10	5%	1/16W	0603	AVX CR10100JT
RZDC	1	CHIP RES	8.2	1%	1/16W	0603	AVX CR108R2FT
RZNT	1	CHIP RES	187	1%	1/16W	0603	IMS RCI-0603-1870F
RZTX	1	CHIP RES	3.32k	1%	1/16W	0603	IMS RCI-0603-3221F
RRDC, TRDC	2	CHIP RES	22K	1%	1/16W	0603	IMS RCI-0603-2202F

Figure 34. Le88010 Device Application Circuit



COMMAND DESCRIPTION AND FORMATS

Command Field Summary

A microprocessor can program and control the Le88010 device using the MPI or GCI. Data programmed previously can be read out for verification. See *Detailed Descriptions of Commands*, on page 48 for the channel and global chip parameters assigned.

MPI DESCRIPTION

This device has a Channel Enable register that allows access to functions linked to the voice channel within the device to be accessed, while other device functions are always accessible on a global basis independent of the setting of the Channel Enable bit. This approach allows for easy expansion to devices incorporating additional voice channels.

The MPI consists of a serial data input (DI) a data output (DO), a data clock (DCLK), and a chip select ($\overline{CS}$). The scope of the commands can be either Global or Voice Channel specific, as indicated in the *Summary of MPI Commands*, on page 47. Access to the Voice Channel commands are controlled by the voice Channel Enable bit (EC1) in the *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 50. The serial input consists of 8-bit commands that can be followed by additional bytes of input data, or by the Le88010 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least a minimum off period before the next byte is read or written.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed as 0 (unless otherwise noted) to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The Le88010 device will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le88010 devices, and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multibyte read or write command sequence, DCLK can also stay in the High state indefinitely. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a High level.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes Low, data will be present at the DO pin even if DCLK has no activity.

SUMMARY OF MPI COMMANDS

Hex*	Description	Scope	Page #
02h	Software Reset	Channel	page 48
04h	Hardware Reset	Global	page 48
06h	No Operation	Global	page 48
1Fh	Read Period Detector	Channel	page 48
40/41h	Write/Read Transmit Time Slot	Channel	page 49
42/43h	Write/Read Receive Time Slot	Channel	page 49
44/45h	Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge	Global	page 49
46/47h	Write/Read Device Configuration Register	Global	page 49
4A/4Bh	Write/Read Channel Enable & Operating Mode Register	Global	page 50
4D/4Fh	Read Signaling Register	Global	page 50
50/51h	Write/Read Voice Path Gains	Channel	page 52
52/53h	Write/Read Input/Output Data Register	Channel	page 52
54/55h	Write/Read Input/Output Direction Register	Channel	page 53
56/57h	Write/Read System State	Channel	page 53
60/61h	Write/Read Operating Functions	Channel	page 54
68/69h	Write/Read System State Configuration	Channel	page 55
6C/6Dh	Write/Read Interrupt Mask Register	Global	page 55
70/71h	Write/Read Operating Conditions	Channel	page 55
73h	Read Revision and Product Code Number (RCN, PCN))	Global	page 56
80/81h	Write/Read GX Filter Coefficients	Channel	page 56
82/83h	Write/Read GR Filter Coefficients	Channel	page 57
86/87h	Write/Read B Filter FIR Coefficients	Channel	page 57
88/89h	Write/Read X Filter Coefficients	Channel	page 58
8A/8Bh	Write/Read R Filter Coefficients	Channel	page 59
96/97h	Write/Read B Filter IIR Coefficients	Channel	page 60
98/99h	Write/Read Z Filter FIR Coefficients	Channel	page 60
9A/9Bh	Write/Read Z Filter IIR Coefficients	Channel	page 60
A6/A7h	Write/Read Converter Configuration	Channel	page 61
C2/C3h	Write/Read Loop Supervision Parameters	Channel	page 62
CA/CBh	Write/Read Digital Impedance Scaling Network (DISN)	Channel	page 63
CDh	Read Transmit PCM/Test Data	Channel	page 63
D2/D3h	Write/Read Signal Generator A, B	Channel	page 64
DE/DFh	Write/Read Signal Generator Control	Channel	page 65
E0/E1h	Write/Read Cadence Timer	Channel	page 66

Notes:

1. **All codes not listed are reserved by Microsemi and should not be used.*

DETAILED DESCRIPTIONS OF COMMANDS

This section details each command used by the Le88010 device. The command is shown, along with the format of any additional data bytes that follow. Unused bits are indicated by “RSVD”; 0’s should be written to these bits (unless otherwise noted), but 0’s are not guaranteed when they are read.

In all commands:

R/$\overline{W}$ = 0: Write

R/$\overline{W}$ = 1: Read

*Default field values are marked by an asterisk. A hardware reset forces the default values.

02h Software Reset

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 02h	0	0	0	0	0	0	1	0

This command only operates on the channels selected by the Channel Enable Register and it does not change clock slots, time slots or global chip parameters. The selected channels will be put into the Disconnect state as a result of a Software reset unless that channel is in the Shutdown state in which case it will stay in the Shutdown state.

04h Hardware Reset

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 04h	0	0	0	0	0	1	0	0

Hardware reset is equivalent to pulling the $\overline{RST}$ pin on the device Low.
This command does not depend on the state of the Channel Enable Register. A Hardware reset will put all channels into the Shutdown state.

Note:
The action of a hardware reset is described in the section on operating the Le88010 device.

06h No Operation

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 06h	0	0	0	0	0	1	1	0

1Fh Read Period Detector

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R: 1Fh	0	0	0	1	1	1	1	1
I/O Data Byte 1:	PERD7	PERD6	PERD5	PERD4	PERD3	PERD2	PERD1	PERD0

PERD[7:0]: Pulse period.
Period of external ringing signal (EXPDT = 0)
or time between rising edges of IO4 (period) (EXPDT = 1).
(0 - 63.75 ms with a scale of 0.25 ms).

This command is read only. Writes to this location are ignored.

40/41h Write/Read Transmit Time Slot

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 40h R: 41h	0	1	0	0	0	0	0	R/$\overline{W}$
I/O Data	RSVD	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0

TTS[6:0]: Transmit Time Slot

0–127: Time Slot Number (TTS0 is LSB, TTS6 is MSB)

This command applies to PCM mode only. Its contents are ignored in GCI mode.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

42/43h Write/Read Receive Time Slot

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 42h R: 43h	0	1	0	0	0	0	1	R/$\overline{W}$
I/O Data	RSVD	RTS6	RTS5	RTS4	RTS3	RTS2	RTS1	RTS0

RTS[6:0]: Receive Time Slot

0–127: Time Slot Number (RTS0 is LSB, RTS6 is MSB)

This command applies to PCM mode only. Its contents are ignored in GCI mode.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

44/45h Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 44h R: 45h	0	1	0	0	0	1	0	R/$\overline{W}$
I/O Data	RSVD	XE	RCS2	RCS1	RCS0	TCS2	TCS1	TCS0

XE Transmit Edge

0*: Transmit changes on negative edge of PCLK

1: Transmit changes on positive edge of PCLK

RCS[2:0]: Receive Clock Slot

0*–7: Receive Clock Slot number

TCS[2:0]: Transmit Clock Slot

0*–7: Transmit Clock Slot number

This command does not depend on the state of the Channel Enable Register.
This command applies to PCM mode only. Its contents are ignored in GCI mode.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

46/47h Write/Read Device Configuration Register

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 46h R: 47h	0	1	0	0	0	1	1	R/$\overline{W}$
I/O Data	INTM	RSVD	SMODE	RSVD	CSEL3	CSEL2	CSEL1	CSEL0

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

INTM: Interrupt Mode

0: CMOS-compatible output

1*: Open drain output

SMODE: PCM Signaling Mode

0*: No signaling on PCM highway
1: Signaling on PCM highway

The PCM clock frequency can be selected by CSEL.

CSEL[3:0]:	PCM Clock Frequency
0000	1.536 MHz
0001	1.544 MHz
0010	2.048 MHz
0011	Reserved
0100	3.072 MHz
0101	3.088 MHz
0110	4.096 MHz
0111	Reserved
1000	6.144 MHz
1001	6.176 MHz
1010*	8.192 MHz
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

This command does not depend on the state of the Channel Enable Register.
This command applies to PCM mode only. Its contents are ignored in GCI mode.

In the absence of external PCLK, the on chip master clock will slow down to it's minimum operating frequency which will be in the range of 1/5 - 1/2 of its normal operating frequency.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 8Ah.

4A/4Bh Write/Read Channel Enable and Operating Mode Register

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 4Ah R: 4Bh	0	1	0	0	1	0	1	R/$\overline{W}$
I/O Data	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EC

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

EC: Channel Enable

0: Disabled, channel cannot receive commands
1*: Enabled, channel can receive commands

* Power Up and Hardware Reset ($\overline{RST}$) Value = 01h.

4D/4Fh Read Signaling Register

This register reads signaling data with (4F) or without (4D) clearing any corresponding interrupt.

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R: 4Dh R: 4Fh	0	1	0	0	1	1	x	1
I/O Data Byte 1	CFAIL	POL	POH	IO2	CAD	DIS	RNGDT	LIU
I/O Data Byte 2	DAT	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

The read without clearing interrupt command (4D) allows signaling bits that are masked (see 6C/6Dh

Write/Read Interrupt Mask Register, on page 55) to be monitored via polling the signaling register, while other bits that are unmasked are serviced in response to interrupts.

An interrupt is generated by pulling the $\overline{INT}$ pin low, or setting the SLCX bit in the upstream GCI SC channel, whenever any unmasked bit in the signaling register changes. There are two types of interrupt:

Type A interrupts are generated on both edge transitions and present the current status of the signal. When the signal state changes, the new state is locked in the signaling register, and an interrupt is generated. When the interrupt is cleared by reading the status in the signaling register (4Fh), the status corresponding to the interrupt is not necessarily cleared. A new interrupt will be generated only when a new change occurs.
CFAIL, IO2, POL, DIS, RNGDT and LIU are type A interrupts

Type B interrupts are generated when a specific event occurs. The corresponding signal is set to 1 and an interrupt is generated. When the read signaling register and clear interrupt (4Fh) command is issued, the interrupt is cleared and the signal is reset.
CAD and POH are type B interrupts.

Other status bits may change while an interrupt is pending. In this case, an additional interrupt is not generated if the new status is reported when the register is read. If the bit that caused the original interrupt has changed after it was latched in the signaling register but before the interrupt was cleared, the latched value will be read and a new interrupt with the new value (which will be latched) will be generated immediately after the interrupt is cleared.

The behavior of the various signals in this register depends on the contents of *C2/C3h Write/Read Loop Supervision Parameters*, on page 62 where thresholds and debounce periods are set.

This command does not depend on the state of the Channel Enable register

DAT: Converter data.

- 0: No new data is available in *CDh Read Transmit PCM/Test Data*, on page 63
- 1: New data is available in *CDh Read Transmit PCM/Test Data*, on page 63

  When unmasked by the ATI bit in the *A6/A7h Write/Read Converter Configuration*, on page 61 the DAT interrupt will be asserted at the time new data is ready to be read from *CDh Read Transmit PCM/Test Data*, on page 63. The interrupt pin is returned to a high level after 54 µsec.

CFAIL: Clock Fail

- 0: The internal clock is synchronized to frame sync.
- 1: The internal clock is not synchronized to frame sync.

When clock fail is set, the data path is cleared for all channels.

POL: Polarity of line voltage

- 0: Normal Polarity. Tip more positive than Ring.
- 1: Reverse Polarity. Ring more positive than Tip

An interrupt generated by this signal indicates a polarity reversal has occurred. Note that this signal will also be generated when on hook and incoming ringing starts

POH: Parallel Off Hook detected while off hook

- 0*: A parallel off hook event has not occurred
- 1: A parallel off hook event occurred

This signal reports a transient event. This signal should be unmasked to ensure that when a parallel off hook event occurs it is latched and an interrupt generated (POH bit is set). Note that this signal will also be set due to an off-hook polarity reversal event

IO2: Input 2 Status. The input value at IO2

- 0: IO2 input is low

1: IO2 input is high

CAD: Cadencer status when masked or interrupt if unmasked

0: Cadence timer is in the programmed on period (masked)
1: Cadence timer is in the programmed off period (masked)

0: Cadence interrupt has not occurred (unmasked).
1: Cadence interrupt has occurred (unmasked)
Cadencer has completed the programmed on period

DIS: Line Disconnected status

0: Connected (Line voltage greater than the TDIS threshold for longer than DDIS)
1: Disconnected (Line voltage less than the TDIS threshold for longer than DDIS)

RNGDT: Ringing Detect

0: RInging not detected
1: Ringing Detected

LIU: Line in Use (Significant when on hook)

0: Line not in use (line voltage greater than TLIU threshold for longer than DLIU)
1: Line in use (line voltage less than the TLIU threshold for longer than DLIU)

* Power Up and Hardware Reset ($\overline{RST}$) Value = 0000

50/51h Write/Read Voice Path Gains

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 50h R: 51h	0	1	0	1	0	0	0	R/$\overline{W}$
I/O Data	RSVD	AX	AR1	AR0	DRL	RSVD	RSVD	RSVD

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

AX: Transmit Analog Gain

0*: 0 dB gain
1: 6.02 dB gain

AR[1:0]: Receive Analog Loss

00*: 0 dB loss
01: 6.02 dB loss
10: 6.02 dB gain
11: RSVD

DRL: Digital Receive Loss. This mode is used in high current metering applications in combination with the 6.02 dB AR gain.

0*: No digital receive loss
1: A 6.02 dB loss is inserted in the voice receive path.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

52/53h Write/Read Input/Output Data Register

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 52h R: 53h	0	1	0	1	0	0	1	R/$\overline{W}$
I/O Data	RSVD	RSVD	IO6	IO5	IO4	IO3	IO2	IO1

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

IO1-IO6: Value at general purpose IO pins.

This register provides both data input and data output functions depending on the setting of the corresponding IOD bits in *54/55h Write/Read Input/Output Direction Register*. The data written appears latched on the I/O pin. In input mode, the logic state of the I/O pin is read. In output mode, the state of the I/O pin is read. A logic 1 written to the data register will cause the output to be logic 1. If the IOD1x bits = 10, then the I/O1 pin is an open drain output capable of driving a relay. A logic 1 written to the data register will cause the output to pull low (current flows in the open drain transistor). In this case, a read of IO1 will read the IO pin voltage and invert the outcome. Thus, in open drain, if the pin voltage is logic low, the system will read back a one.

54/55h Write/Read Input/Output Direction Register

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 54h R: 55h	0	1	0	1	0	1	0	R/$\overline{W}$
I/O Data	EXTPDT	IOD6	IOD5	IOD4	IOD3	IOD2	IOD12	IOD11

EXPDT: External Period Detect

0*: Period detector connected to polarity detector.
1: Period detector connected to IO4.

IOD1[2:1]: Direction of the IO1 pins (input or output)

00*: IO1 is an input
01: IO1 is an output
10: IO1 is open drain
11: Reserved

IOD2-6: Direction of the IO2-6 pins (input or output)

0*: IOx is an input
1: IOx is an output

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

56/57h Write/Read System State

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 56h R: 57h	0	1	0	1	0	1	1	R/$\overline{W}$
I/O Data	RSVD	RSVD	ACT	RSVD	SS3	SS2	SS1	SS0

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

ACT: Activate Codec

0*: Codec deactivated
1: Codec Activated

No valid PCM data is transmitted until after the third FS pulse is received after the ACT bit is set.

SS[3:0]: System State is defined by the table below. The Le88010 device utilizes two system states in combination with the ACT bit to implement the necessary System States in combination with I/O1 being used for on/off hook control. This produces 3 effective system states, Shutdown, Idle (Supervision Enabled with Codec deactivated) used when on hook, and Active (Supervision Enabled with Codec activated) which is used while off hook and for caller ID reception. All other states are reserved.

SS3	SS2	SS1	SS0	Mode
1*	1*	1*	1*	Shutdown
1	0	0	1	Supervision Enabled
All other combinations				RSVD

Notes:

1. *Where there is a conflict on a write to this register between the System State (SS) and the other bits, the other bits take precedence Power Up and Hardware Reset ($\overline{RST}$) Value = 0Fh*

60/61h Write/Read Operating Functions

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 60h R: 61h	0	1	1	0	0	0	0	R/$\overline{W}$
I/O Data	C/L	A/µ	EGR	EGX	EX	ER	EZ	EB

C/L: Linear Code

0*: Compressed coding
1: Linear coding

A/µ: A-law or µ-law

0*: A-law coding
1: µ-law coding

EGR: GR Filter

0*: Default GR filter enabled
1: Programmed GR filter enabled

EGX: GX Filter

0*: Default GX filter enabled
1: Programmed GX filter enabled

EX: X Filter

0*: Default X filter enabled
1: Programmed X filter enabled

ER: R Filter

0*: Default R filter enabled
1: Programmed R filter enabled

EZ: Z Filter

0*: Default Z filter enabled
1: Programmed Z filter enabled

EB: B Filter

0*: Default B filter enabled
1: Programmed B filter enabled

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

68/69h Write/Read System State Configuration

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 68h R: 69h	0	1	1	0	1	0	0	R/$\overline{W}$
I/O Data	RSVD	RSVD	ACFS	RSVD	RSVD	RSVD	ASSC	RSVD

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

ACFS: Automatic Clock Fail Switching

0: Automatic Clock Fail switching disabled

1*: Automatic Clock Fail switching enabled
When a Clock Fail alarm is detected and persists for between 0.5 ms and 3 ms the channel will switch to the Shutdown state.

ASSC: Automatic System State Control

0*: Automatic system state switching enabled
System State will change due to the following supervision stimuli
In the Supervision Enabled state, incoming ringing detect (RNGDT) will change state to Active, Supervision Enabled, and set the IO1 bit to take the system off hook

1: Automatic system state switching disabled
State changes only occur as a result of user commands

*Power Up and Hardware Reset ($\overline{RST}$) Value = 20h.

6C/6Dh Write/Read Interrupt Mask Register

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 6Ch R: 6Dh	0	1	1	0	1	1	0	R/$\overline{W}$
I/O Data Byte 1	MCFAIL	MPOL	MPOH	MIO2	MCAD	MDIS	MRNGDT	MLIU
I/O Data Byte 2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

In the MPI mode, this register defines which signals can generate interrupts and be latched in the *4D/4Fh Read Signaling Register*, on page 50. In GCI mode, this register defines which signals can cause the SLCX bit to be set in the upstream signaling channel. In GCI mode, MRNGDT, MLIU should always be masked.

RSVD: Reserved for future use. Always write as 1, but 1 is not guaranteed when read.

Mx: Mask Interrupt/Signaling bits

0: Signal is NOT masked, change will generate an interrupt or set SLCX

1*: Signal is masked, a change does not cause an interrupt or set SLCX

This command does not depend on the state of the Channel Enable Register.

*Power Up and Hardware Reset ($\overline{RST}$) Value = FFFFh.

70/71h Write/Read Operating Conditions

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 70h R: 71h	0	1	1	1	0	0	0	R/$\overline{W}$
I/O Data	CTP	CRP	HPF	LRG	RSVD	ILB	RSVD	TON

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

CTP: Cutoff Transmit Path

0*: Transmit path connected

1: Transmit path cut off

CRP: Cutoff Receive Path

0*: Receive path connected
1: Receive path cutoff

HPF: High Pass Filter

0*: Transmit Highpass filters enabled
1: Transmit Highpass filters disabled

LRG: Lower Receive Gain

0*: 6-dB loss not inserted
1: 6-dB loss inserted

ILB: Interface Loopback

0*: TSA loopback disabled
1: TSA loopback enabled

TON: 1 kHz Receive Tone

0*: 1 kHz receive tone off
1: 1 kHz receive tone on

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

73h Read Revision and Product Code Number (RCN,PCN)

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R: 73h	0	1	1	1	0	0	1	1
Output Data Byte 1	RCN7	RCN6	RCN5	RCN4	RCN3	RCN2	RCN1	RCN0
Output Data Byte 2	PCN7	PCN6	PCN5	PCN4	PCN3	PCN2	PCN1	PCN0

This command returns an 8-bit number (RCN) describing the revision number of the device and an 8-bit product code number indicating the VE880 series part number.

The revision code (RCN) of the Le88010 Rev. AAA device is 01h.

PCN: Product Code Number

06h Le88010 device

This command does not depend on the state of the Channel Enable Register.

80/81h Write/Read GX Filter Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 80h R: 81h	1	0	0	0	0	0	0	R/$\overline{W}$
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + (C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190h (H_{GX} = 1 (0 dB)).

Note:
The default value is contained in a ROM register separate from the programmable coefficient RAM and the ROM register's default value can not be read. There is a filter enable bit in Operating Functions register to switch between the default and programmed values.

82/83h Write/Read GR Filter Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 82h R: 83h	1	0	0	0	0	0	1	R/$\overline{W}$
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The coefficient for the GR filter is defined as:

$$H_{GR} = C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0111h (H_{GR} = 1 (0 dB)).

See note under Command 80/81h on page 56

86/87h Write/Read B Filter FIR Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 86h R: 87h	1	0	0	0	0	1	1	R/$\overline{W}$
I/O Input Data Byte 1	C32	m32			C22	m22		
I/O Input Data Byte 2	C12	m12			C33	m33		
I/O Input Data Byte 3	C23	m23			C13	m13		
I/O Input Data Byte 4	C34	m34			C24	m24		
I/O Input Data Byte 5	C14	m14			C35	m35		
I/O Input Data Byte 6	C25	m25			C15	m15		
I/O Input Data Byte 7	C36	m36			C26	m26		
I/O Input Data Byte 8	C16	m16			C37	m37		
I/O Input Data Byte 9	C27	m27			C17	m17		
I/O Input Data Byte 10	C38	m38			C28	m28		
I/O Input Data Byte 11	C18	m18			C39	m39		
I/O Input Data Byte 12	C29	m29			C19	m19		
I/O Input Data Byte 13	C310	m310			C210	m210		
I/O Input Data Byte 14	C110	m110			RSVD	RSVD		

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The Z-transform equation for the B filter is defined as:

$$H_B(z) = B_2 \bullet z^{-2} + \ldots + B_9 \bullet z^{-9} + \frac{B_{10} \bullet z^{-10}}{1 - B_{11} \bullet z^{-1}}$$

Sample rate = 16 kHz

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

For i = 2 to 10,

$$B_i = C1i \bullet 2^{-mli}[1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i})]$$

The feedback coefficient of the IIR B section is defined as:

$$B_{11} = C111 \bullet 2^{-m111}\{1 + C211 \bullet 2^{-m211}[1 + C311 \bullet 2^{-m311}(1 + C411 \bullet 2^{-m411})]\}$$

Refer to Command 96/97h for programming of the B_{11} coefficients.

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0900 9009 0090 0900 9009 0090 0900h

$$H_B(z) = 0$$

See note under Command 80/81h on page 56.

88/89h Write/Read X Filter Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 88h R: 89h	1	0	0	0	1	0	0	R/$\overline{W}$
I/O Input Data Byte 1	C40	m40			C30	m30		
I/O Input Data Byte 2	C20	m20			C10	m10		
I/O Input Data Byte 3	C41	m41			C31	m31		
I/O Input Data Byte 4	C21	m21			C11	m11		
I/O Input Data Byte 5	C42	m42			C32	m32		
I/O Input Data Byte 6	C22	m22			C12	m12		
I/O Input Data Byte 7	C43	m43			C33	m33		
I/O Input Data Byte 8	C23	m23			C13	m13		
I/O Input Data Byte 9	C44	m44			C34	m34		
I/O Input Data Byte 10	C24	m24			C14	m14		
I/O Input Data Byte 11	C45	m45			C35	m35		
I/O Input Data Byte 12	C25	m25			C15	m15		

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The Z-transform equation for the X filter is defined as:

$$H_x(z) = x_0 + x_1z^{-1} + x_2z^{-2} + x_3z^{-3} + x_4z^{-4} + x_5z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the X filter are defined as:

$$Xi = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0111 0190 0190 0190 0190 0190h

($H_X(z) = 1$)

See note under Command 80/81h on page 56.

8A/8Bh Write/Read R Filter Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 8Ah R: 8Bh	1	0	0	0	1	0	1	R/$\overline{W}$
I/O Input Data Byte 1	C46	m46			C36	m36		
I/O Input Data Byte 2	C26	m26			C16	m16		
I/O Input Data Byte 3	C40	m40			C30	m30		
I/O Input Data Byte 4	C20	m20			C10	m10		
I/O Input Data Byte 5	C41	m41			C31	m31		
I/O Input Data Byte 6	C21	m21			C11	m11		
I/O Input Data Byte 7	C42	m42			C32	m32		
I/O Input Data Byte 8	C22	m22			C12	m12		
I/O Input Data Byte 9	C43	m43			C33	m33		
I/O Input Data Byte 10	C23	m23			C13	m13		
I/O Input Data Byte 11	C44	m44			C34	m34		
I/O Input Data Byte 12	C24	m24			C14	m14		
I/O Input Data Byte 13	C45	m45			C35	m35		
I/O Input Data Byte 14	C25	m25			C15	m15		

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

$$HR = H_{IIR} \bullet H_{FIR}$$

The Z-transform equation for the IIR filter (RI) is defined as:

$$H_{IIR} = \frac{1 - z^{-1}}{1 - \left(R_6 \bullet z^{-1}\right)}$$

Sample rate = 8 kHz

The coefficient for the IIR filter is defined as:

$$R_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}[1 + C36 \bullet 2^{-m36}(1 + C46 \bullet 2^{-m46})]\}$$

R6 should normally not be set to unity. If it is required to generate DC levels through the receive path from the PCM, the CRP bit (*70/71h Write/Read Operating Conditions*) should be set 5ms before writing R6 to unity. The RTP bit can then be reset and DC or low frequency signals passed from the PCM.

The Z-transform equation for the FIR filter is defined as:

$$H_{FIR}(z) = R_0 + R_1 z^{-1} + R_2 z^{-2} + R_3 z^{-3} + R_4 z^{-4} + R_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the R2 filter are defined as:

$$R_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 2E01 0111 0190 0190 0190 0190 0190h

(H_{FIR} (z) = 1, R_6 = 0.9902)

See note under Command 80/81h on page 56.

96/97h Write/Read B Filter IIR Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 96h R: 97h	1	0	0	1	0	1	1	R/$\overline{W}$
I/O Data Byte 1	C411	m411			C311	m311		
I/O Data Byte 2	C211	m211			C111	m111		

This function is described in command *86/87h Write/Read B Filter FIR Coefficients*, on page 57

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190h (B_{11} = 0)

See note under Command 80/81h on page 56.

98/99h Write/Read Z Filter FIR Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 98h R: 99h	1	0	0	1	1	0	0	R/$\overline{W}$
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		
I/O Data Byte 3	C41	m41			C31	m31		
I/O Data Byte 4	C21	m21			C11	m11		
I/O Data Byte 5	C42	m42			C32	m32		
I/O Data Byte 6	C22	m22			C12	m12		
I/O Data Byte 7	C43	m43			C33	m33		
I/O Data Byte 8	C23	m23			C13	m13		
I/O Data Byte 9	C44	m44			C34	m34		
I/O Data Byte 10	C24	m24			C14	m14		

This function is described in command *9A/9Bh Write/Read Z Filter IIR Coefficients*, on page 60

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190h

($H_Z(z)$ = 0)

9A/9Bh Write/Read Z Filter IIR Coefficients

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: 9Ah R: 9Bh	1	0	0	1	1	0	1	R/$\overline{W}$
I/O Data Byte 1	C45	m45			C35	m35		
I/O Data Byte 2	C25	m25			C15	m15		
I/O Data Byte 3	C26	m26			C16	m16		
I/O Data Byte 4	C47	m47			C37	m37		
I/O Data Byte 5	C27	m27			C17	m17		

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0 to 5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 01 0190h

($H_Z(z) = 0$)

See note under Command 80/81h on page 56.

Note:

Z_6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of $1/Z_6$, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z_6 to normalize the overall gain. Z_5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial $1/Z_6$ gain. The theoretical effective IIR gain, without the Z_6 gain and normalization, is actually Z_5/Z_6.

A6/A7h Write/Read Converter Configuration

Command	D7	D6	D5	D4	D3	D2	D1	D0
W: A6 R: A7h	1	0	1	0	0	1	1	R/$\overline{W}$
I/O Data	ATI	DRAT2	DRAT1	DRAT0	SEL3	SEL2	SEL1	SEL0

ATI: Arm Transmit PCM data Interrupt.

0*: Transmit Data Ready interrupt disabled.
1: Transmit Data Ready interrupt enabled

When ATI is 1, the interrupt pin will go active when the XDATA becomes available in *CDh Read Transmit PCM/Test Data*, on page 63. The interrupt will be cleared automatically after 54us (or when the data is read from the XDAT register).

DRAT[2:0]: Data rate at which the converter data is updated.

The sampled data is output on the PCM highway and in register *CDh Read Transmit PCM/Test Data*, on page 63, as defined below. The ATI interrupt will also occur at this data rate if unmasked.

000*: 8 kHz
001: 4 kHz
010: 2 kHz
011: 1 kHz
100: 500 Hz
101: Reserved
110: Reserved
111: Reserved

SEL[3:0]: This register selects the transmit path analog input source

The bits SEL3 - SEL0 select which input is routed to the A/D converter and hence which measurement shows up at the PCM highway and in register *CDh Read Transmit PCM/Test Data*, on page 63. All unspecified codes are reserved.

SEL3	SEL2	SEL1	SEL0	Value written to measurement register	Operating Range	Scale
0*	0*	0*	0*	VINP - VINM input voltage	-3.40 V to 3.40 V	104 µV
0	1	0	0	Tip Voltage to ground	TBD V	TBD mV
0	1	0	1	Ring Voltage to ground	TBD V	TBD mV
0	1	1	0	Tip - Ring Metallic DC coupled Voltage	TBD V	TBD mV
1	0	0	1	Calibration Current (IREF)	-25 µA to 25 µA	2.27 nA
1	0	1	0	Voice DAC Analog Loopback	-1.53 V to 1.53 V	46.8 µV
1	0	1	1	No connection - read ADC output offset 1.	-3.44 V to 3.44 V	105 µV
1	1	0	1	Tip Voltage to ground Low Scale	TBD V	TBD mV
1	1	1	0	Ring Voltage to ground Low Scale	TBD V	TBD mV

1. The ADC output offset is defined relative to the default metallic AC coupled tip-ring voltage.
2. Operating ranges assume the standard external application circuit component values are used.

The operating range values may be less than the full scale ranges of the output. The scale assumes register *60/61h Write/Read Operating Functions* = 80 h, register *50/51h Write/Read Voice Path Gains* = 00 h and register *CA/CBh Write/Read Digital Impedance Scaling Network (DISN)* = 00 h.

The voltage and current scales define the typical values and do not imply a specific accuracy for the measurement path and A/D converter. The absolute accuracy of the measurement paths can be found in the electrical specification section.
A full digital loop back from the digital input through the DAC to the ADC and back to the digital output is achieved by making the connection to the voice DAC. The nominal gain of this path is 3.44 / 1.53 = 7.04 dB.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

C2/C3h Write/Read Loop Supervision Parameters

Command	D7	D6	D5	D4	D3	D2	D1	D0
W: C2h R: C3h	1	1	0	0	0	0	1	R/$\overline{W}$
I/O Data Byte 1	RDAOVR	RSVD	TDIS2	TDIS1	TDIS0	TLIU2	TLIU1	TLIU0
I/O Data Byte 2	DDIS2	DDIS1	DDIS0	DLIU4	DLIU3	DLIU2	DLIU1	DLIU0
I/O Data Byte 3	TMINP7	TMINP6	TMINP5	TMINP4	TMINP3	TMINP2	TMINP1	TMINP0
I/O Data Byte 4	TMAXP7	TMAXP6	TMAXP5	TMAXP4	TMAXP3	TMAXP2	TMAXP1	TMAXP0

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

RDAOVR: Ringing Detect Amplitude Override

0: Amplitude detector and period detector both contribute to ringing detect output.
1: Only period detector contributes to ringing detect output.

TDIS[2:0]: Disconnect Threshold; 0 - 10V with a step of 1.4 volts
(default = 011b = 4.2 V)

TLIU[2:0]: Line In Use and Ring Detect threshold; 16 - 91V with a scale of 11 V/step
(default = 010b = 38 V)

DDIS[2:0]: Disconnect debounce; 0–28 ms, with a scale of 4 ms/step
(default = 100b = 16 ms)
Going from on-hook to disconnect, the debounce time will be

DLIU+DDIS.

DLIU[4:0]: Line In Use debounce interval; 0–62 ms, with a scale of 2 ms/step (default = 00100b = 8 ms)

TMINP[7:0]: Minimum Period Threshold. Lower limit threshold for period to be above. Condition is satisfied if the time between alternate pulses is greater than TMINP. (0 - 63.75 ms with a scale of 0.25 ms). If the EXPDT bit is set, the TMAXP applies to the time between successive pulses. (default = 85h =33.35 ms)

TMAXP[7:0]: Maximum Period Threshold. Upper limit threshold for period to be below. Condition is satisfied if the time between alternate pulses is less than TMAXP. (0 - 63.75 ms with a scale of 0.25 ms). A ringing detect interrupt is generated if the measured half period is between TMINP and TMAXP and the amplitude threshold requirement is met. If the EXPDT bit is set, the TMAXP applies to the time between successive pulses. (default = FFh = 63.75 ms)

Note that the stated thresholds assume the standard external application circuit component values are connected to RDC and TDC pins.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 1A84 85FFh

CA/CBh Write/Read Digital Impedance Scaling Network (DISN)

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: CAh R: CBh	1	1	0	0	1	0	1	R/$\overline{W}$
I/O Data	DISN7	DISN6	DISN5	DISN4	DISN3	DISN2	DISN1	DISN0

DISN[7:0]: Digital Impedance scaling network two's complement gain value.

The DISN gain can be varied from -1.0 to 0.992 in steps of 0.0078. A value of 0 removes the DISN from the impedance loop.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

CDh Read Transmit PCM/Test Data

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R: CDh	1	1	0	0	1	1	0	1
Output Data Byte 1	XDAT15	XDAT14	XDAT13	XDAT12	XDAT11	XDAT10	XDAT9	XDAT8
Output Data Byte 2	XDAT7	XDAT6	XDAT5	XDAT4	XDAT3	XDAT2	XDAT1	XDAT0

XDAT: Read signal Value.

XDAT[7:0] Contains A-law or μ-law transmit data in Companded mode.
XDAT[15:0] Contains upper and lower data bytes in Linear mode with sign in XDAT15.

In test mode, as defined by command *A6/A7h Write/Read Converter Configuration*, on page 61, the A/D converter is connected either to the voice path (codec bypass), or to other signals as defined by the SEL bits. In this case the XDAT[0-15] bits indicate the measured value of the variable connected to the A/D converter in 1.15 format. The maximum values and scales are given in the chart. Negative Tip, Ring and battery voltages are reported as positive values.

This register input is sampled data at a default 8KSa/sec rate (set by DRAT in command *A6/A7h Write/Read Converter Configuration*, on page 61) and the register is updated at the programmed data rate. A new measurement may be made by writing the converter configuration register. An interrupt can be generated every time this register is updated by setting the ATI bit in *6C/6Dh Write/Read Interrupt Mask Register*, on page 55. The signal may be sampled by the user as fast as 8KSa/sec in this mode.

To get meaningful DC test data, the codec high pass filter in *70/71h Write/Read Operating Conditions*, on page 55 must be disabled and the compression should be set to linear in *60/61h Write/Read Operating*

Functions, on page 54. To achieve the specified accuracies, the ADC offset voltage should first be read by selecting the 'No connection' option and subtracting this result from subsequent measurements.

While this register can be read in GCI mode, the monitor channel protocol only allows this data to be sampled at a slow rate. It is recommended that the compressed B channel data is read directly from the GCI bus in this mode.

D2/D3h Write/Read Signal Generator A and B Parameters

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: D2h R: D3h	1	1	0	1	0	0	1	R/$\overline{W}$
I/O Byte 1	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
I/O Byte 2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
I/O Byte 3	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
I/O Byte 4	RSVD	FRQA14	FRQA13	FRQA12	FRQA11	FRQA10	FRQA9	FRQA8
I/O Byte 5	FRQA7	FRQA6	FRQA5	FRQA4	FRQA3	FRQA2	FRQA1	FRQA0
I/O Byte 6	AMPA15	AMPA14	AMPA13	AMPA12	AMPA11	AMPA10	AMPA9	AMPA8
I/O Byte 7	AMPA7	AMPA6	AMPA5	AMPA4	AMPA3	AMPA2	AMPA1	AMPA0
I/O Byte 8	RSVD	FRQB14	FRQB13	FRQB12	FRQB11	FRQB10	FRQB9	FRQB8
I/O Byte 9	FRQB7	BRQA6	FRQB5	FRQB4	FRQB3	FRQB2	FRQB1	FRQB0
I/O Byte 10	AMPB15	AMPB14	AMPB13	AMPB12	AMPB11	AMPB10	AMPB9	AMPB8
I/O Byte 11	AMPB7	AMPB6	AMPB5	AMPB4	AMPB3	AMPB2	AMPB1	AMPB0

RSVD — Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

FRQA[14:0]: Frequency/slope parameter of signal generator A
FRQA is an unsigned number with a frequency step size of 0.3662 Hz.
The maximum allowable frequency is 3400 Hz. The signal generator runs through the voice path which has internal filters and a sampling rate of 8KSa/sec.
(default = 0037h = 20.1Hz)

AMPA[15:0]: Amplitude parameter of signal generator A
Up to +3.14 dBm0 into the voice path
AMPA is the peak value of the digital sine wave.
A positive value will start the wave at 0 with a positive initial first derivative (wave goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down).
(default = 4AA4h = -1.55dBm0)

FRQB[14:0]: Frequency parameter of signal generator B
FRQB is an unsigned number with a frequency step size of 0.3662 Hz.
The maximum allowable frequency is 3400 Hz. The signal generator runs through the voice path which has internal filters and a sampling rate of 8KSa/sec.
(default = 0000h)

AMPB[15:0]: Amplitude parameter of signal generator B
Up to +3.14 dBm0 into the voice path
AMPB is the peak value of the digital sine wave.
A positive value will start the wave at 0 with a positive initial first derivative (wave goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down).

(default = 0000h)

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00 0000 0037 4AA4 0000 0000h

DE/DFh Write/Read Signal Generator Control

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: DEh R: DFh	1	1	0	1	1	1	1	R/$\overline{W}$
I/O Data	SGCAD	CNTOS	EGDP	RSVD	RSVD	RSVD	EGB	EGA

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

SGCAD: Signal Generator Cadencing

0*: No Signal generator cadencing

1: The enabled tone generators specified by EGA - EGDP will cadence on and off as determined by command *E0/E1h Write/Read Cadence Timer*, on page 66

The EGx bits will read back zero in the cadence off time.

This command makes use of the cadence timer. The enabled functions are toggled at a rate specified by the cadence timer. The CAD bit in command *4D/4Fh Read Signaling Register*, on page 50 is set at the end of the on period, which can optionally generate an interrupt if MCAD is reset in command *6C/6Dh Write/Read Interrupt Mask Register*, on page 55. At this time, the user may write new values into the cadence timer and reissue the signal generator control command.

If no enable bits are set, the cadencer will run and will still set the CAD bit at the end of the on period and can produce an interrupt. In this way, the cadencer can be used as a system timer.

CNTOS: Continuous or One Shot cadence operation.

0*: Continuous cadencing. Cadencing will continue until the user intervenes.

1: One shot. The generators will turn on for one on period only. The dial pulse relay driver will turn off (no current flows) for one on period. All enable bits and SGCAD will be set to zero after the off period. An interrupt will be sent at the end of the on period.

EGDP: Enable Dial Pulse Generation

0*: Dial Pulse generation disabled

1: Dial Pulse generation enabled

Dial pulsing is performed by toggling IO1.

EGB: Enable Signal Generator B

0*: Generator B disabled

1: Generator B enabled

EGA: Enable Signal Generator A

0*: Generator A disabled

1: Generator A enabled

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

E0/E1h Write/Read Cadence Timer

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W: E0h R: E1h	1	1	1	0	0	0	0	R/$\overline{W}$
I/O Byte 1	RSVD	RSVD	RSVD	RSVD	RSVD	CADON10	CADON9	CADON8
I/O Byte 2	CADON7	CADON6	CADON5	CADON4	CADON3	CADON2	CADON1	CADON0
I/O Byte 3	RSVD	RSVD	RSVD	RSVD	RSVD	$CADOFF_{10}$	$CADOFF_9$	$CADOFF_8$
I/O Byte 4	$CADOFF_7$	$CADOFF_6$	$CADOFF_5$	$CADOFF_4$	$CADOFF_3$	$CADOFF_2$	$CADOFF_1$	$CADOFF_0$

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

CADON[10:0]: Cadence On Time. 0 - 10.24 seconds with a scale of 5 ms per step. (default* = 190h = 2 sec)

CADOFF[10:0]: Cadence Off Time. 0 - 10.24 seconds with a scale of 5 ms per step. (default* = 320h = 4 sec)

During the ring off time, the system state is Active.

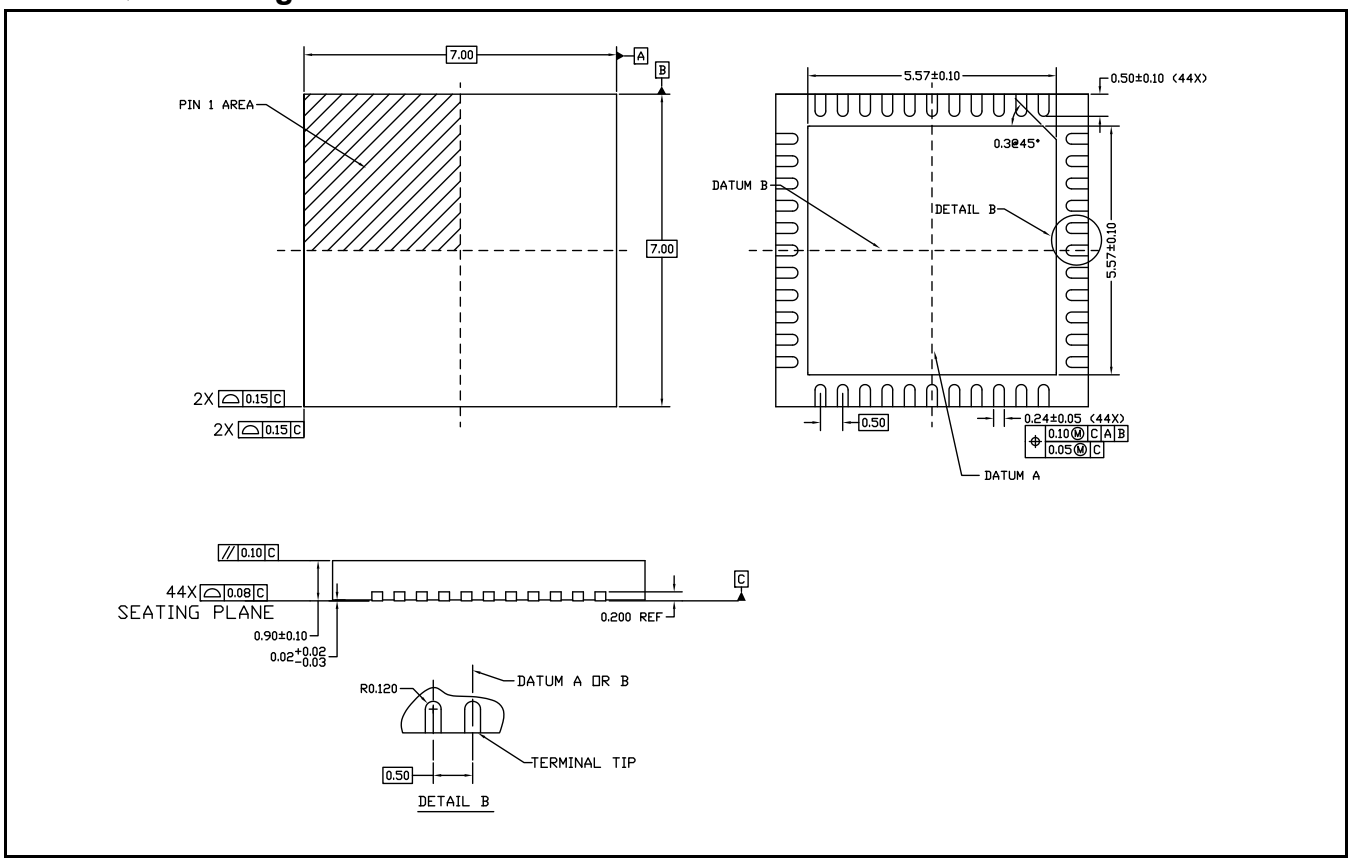
If the cadence off time is 0, the function will be enabled indefinitely.

The cadencer is a shared timer that is used for a variety of functions including; dial pulse generation, and tone pulsing e.g. DTMF dialling.The on and off times are set by this command and the individual commands for these functions enable the cadencer.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 0190 0320h

PHYSICAL DIMENSIONS

44-Pin QFN Package



Notes:

1. *Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.*

REVISION HISTORY

Revision A1 to B1

- Updated Connection Diagram to show larger exposed pad.
- Updated 44-pin QFN package outline drawing
- Removed TSCA pin function and all references, and reassigned pin as an additional DGND
- Enhanced $\overline{\text{INT}}$ pin to support S2 GCI packet assignment function
- Product will only be available in a “green” package.
- Converter Configuration signal sense accuracies and ranges updated, and Note 3 added.
- CS off time increased from 500ns to 2500ns.
- Added mode to allow device to function at slower rate by operating on free running internal clock when external clocks are not present
- Added DAT bit to the signaling register
- Added ATI and DRAT bits to converter configuration register

Revision B1 to B2

- Updated application circuit in Figure 34, on page 45.
  - Corrected connection of C_{NTS} to the drain of Q1.
- Updated *Physical Dimensions*, on page 67 to reflect changes in exposed pad and pin pad dimensions.

Revision B2 to B3

- Added note to *Physical Dimensions*
- Added new headers/footers due to Microsemi purchase of Legerity on August 3, 2007

Revision B3 to B4

- Migrated to Microsemi format.
- Replaced all instances of Zarlink with Microsemi.
- The workaround for Device Errata C.1 in L88010 Voiceport SLAC Device - Revision C, Document 081618 Revision A, Version 2 September 24, 2007 is now the permanent fix to Errata.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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