PL611-31-xxx

Programmable Quick Turn Clock

Revision 2.0

General Description

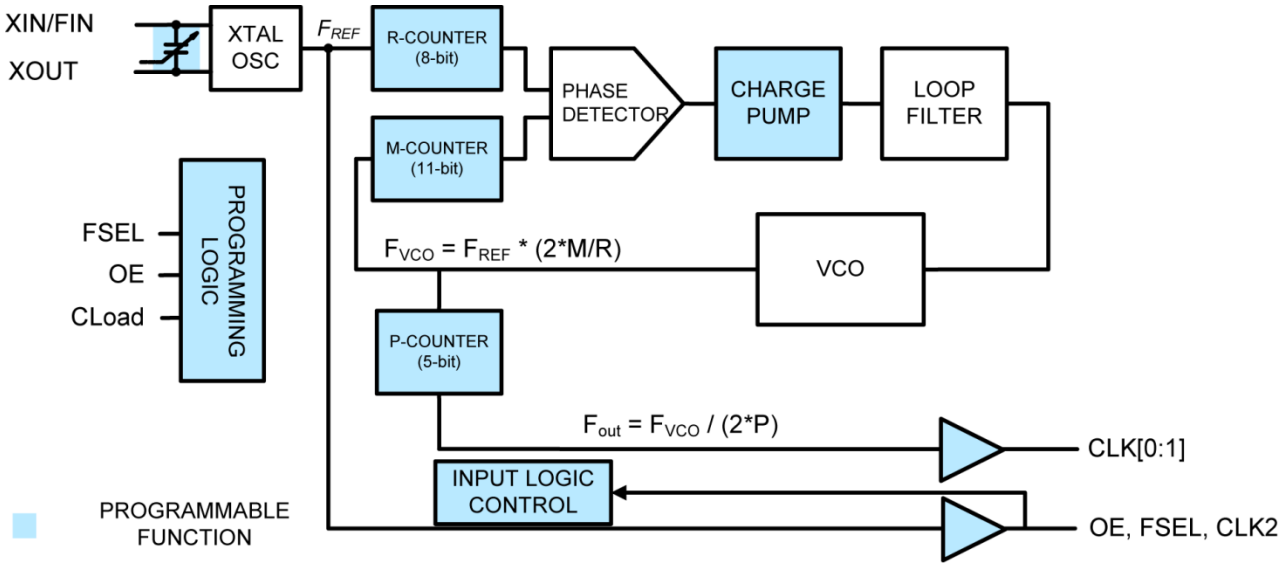
The PL611-31-xxx is a low-cost, general purpose frequency synthesizer and a member of Micrel's factory-programmable Quick Turn Clock (QTC) family. The PL611-31-xxx product family can generate any output frequency up to 200MHz from a fundamental crystal input of 10MHz to 30MHz. In addition, the complementary LVCMOS outputs can be used to drive differential LVPECL, LVDS, HCSL or CML inputs at 2.5V or 3.3V.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

Features

- Advanced programmable PLL design
- Very low jitter and phase noise (<40ps peak-to-peak typical)
- Up to 3 outputs
- Output frequency up to 200MHz CMOS
  - Provides complementary LVCMOS outputs to drive LVCMOS, LVPECL, LVDS, HCSL or CML inputs
- Input frequencies:
  - Fundamental crystal: 10MHz – 30MHz
  - Reference clock: 1MHz – 200MHz
- Accepts <1.0V reference signal input voltage
- One programmable I/O pin can be configured as output enable (OE) input, frequency selection (FSEL) input, or reference clock output
- Single 2.5V ~ 3.3V ±10% power supply
- Operating temperature range from –40°C to +85°C
- Available in 8-pin SOICN, GREEN/RoHS-compliant package

Block Diagram



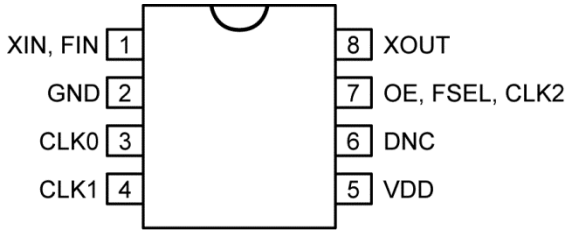
Ordering Information

Part Number[1, 2]	Marking[2]	Junction Temp. Range	Package
PL611-31-xxxUZZ	P611-31 XXX LLLLL	0° to +70°C	8-Pin SOICN (Tube)
PL611-31-xxxUZZ TR	P611-31 XXX LLLLL	0° to +70°C	8-Pin SOICN (Tape and Reel)
PL611-31-xxxUZY	P611-31 XXXI LLLLL	–40° to +85°C	8-Pin SOICN (Tube)
PL611-31-xxxUZY TR	P611-31 XXXI LLLLL	–40° to +85°C	8-Pin SOICN (Tape and Reel)

Note:

1. Other voltages are available. Contact Micrel for details.
2. xxx: Micrel will assign a unique 3-digit ID code for each approved programmed part number.
   LLLL: IC lot number

Pin Configuration



8-Pin SOICN

Pin Description

Pin Number	Pin Name	Type	Description
1	XIN, FIN	I	Crystal or reference input pin
2	GND	P	GND connection
3, 4	CLK[0:1]	O	Programmable clock output [note: CLK0 = CLK1]
5	VDD	P	VDD connection (2.25V~3.63V)
6	DNC		Do not connect
7	OE, FSEL, CLK2	B	This programmable I/O pin can be configured as output enable (OE) input, frequency select (FSEL) input, or CLK2 (=F_{IN}) output. This pin has an internal 60kΩ pull-up resistor.
8	XOUT	O	Crystal output pin

State	OE	FSEL
0	Tristate CLK[0:1]	Bank 0
1 (default)	Normal mode	Bank 1

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Key Programming Parameters

CLK[0:2] Output Frequency	Output Drive Strength	Crystal Load	Programmable Input/Output (pin 7)	Number of Register Banks
$F_{OUT} = F_{IN} \times M \div (R \times P)$ where M = 10-bit R = 8-bit P = 5-bit 1. CLK[0:1] = VCO÷(2×P) 2. CLK0 = ~CLK1 3. CLK[2] = F_{IN}	Standard: 10mA (default) High: 24mA	±200ppm tuning	One output can be configured as: • CLK2 output • FSEL input • OE input	2

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Absolute Maximum Ratings[3]

Supply Voltage (V_{DD}) ..... –0.5V to +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ..... –0.5V to V_{DD}+0.5V
Data Retention (at +85°C) ..... 10 Years
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (Ts) ..... –60°C to +150°C
ESD Rating[5] 2kV

Operating Ratings[4]

Supply Voltage (V_{DD}) ..... +2.25V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
SOICN (θ_{JA}) ..... 99°C/W

AC Electrical Characteristics[6]

V_{DD} = 3.3V; C_L = 15pF; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Crystal Input Frequency	Fundamental crystal	10		30	MHz
(F_{IN}) Input Frequency		1		200	MHz
(F_{IN}) Input Signal Amplitude	AC-coupled externally: add capacitor in series with F_{IN}	0.8		V_{DD}	V_{PP}
(F_{IN}) Input Signal Low Level, V_{IL}	DC coupled CMOS signal into F_{IN}			30% V_{DD}	
(F_{IN}) Input Signal High Level, V_{IH}	DC coupled CMOS signal into F_{IN}	70% V_{DD}			
Output Frequency		5		200	MHz
Settling Time	At power-up (V_{DD} ≥ 2.25V)			10	ms
VDD Sensitivity	Frequency vs. V_{DD} ±10%	–2		2	ppm
Output Rise Time	15pF load, 10/90% V_{DD}, standard drive		2.5	3.5	ns
	15pF load, 10/90% V_{DD}, high drive		1.0	1.5	ns
	Differential, resistive load, 20/80%, high drive		0.3	0.5	ns
Output Fall Time	15pF load, 90/10% V_{DD}, standard drive		2.5	3.5	ns
	15pF load, 90/10% V_{DD}, high drive		1.0	1.5	ns
Duty Cycle	At V_{DD}/2	45	50	55	%
Output Skew between CLK0 and CLK1	Equal loading (15pF), equal drive strength			200	ps
Period Jitter, peak-to-peak[7] (10,000 samples measured)	With capacitive decoupling between V_{DD} and GND. Crystal = 27MHz, CLK[0:1] = 148.5MHz.			60	ps

Notes:

3. Exceeding the absolute maximum ratings may damage the device.
4. The device is not guaranteed to function outside its operating ratings.
5. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
6. Specification for packaged product only
7. Jitter performance depends on the programming parameters.

DC Electrical Characteristics[6]

V_{DD} = 3.3V; C_L = 15pF; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply Current, Dynamic, with Loaded Outputs	At CLK0=CLK1=10MHz, both loaded with 15pF, V_{DD}=3.3V			15	mA
V_{DD}	Operating Voltage		2.25		3.63	V
I_{OSD}	Output Current, standard drive	V_{OL} = 0.4V, V_{OH} = V_{DD} - 0.9V, V_{DD} = 3.3V		10		mA
I_{OHD}	Output Current, high drive	V_{OL} = 0.4V, V_{OH} = V_{DD} - 0.9V, V_{DD} = 3.3V		24		mA
I_S	Short-Circuit Current			±50		mA

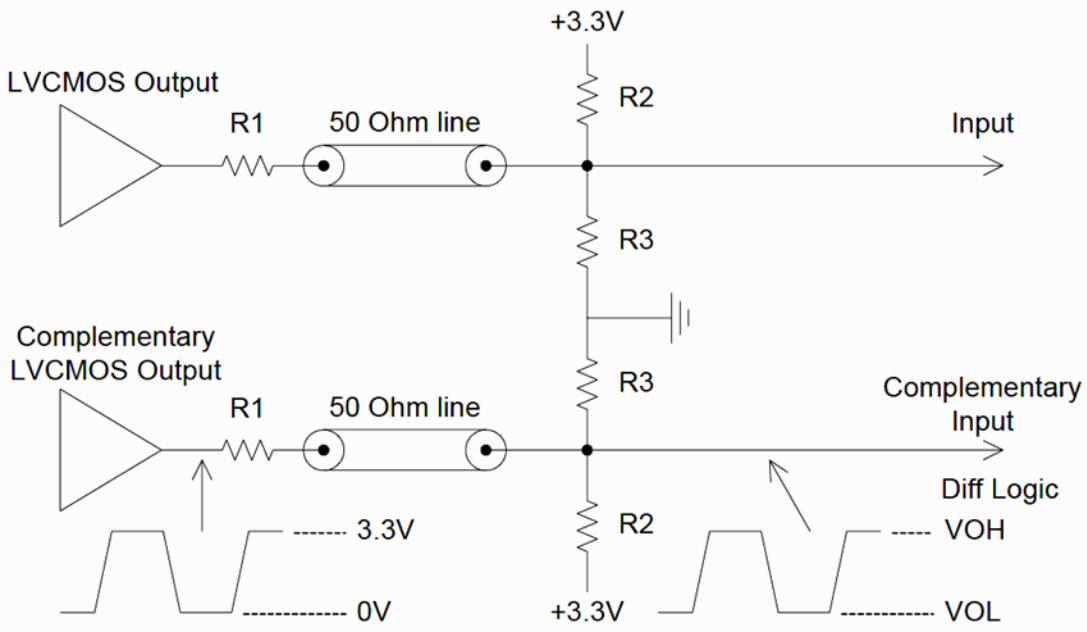
Crystal Specifications

Symbol	Parameter	Min.	Typ.	Max.	Units
F_{XIN}	Fundamental crystal resonator frequency	10		30	MHz
$C_{L\ (XTAL)}$	Crystal loading rating (The IC can be programmed for any value in this range)	5		20	pF
	Maximum sustainable drive level			500	µW
	Operating drive level		100		µW
C0	Crystal shunt capacitance			6	pF
ESR	Effective series resistance, fundamental, 10MHz to 30MHz			30	Ω

Terminating Complementary LVCMOS Outputs

The figure below describes how to terminate the complementary LVCMOS outputs of the PL611-31-xxx programmable clock for use with LVPECL, LVDS, HCSL, or CML inputs.

The unique feature of complementary LVCMOS outputs allows great flexibility for board designers. By standardizing on one termination scheme, the PL611-31-xxx can be used for all LVPECL, LVDS, HCSL, and CML clock requirements up to 400MHz.



The layout above allows the PL611-31-xxx to drive several types of differential inputs by simply changing the values of R1, R2, and R3.

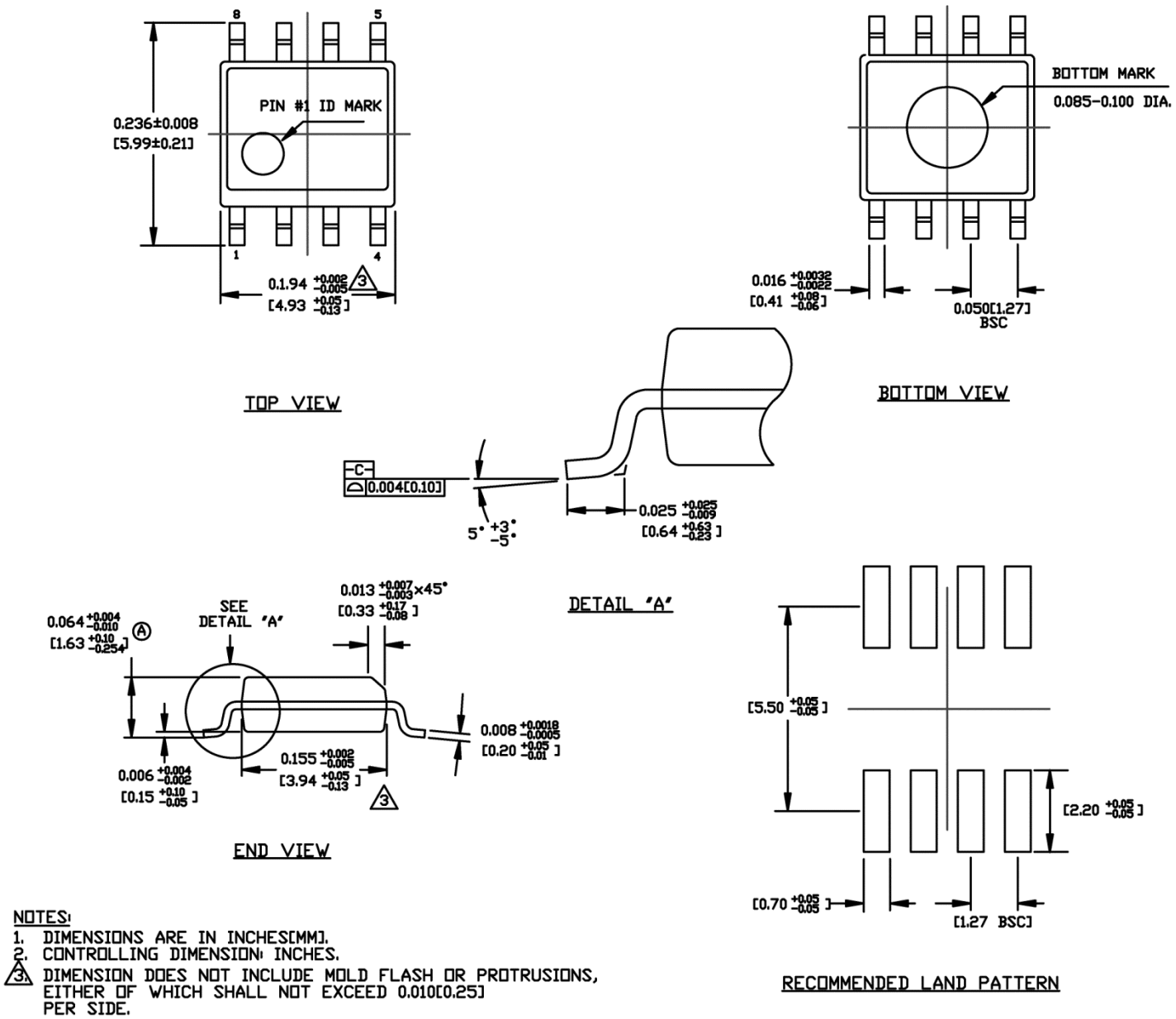
Recommended R1, R2 and R3 Values:

Logic	VDD	R1	R2	R3	VOL	VOH
HCSL	2.5V	100Ω	None	50Ω	0.00V	0.75V
	3.3V	150Ω	None	50Ω		
CML	2.5V	240Ω	50Ω	None	V_{DD}-0.40V	V_{DD}
	3.3V	330Ω	50Ω	None		
LVPECL	2.5V	82Ω	110Ω	91Ω	V_{DD}-1.71V	V_{DD}-0.95V
	3.3V	130Ω	82Ω	130Ω		
LVDS	2.5V	240Ω	100Ω	100Ω	1.10V	1.40V
	3.3V	360Ω	130Ω	82Ω		

Place R1 as close to the LVCMOS outputs as possible.

Place R2 and R3 as close to the target differential inputs as possible.

Package Information[8]



8-Pin SOICN

Note:

8. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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