0.5kHz-125MHz, MHz to KHz Programmable Clock™

FEATURES

- Designed for Very Low-Power applications
- Input Frequency, AC Coupled:
  - Reference Input: 1MHz to 125MHz
  - Accepts >0.1V input signal voltage
- Output Frequency up to 125MHz LVCMOS
  - ≤65MHz @ 1.8V operation
  - ≤90MHz @ 2.5V operation
  - ≤125MHz @ 3.3V operation
- One programmable input pin can be configured as Power Down (PDB) input, output Enable (OE), or Frequency Selection Switching input
- Disabled outputs Active Low
- Low current consumption:
  - <1.0mA with 27MHz & 32kHz outputs
  - <5µA when PDB is activated
- Single 1.8V ~ 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN, and SOT23 GREEN/RoHS compliant packages

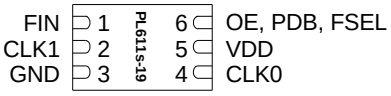
DESCRIPTION

The PL611s-19 is a low-cost general purpose frequency synthesizer and a member of 'Quick Turn Clock (QTC)' family. PL611s-19 offers the versatility of using a single reference clock input and producing up to two (kHz or MHz) system clock outputs. Designed for low-power applications with very stringent space requirement, PL611s-19 consumes ~1.0mA, while producing 2 distinct outputs of 27MHz and 32kHz. The power down feature of PL611s-19, when activated, allows the IC to consume less than 5µA of power.

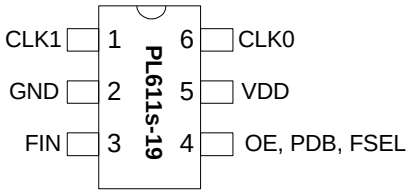
The PL611s-19 fits in a small DFN or SOT23 package. Cascading of the PL611s-19 with other programmable clocks allow generating system level clocking requirements, thereby reducing the overall system implementation cost.

In addition, one programmable input pin can be configured as Power Down (PDB) input, Output Enable (OE), or Frequency switching (FSEL). The CLK1 output can be programmed as FREF or CLK0.

PIN CONFIGURATIONS

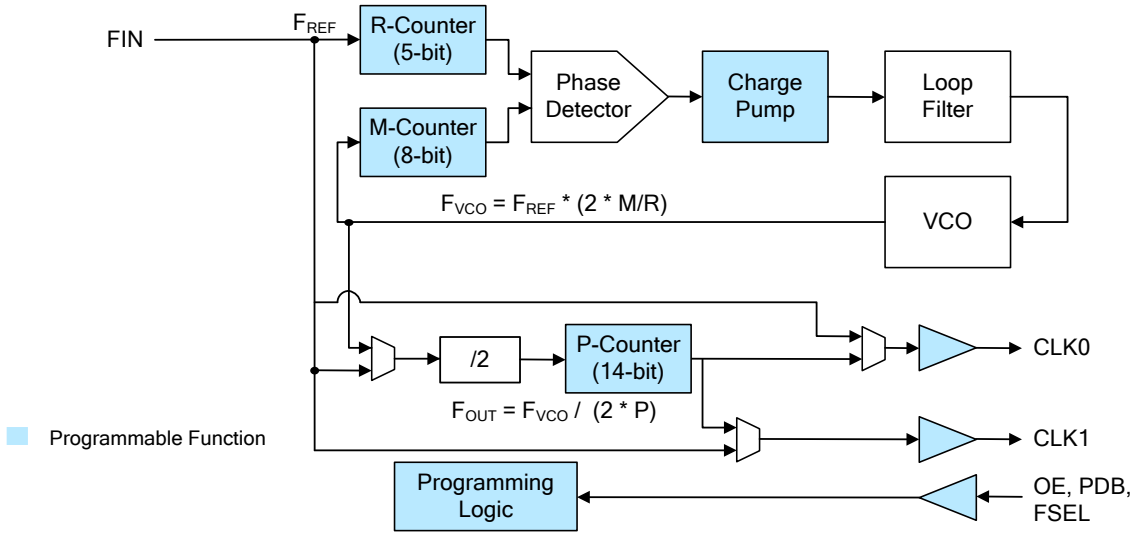


DFN-6L
(2.0 x 1.3 x 0.6mm)



SOT23-6L
(3.0 x 3.0 x 1.35mm)

BLOCK DIAGRAM



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KEY PROGRAMMING PARAMETERS

CLK Output Frequency	Output Drive Strength	Programmable Input
$F_{OUT} = F_{REF} * M / (R * P)$ Where M = 8 bit R = 5 bit P = 14 bit CLK0 = F_{OUT}, F_{REF} or F_{REF} / (2*P) CLK1 = F_{REF} or CLK0	Two optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default)	One output pin can be configured as: • OE - input • FSEL - input • PDB – input

PIN DESCRIPTIONS

Name	Pin Assignment			Type	Description
	DFN Pin#	SC70 Pin#	SOT Pin #		
CLK1	2	1	1	I/O	Programmable Clock Output
GND	3	5	2	P	GND connection
FIN	1	3	3	I	Reference input pin
OE, PDB, FSEL	6	2	4	O	This programmable input pin can be configured as an Output Enable (OE) input, Power Down input (PDB) or On-the-Fly Frequency Switching Selector (FSEL). This pin has an internal pull up resistor for OE, PDB & FSEL.
VDD	5	4	5	P	VDD connection
CLK0	4	6	6	O	Programmable Clock Output

OE AND PDB FUNCTION DESCRIPTION

OE	PDB	Osc.	PLL	CLK0	CLK1	
					When CLK1=F_{REF}	When CLK1=CLK0
1(Default)	N/A	On	On	On	On	On
0	N/A	On	Off	Active Low	On	Active Low
N/A	1(Default)	On	On	On	On	On
N/A	0	Off	Off	Active Low	Active Low	Active Low

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FUNCTIONAL DESCRIPTION

PL611s-19 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-19 accepts a reference clock input of 1MHz to 125MHz and is capable of producing two outputs from 0.5kHz to 125MHz. This flexible design allows the PL611s-19 to deliver any PLL generated frequency, FREF (Ref Clock) frequency or FREF/(2*P) to CLK0 and/or CLK1. Some of the design features of the PL611s-19 are mentioned below:

PLL Programming

The PLL in the PL611s-19 is fully programmable. The PLL is equipped with an 5-bit input frequency divider (R-Counter), and an 8-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 14-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * M / (R * P)].

Clock Output (CLK0)

The output of CLK0 can be configured as the PLL output (F_{VCO}/(2*P)), FREF (Ref Clk Frequency) output, or FREF/(2*P) output. The output drive level can be programmed to Low Drive (4mA) or Standard Drive (8mA). The maximum output frequency is 125MHz @ 3.3V, 90MHz @ 2.5V or 65MHz @ 1.8V.

Clock Output (CLK1)

The output of CLK1 can be configured as:

FREF – Reference (Ref Clock) Frequency
CLK0 – PLL Derived Frequency

The output drive level can be programmed to Low Drive (4mA) or Standard Drive (8mA). The maximum output frequency is 125MHz @ 3.3V, 90MHz @ 2.5V or 65MHz @ 1.8V.

Programmable Input Pin (OE/PDB/FSEL)

The PL611s-19 provides one programmable I/O pin which can be configured as one of the following functions:

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the CLK0 output by toggling the OE pin. Using the OE function the CLK1 clock output will remain on when programmed as FREF and will disable when programmed to CLK0 (See OE and PDB Function Description on page 2). The OE pin incorporates a 60kΩ pull up resistor giving a default condition of logic “1” (Enabled).

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-19 into “Sleep Mode”. When activated (logic ‘0’), PDB ‘Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <5µA of power. The PDB pin incorporates a pull up resistor giving a default condition of logic “1” (Enabled).

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-19 to switch between two pre-programmed outputs allowing the device “On the Fly” frequency switching. The FSEL pin incorporates a 60kΩ pull up resistor giving a default condition of logic “1”.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	@ V_{DD} =3.3V	1		125	MHz
	@ V_{DD} =2.5V			90	
	@ V_{DD} =1.8V			65	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.8		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V	0.5kHz		125	MHz
	@ V_{DD} =2.5V			90	MHz
	@ V_{DD} =1.8V			65	MHz
Settling Time	At power-up (after V_{DD} increases over 90% of operating V_{DD})			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, Std Drive, 3.3V		2.0	3.0	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, Std Drive, 3.3V		2.0	3.0	ns
Duty Cycle	PLL Enabled, @ V_{DD} /2	45	50	55	%
Period Jitter,Pk-to-Pk* (10K samples measured)	Capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	@ V_{DD} =3.3V, 27MHz, load=15pF		4.0		mA
Supply Current, Dynamic	I_{DD}	@ V_{DD} =2.5V, 27MHz, load=10pF		2.7		mA
Supply Current, Dynamic	I_{DD}	@ V_{DD} =1.8V, 27MHz, load=5pF		1.1		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =3.3V, 32kHz, load=15pF		0.6		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =2.5V, 32kHz, load=15pF		0.5		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =1.8V, 32kHz, load=15pF		0.2		mA
Supply Current, Dynamic	I_{DD}	When PDB=0			5	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA

PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to PL611s-19 as short as possible, as well as keeping all other traces as far away from it as possible.

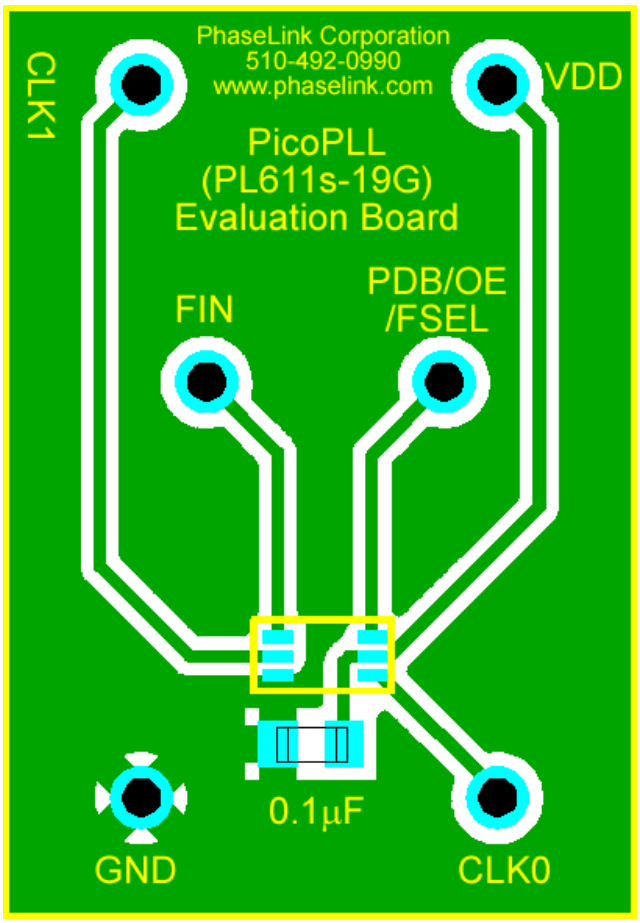
- When a reference input clock is generated from a crystal, place the PL611s-19 'FIN' as close as possible to the 'Xout' crystal pin. This will reduce the cross-talk between the reference input and the other signals.

- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.

- It is highly recommended to keep the VDD and GND traces as short as possible.

- When connecting long traces (> 1 inch) to a LVCMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the LVCMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and LVCMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the LVCMOS output pin to the 'stripline' trace.

- Please contact Micrel for the application note on how to design outputs driving long traces or for additional layout assistance.

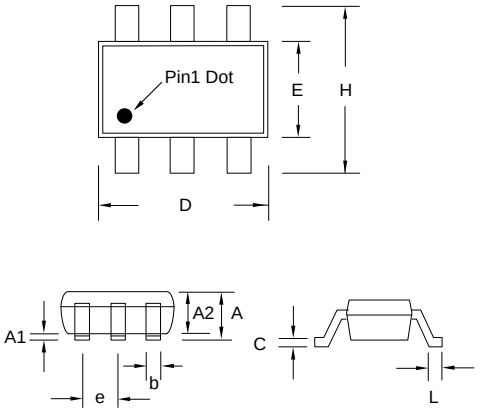


DFN-6L Evaluation Board

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

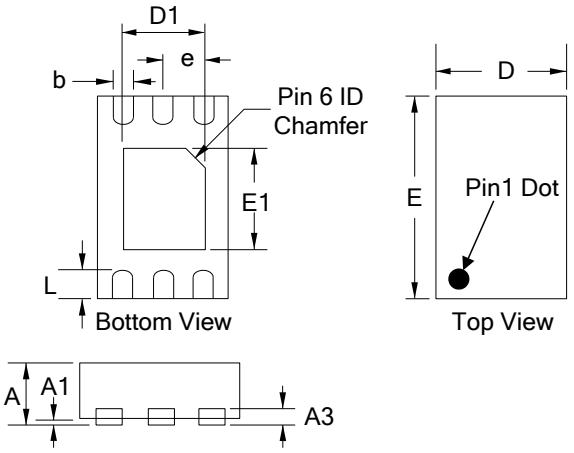
SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-19-XXX X X X

PART NUMBER

3 DIGIT ID Code *
(will be assigned at programming time)

PACKAGE TYPE
G=DFN-6L
T=SOT-6L

R=TAPE and REEL

TEMPERATURE
C=COMMERCIAL (0°C to 70°C)
I = INDUSTRIAL (-40°C to 85°C)

* Micrel will assign a unique 3-digit ID code for each approved programmed part number.

Part /Order Number	Marking†	Package Option
PL611s-19-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-19-XXXTC-R	19XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number.