ATBTLC1000-QFN

Ultra-Low Power BLE ATBTLC1000-QFN Data Sheet

Introduction

The ATBTLC1000 is an ultra-low power Bluetooth® Low Energy (BLE) 5.0 System in a Package (SiP) with Integrated MCU, Transceiver, Modem, Medium Access Controller (MAC), Power Amplifier (PA), Transmit/Receive (T/R) Switch, and Power Management Unit (PMU). It can be used as a BLE link controller, and data pump with external host MCU.

The qualified Bluetooth SIG protocol stack is stored in a dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and Generic Access Profile (GAP). Additionally, example applications are available for application profiles such as proximity, thermometer, heart rate, blood pressure, and many other SIG-defined profiles.

Microchip BluSDK offers a comprehensive set of tools, including reference applications for several Bluetooth SIG-defined profiles and a custom profile. The BluSDK helps the user to quickly evaluate, design and develop BLE products with the ATBTLC1000-QFN. The ATBTLC1000-QFN passed the Bluetooth SIG certification for interoperability with the Bluetooth Low Energy 5.0 specification.

Features

- Compliant with Bluetooth v5.0
- 2.4 GHz Transceiver and Modem
  - -95 dBm/-93 dBm programmable receiver sensitivity
  - -55 to +3.5 dBm programmable TX output power
  - Integrated Transmit/Receive (T/R) switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit Processor
  - Serial Wire Debug (SWD) interface
  - Four-channel Direct Memory Access (DMA) controller
  - Brown-out Detector (BOD) and Power-on Reset (POR)
  - Watchdog Timer
- Memory
  - 128 KB embedded RAM
  - 128 KB embedded ROM
- Hardware Security Accelerators
  - Advanced Encryption Standard (AES)-128
  - Secure Hash Algorithm (SHA)-256
- Peripherals

  - 12 digital and two mixed-signal General Purpose Input Outputs (GPIOs) with 96 kOhm internal programmable pull-up or down resistors and retention capability, and one wake-up GPIO with 96 kOhm internal pull-up resistor(1)
  - Two Serial Peripheral Interface (SPI) master/slave interface(1)
    Two Inter-Integrated Circuit (I_2C) master/slave(1)
  - Two Universal Asynchronous Receiver/Transmitter (UART) interface(1)
  - Three-axis quadrature decoder(1)
  - Four Pulse Width Modulation (PWM) channels(1)
  - Three general purpose timers, and one wake-up timer(1)
  - Two channel 11-bit Analog-to-Digital Converter (ADC)(1)
- Host Interface
  - Host MCU can control through UART with hardware flow control
  - Only two microcontroller GPIO lines necessary
  - One interrupt pin from ATBTLC1000 which can be used for host wake up
- Clock
  - Integrated 26 MHz RC oscillator
  - Integrated 2 MHz RC oscillator
  - 26 MHz crystal oscillator (XO)
  - 32.768 kHz Real Time Clock crystal oscillator (RTC XO)
- Ultra-Low Power
  - 2.01 µA sleep current
  - 3.91 mA peak TX current(2)
  - 5.24 mA peak RX current
  - 15.1 µA average advertisement current(3)
- Integrated Power Management
  - 1.8 V to 4.3 V battery voltage range
  - Fully integrated Buck DC/DC converter
- Temperature Range
  - -40°C to 85°C
- Package
  - 32 pin IC package 4 mm x 4 mm
  - BT SIG QDID: 117593 (https://launchstudio.bluetooth.com/listings/search)

Note:

1. Usage of this feature is not supported by the BluSDK. The datasheet will be updated once support for this feature is added in BluSDK.
2. TX output power - 0 dBm
3. Advertisement channels - 3; Advertising interval - 1 second; Advertising event type - Connectable undirected; Advertisement data payload size - 31 octets.

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1. Ordering Information

The following table provides the ATBTLC1000-QFN ordering information.

Table 1-1. ATBTLC1000-QFN Ordering Information

Model Number	Ordering Code	Package	Description
ATBTLC1000	ATBTLC1000A-MU-T	4 mm x 4 mm QFN 32	ATBTLC1000 Tape and Reel
ATBTLC1000	ATBTLC1000A-MU-Y	4 mm x 4 mm QFN 32	ATBTCL1000 Tray

2. Package Information

The following table provides the ATBTLC1000 4x4 QFN 32 package information.

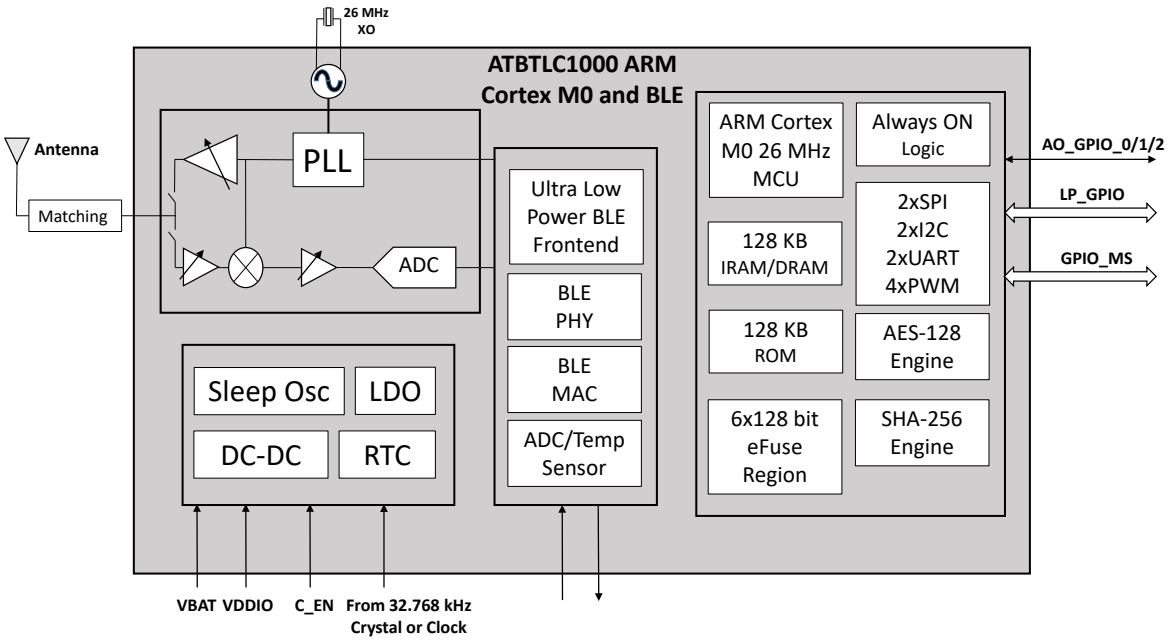
Table 2-1. ATBTLC1000 Package Information

Parameter	Value	Units	Tolerance
Package Size	4 x 4	mm	±0.1
QFN Pad count	32	-	-
Total thickness	0.85	mm	+0.15/-0.05
QFN Pad pitch	0.4		
Pad width	0.2		
Exposed Pad size	2.7 x 2.7		

3. Block Diagram

The ATBTLC1000 block diagram is shown in the following figure.

Figure 3-1. ATBTLC1000 Block Diagram



4. Pinout Information

The ATBTLC1000 is offered in an exposed pad 32-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The following figure shows the QFN package pin assignment. The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – digital I/O power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

Figure 4-1. ATBTLC1000 Pin Assignment

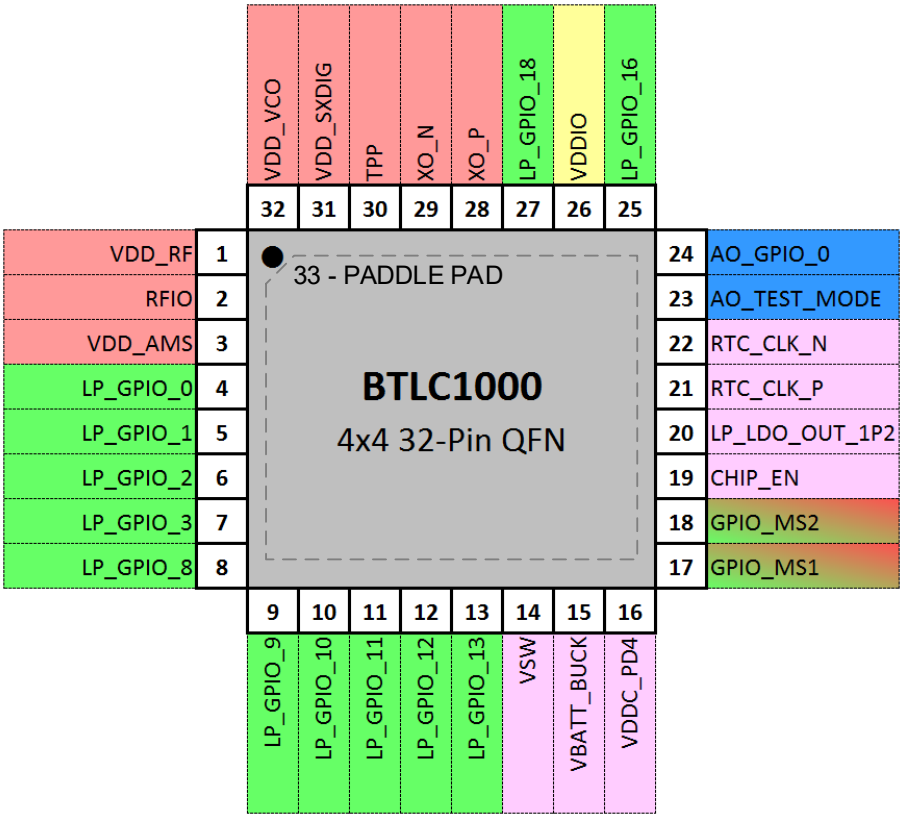


Table 4-1. ATBTLC1000 Pin Description

Pin No.	Pin Name	Pin Type	Description / Default Function
1	VDD_RF	Analog/RF	RF supply 1.2 V
2	RFIO	Analog/RF	RX input and TX output Single-ended RF I/O; To be connected to antenna
3	VDD_AMS	Analog/RF	AMS supply 1.2 V

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Pin No.	Pin Name	Pin Type	Description / Default Function
4	LP_GPIO_0	Digital I/O	SWD clock
5	LP_GPIO_1	Digital I/O	SWD I/O
6	LP_GPIO_2	Digital I/O	UART RXD Default function (6-wire mode): UART1_RXD Alternate (4-wire mode): UART1_RXD
7	LP_GPIO_3	Digital I/O	UART TXD Default function (6-wire mode): UART1_TXD Alternate (4-wire mode): UART1_TXD
8	LP_GPIO_8(1)	Digital I/O	UART_CTS Default function (6-wire mode): GPIO with Programmable Pull Up/Down Alternate (4-wire mode): UART1_CTS
9	LP_GPIO_9(1)	Digital I/O	UART_RTS Default function (6-wire mode): GPIO with Programmable Pull Up/Down Alternate (4-wire mode): UART1_RTS
10	LP_GPIO_10	Digital I/O	SPI SCK/SPI Flash SCK Default function (6-wire mode): UART2_RTS Alternate (4-wire mode): GPIO with Programmable Pull Up/Down
11	LP_GPIO_11	Digital I/O	SPI MOSI/SPI Flash TXD Default function (6-wire mode): UART2_CTS Alternate (4-wire mode): GPIO with Programmable Pull Up/Down
12	LP_GPIO_12	Digital I/O	SPI SSN/SPI Flash SSN Default function (6-wire mode): UART2_TXD Alternate (4-wire mode): GPIO with Programmable Pull Up/Down
13	LP_GPIO_13	Digital I/O	SPI MISO/SPI Flash RXD Default function (6-wire mode): UART2_RXD Alternate (4-wire mode): GPIO with Programmable Pull Up/Down
14	VSW	PMU	DC/DC Converter switching node
15	VBATT_BUCK	Power supply	Power supply pin for the DC/DC convertor
16	VDDC_PD4	PMU	DC/DC converter 1.2V output and feedback node

.....continued

Pin No.	Pin Name	Pin Type	Description / Default Function
17	GPIO_MS1	Mixed Signal I/O	GPIO with Programmable Pull Up/ Down Default function in BluSDK: Host wake-up
18	GPIO_MS2	Mixed Signal I/O	GPIO with Programmable Pull Up/Down
19	CHIP_EN	Digital Input	Can be used to control the state of PMU. High-level enables the module; low-level places module in the power-down mode. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MOhm pull down resistor to ensure a low- level at power-up.
20	LP_LDO_OUT_1P2	PMU	Low power LDO output (connect to 1µF decoupling cap)
21	RTC_CLK_P	Analog	32.768 kHz Crystal pin or External clock supply, see 7.2 32.768 kHz RTC Crystal Oscillator
22	RTC_CLK_N	Analog	Crystal pin, see 7.2 32.768 kHz RTC Crystal Oscillator
23	AO_TEST_MODE	Digital Input	Always On Test Mode. Connect to GND.
24	AO_GPIO_0	Always On Digital I/O	Can be used to wake-up the device from the Ultra_Low_Power mode by the host MCU
25	LP_GPIO_16	Digital I/O	GPIO with Programmable Pull Up/Down
26	VDDIO	Power supply	I/O supply can be less than or equal to VBATT_BUCK
27	LP_GPIO_18	Digital I/O	GPIO with Programmable Pull Up/Down
28	XO_P	Analog/RF	26 MHz Crystal pin or External clock supply, see 7.1 26 MHz Crystal Oscillator
29	XO_N	Analog/RF	26 MHz Crystal pin, see 7.1 26 MHz Crystal Oscillator
30	TPP	Analog/RF	Do not connect
31	VDD_SXDIG	Analog/RF	Synthesizer digital supply 1.2 V
32	VDD_VCO	Analog/RF	Synthesizer VCO supply 1.2 V
Paddle	Paddle pad	Ground	Exposed paddle must be soldered to system ground

Note:

1. These GPIO pads are high-drive pads.

5. Host Microcontroller Interface

This section describes the interface of ATBTLC1000-QFN with the host MCU.

The host interface pins depend on the mode of the device. The ATBTLC1000 can be interfaced with the host MCU in either of the two modes:

- 6-Wire mode (default)
- 4-Wire mode

To configure the device to function in the 4-Wire mode, program the bit 28 of NVM eFuse Bank 5 Block 3. The following figures describe the required hardware interface between host MCU and ATBTLC1000 in both the 6-Wire mode and 4-Wire mode. The interface requires two additional GPIOs and one interrupt pin from the host MCU.

Figure 5-1. Host Microcontroller to ATBTLC1000-QFN Interface - 4-Wire Mode

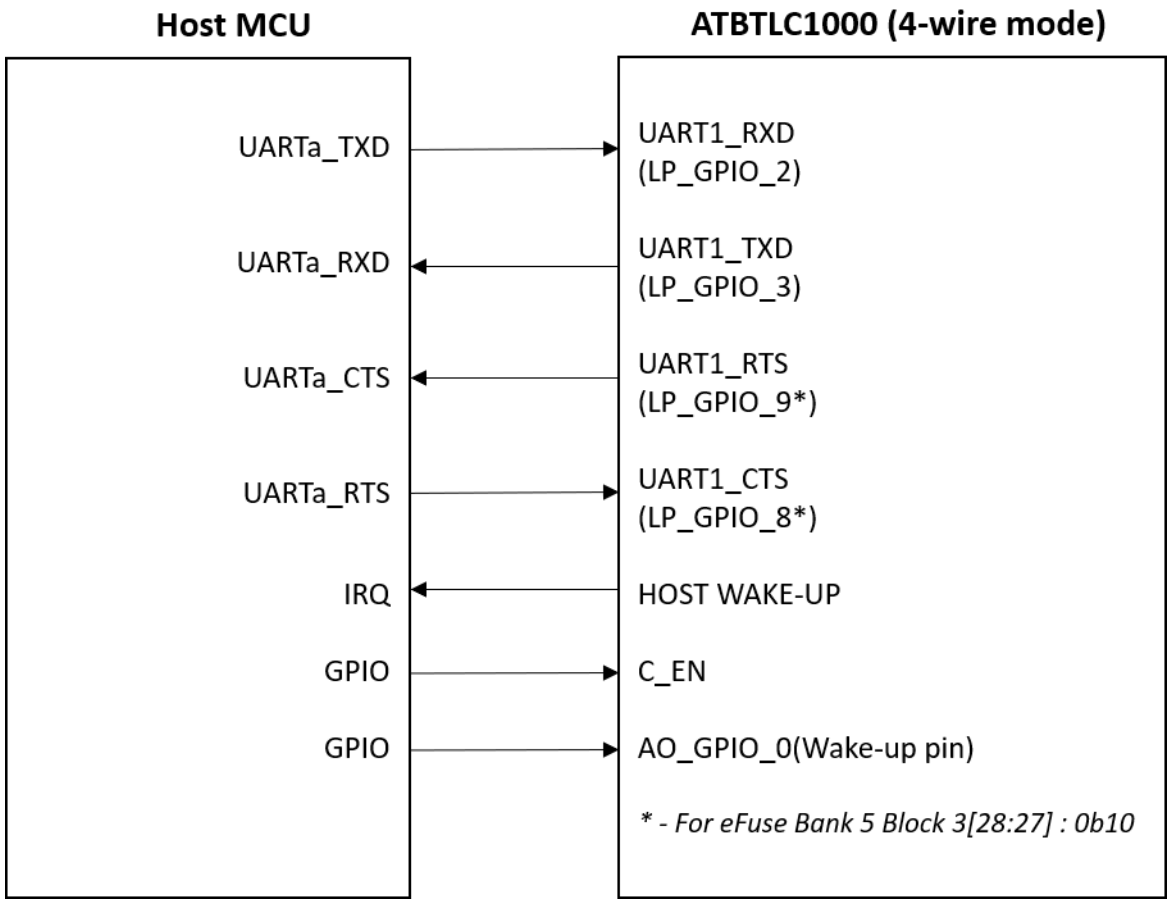
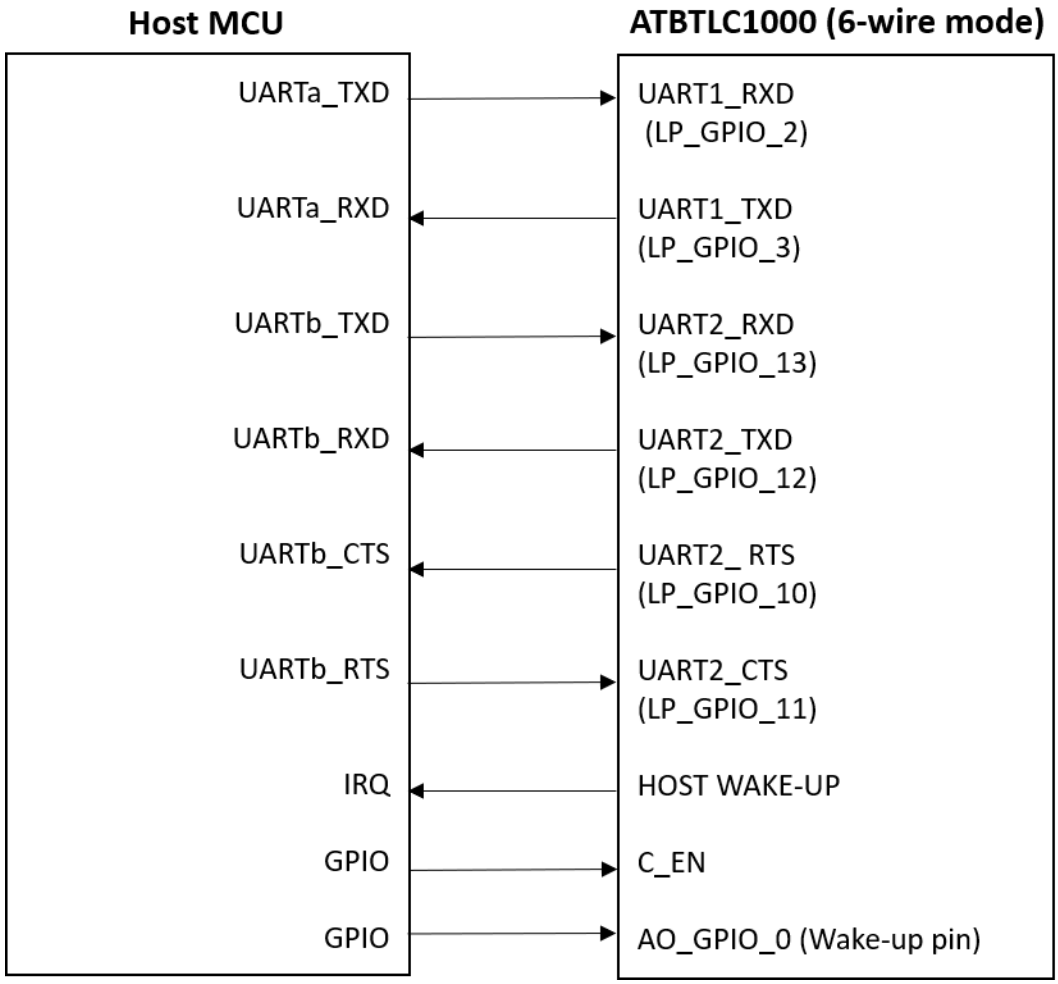


Figure 5-2. Host Microcontroller to ATBTLC1000-QFN Interface - 6-Wire Mode



The host wake-up pin from ATBTLC1000 can be connected to any interrupt pin of the host MCU. The host MCU can monitor this pin level and decide to wake up based on events from ATBTLC1000.

The host wake-up pin will be held in logic high ('1') by default and at conditions where there is no pending event data in the ATBTLC1000. The host wake-up pin will be held in logic low ('0') when there is event data available from ATBTLC1000 and the pin will be held in this state until all event data is sent out from ATBTLC1000. By default in BluSDK, GPIO_MS1 is used as the host wake-up pin. Refer to release notes and API user manual documents available in the BluSDK release package for more details on available options to re-configure the host wake-up pin from ATBTLC1000.

The UART configuration to be used are as below:

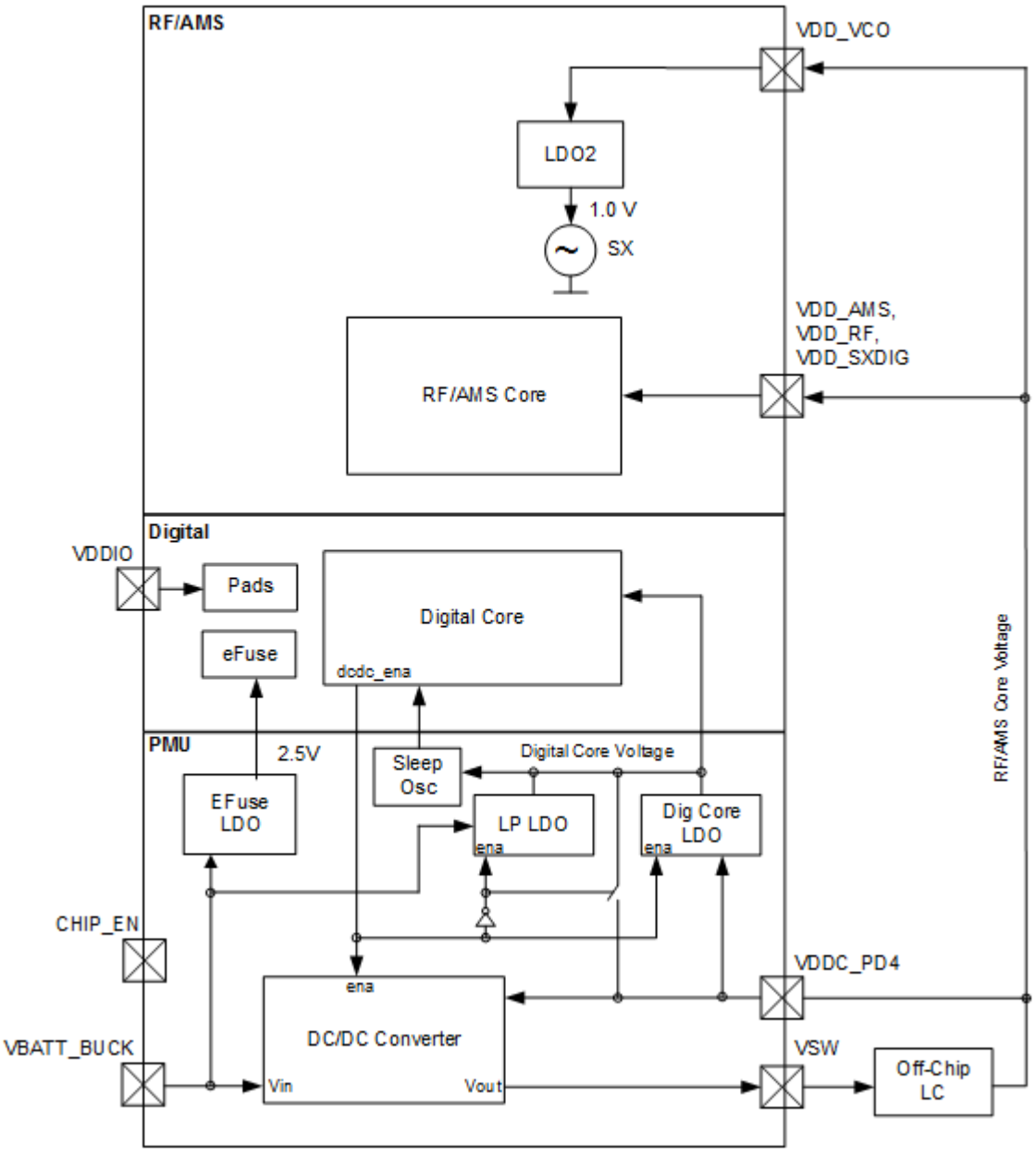
- Baud rate: configurable in the BluSDK during initialization. Refer to release notes and API user manual documents available in the ATBTLC1000 BluSDK Release Package, for more details
- Parity: None
- Stop bits: 1
- Data size: 8 bits

6. Power Management

6.1 Power Architecture

The ATBTLC1000 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The integrated power management block includes a DC/DC buck converter and separate Low Drop Out (LDO) regulators for different power domains. The DC/DC buck converter converts battery voltage to a lower internal voltage for the different circuit blocks with high efficiency. The DC/DC converter requires three external components for proper operation (two inductors (L) 4.7 µH and 9.1 nH, and one capacitor (C) 4.7 µF).

Figure 6-1. ATBTLC1000 Power Architecture



6.2 DC/DC Converter

The DC/DC converter is intended to supply current to the BLE digital core and the RF transceiver core. The DC/DC converter consists of a power switch, 26 MHz RC oscillator, controller, external inductor, and an external capacitor. The DC/DC converter is utilizing the pulse skipping discontinuous mode as its control scheme. The DC/DC converter specifications are shown in the following tables and figures.

Note: The DC/DC converter specifications performance is guaranteed for (L) 4.7µH and (C) 4.7µF.

Table 6-1. DC/DC Converter Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output current capability	I_{REG}	0	10	30	mA	Dependent on external component values and DC/DC converter settings with acceptable efficiency
External capacitor range	C_{EXT}	2	4.7	20	µF	External capacitance range
External inductor range	L_{EXT}	2	4.7	10	µH	External inductance range
Battery voltage	V_{BATT}	1.8	3	4.3	V	Functionality and stability given
Output voltage range	V_{REG}	1.05	1.2	1.47		25 mV step size
Current consumption	I_{DD}	-	125	-	µA	DC/DC quiescent current
Startup time	$t_{startup}$	20	-	600	µs	Dependent on external component values and DC/DC settings
Voltage ripple	ΔV_{REG}	5	10	30	mV	Dependent on external component values and DC/DC settings
Efficiency	η	-	85	-	%	Measured at 3 V VBATT, at load of 10 mA
Overshoot at startup	V_{OS}	-	0	-	mV	No overshoot, no output pre-charge
Line Regulation	ΔV_{REG}	-	10	-		Ranges from 1.8 to 4.3 V
Load regulation	ΔV_{REG}	-	5	-		Ranges from 0 to 10 mA

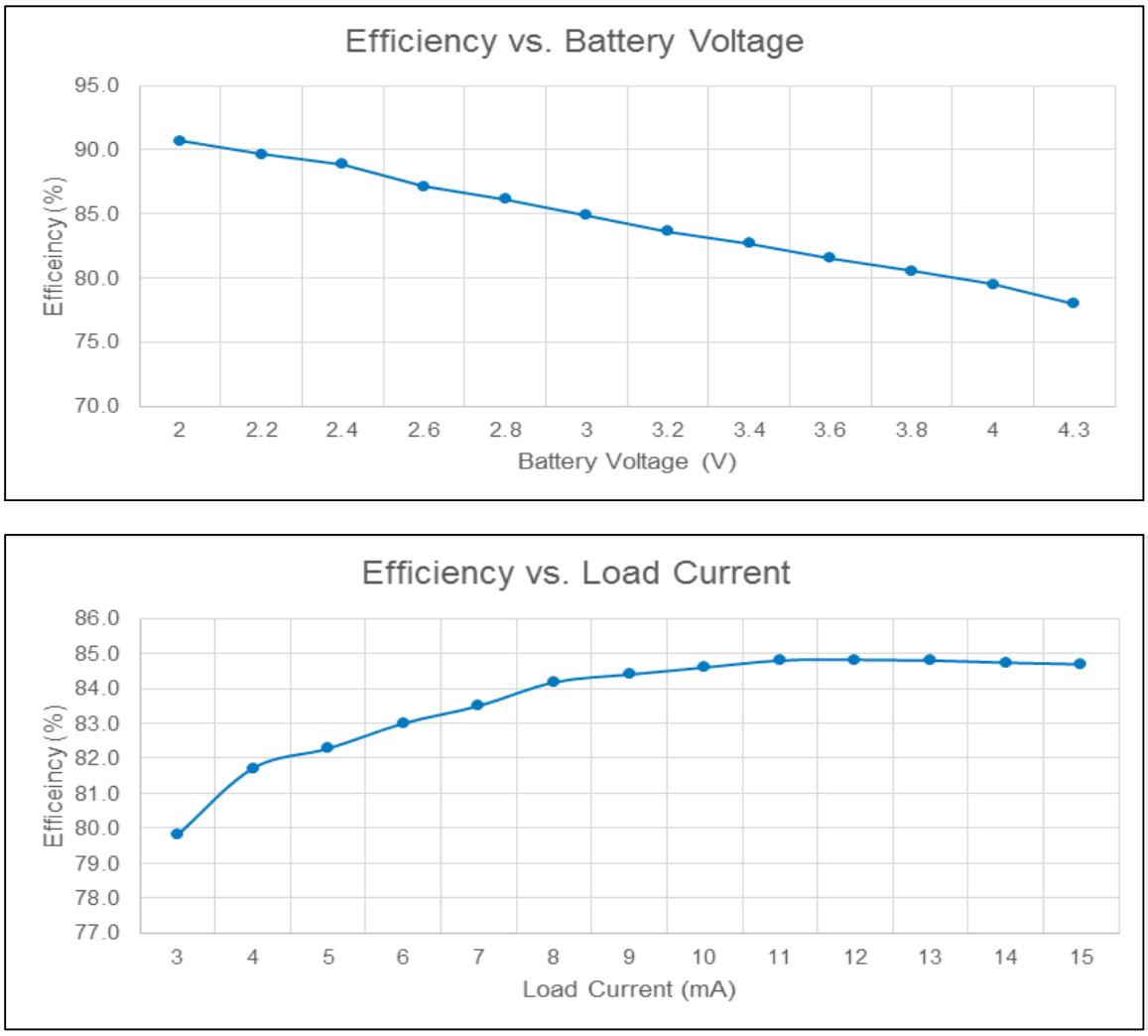
Table 6-2. DC/DC Converter Allowable On-board Inductor and Capacitor Values (VBATT is 3 V)

Inductor [µH]	Efficiency [%]	V_{ripple} [mV]			RX Sensitivity (1) [dBm]
		C at 2.2 µF	C at 4.7 µF	C at 10 µF	
2.2	83	N/A	<5	<5	~1.5 dB degrade
4.7	85	9	5	<5	~0.7 dB degrade

Note:

1. The indicated degradation is relative to an design that is powered by external LDO and with disabled internal DC/DC converter.

Figure 6-2. DC/DC Converter Efficiency



6.3 Device States

This section provides a description of and information about controlling the device states.

6.3.1 Description of Device States

The ATBTLC1000 has multiple device states, depending on the state of the ARM processor and BLE subsystem.

If the BLE subsystem is active, the ARM must be powered on.

- BLE_ON_Transmit – Device actively transmits a BLE signal (irrespective of whether ARM processor is active or not)
- BLE_ON_Receive – Device actively receives a BLE signal (irrespective of whether ARM processor is active or not)
- Ultra_Low_Power – BLE subsystem and ARM processor are powered down (with or without RAM retention)
- Power_Down – Device core supply is powered off

6.3.2 Controlling the Device States

The following pins are used to switch between the main device states:

- CHIP_EN – used to enable PMU
- VDDIO – I/O supply voltage from external supply
- AO_GPIO_0 - used to control the device to enter/exit Ultra_Low_Power mode

In Power_Down state, VDDIO must be ON and CHIP_EN must be set low (at GND level). To exit from the Power_Down state, CHIP_EN must change between logic low and logic high (VDDIO voltage level). Once the device is out of the Power_Down state, all other state transitions are controlled by software. When VDDIO is OFF and CHIP_EN is low, the chip is powered OFF with no leakage.

When power is not supplied to the device (DC/DC converter output and VDDIO are OFF, at ground potential), a voltage cannot be applied to the ATBTLC1000 pins because each pin contains an ESD diode from the pin to supply. This diode turns ON when a voltage higher than one diode-drop is supplied to the pin.

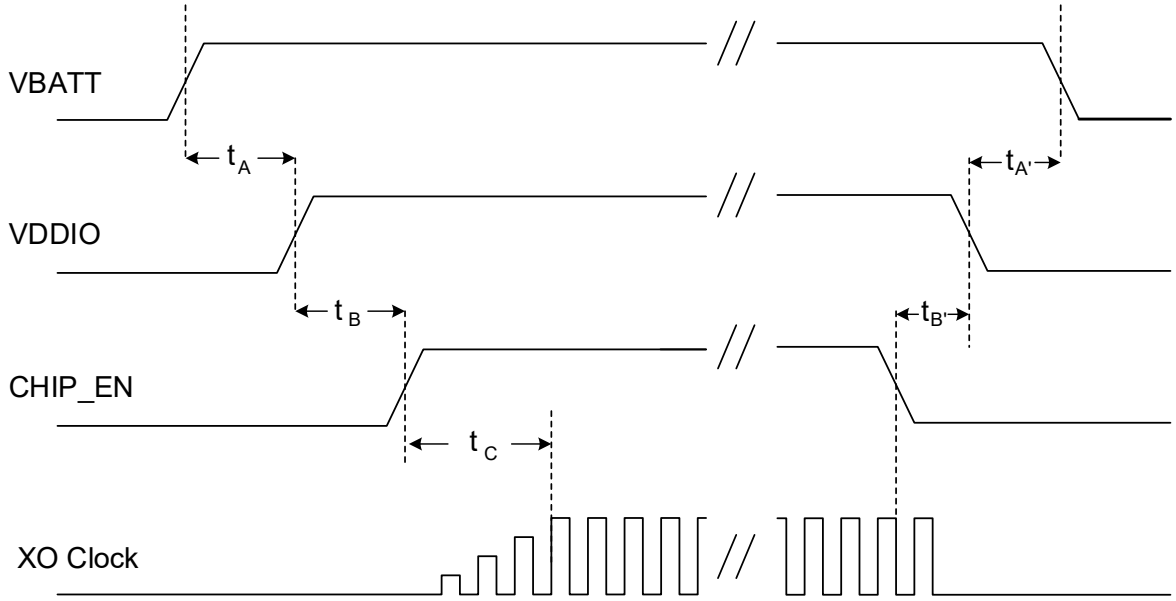
If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be ON, so the Power_Down state is used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below the ground to any pin.

The AO_GPIO_0 pin is used to control the device to enter and exit the Ultra_Low_Power mode. When AO_GPIO_0 is maintained in Logic High state, the device does not enter the Ultra_Low_Power mode. When AO_GPIO_0 is maintained in Logic Low state, the device enters the Ultra_Low_Power mode when there are no BLE events to handle.

6.4 Power-up/Power-down Sequence

The power sequences for ATBTLC1000 are shown in the following figure.

Figure 6-3. ATBTLC1000 Power-up/down Sequence



The timing parameters are provided in the following table.

Table 6-3. ATBTLC1000 Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or connected together.
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, it must not be left floating.
t_C	10		µs	CHIP_EN rise to 31.25 kHz (2 MHz / 64) oscillator stabilizing	
t_A'	0		ms	CHIP_EN fall to VDDIO fall	CHIP_EN must fall before VDDIO. CHIP_EN must be driven high or low, it must not be left floating.
t_B'	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or be tied together.

6.5 Power-on Reset and Brown-out Detector

The ATBTLC1000 has a Power-on Reset (POR) circuit for system power bring up and a Brown-out Detector (BOD) to reset the system operation when a drop in battery voltage is detected.

- The POR circuit output becomes a HIGH logic value when the VBATT_BUCK is below the voltage threshold. The POR output becomes a LOW logic value when the VBATT_BUCK is above the voltage threshold.

- The BOD output becomes a HIGH logic value when the VBATT_BUCK voltage falls below the predefined voltage threshold. The BOD output becomes a LOW logic value when the VBATT_BUCK voltage level is restored above the voltage threshold.
- The counter creates a pulse that holds the chip in reset for 256*(64*T_2 MHz) ~ 8.2 ms.

The following figures illustrate the system block diagram and timing sequence.

Figure 6-4. ATBTLC1000 POR and BOD Block Diagram

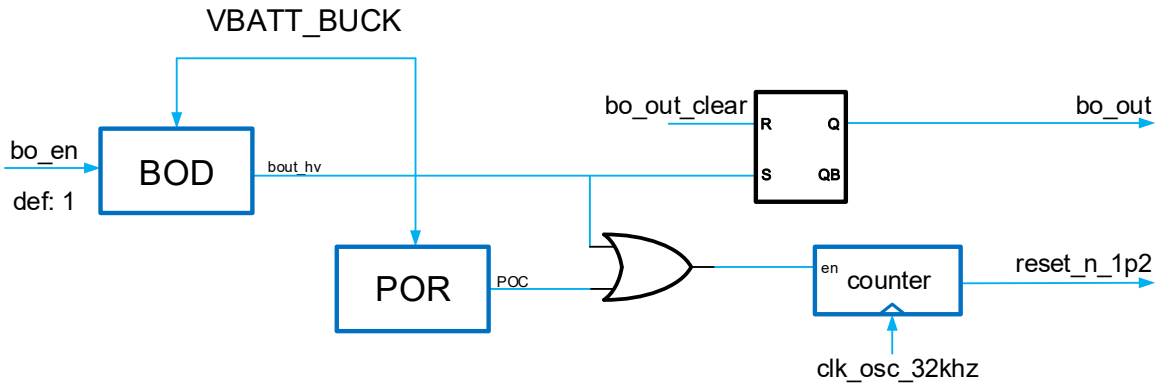
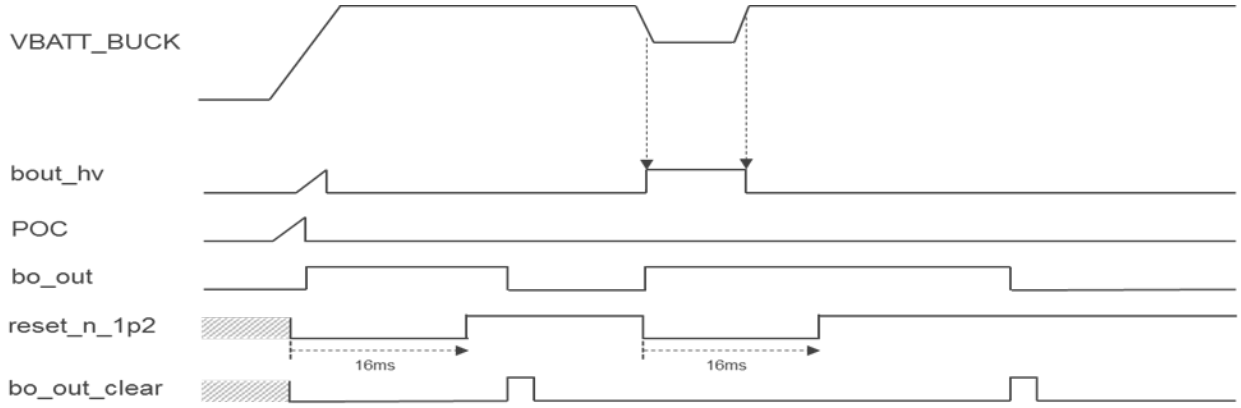


Figure 6-5. ATBTLC1000 POR and BOD Timing Sequence



The following table shows the BOD thresholds.

Table 6-4. ATBTLC1000 BOD Thresholds

Parameter	Min.	Typ.	Max.	Comment
BOD threshold	1.73 V	1.80 V	1.92 V	
BOD threshold temperature coefficient		-1.09 mV/C		
BOD current consumption		300 nA		
t_{POR}		8.2 ms		

6.6 Digital and Mixed-Signal I/O Pin Behavior during Power-Up Sequence

The following table represents I/O pin states corresponding to the device power modes.

Table 6-5. I/O Pin Behavior in Different Device States (1)

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull-Up/Down Resistor (2)
Power_Down: core supply OFF	High	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-on Reset: core supply ON, and POR hard reset pulse ON	High	High	Disabled (Hi-Z)	Disabled	Disabled(3)
Power-on Default: core supply ON, and device out of reset but not programmed	High	High	Disabled (Hi-Z)	Enabled (4)	Enabled Pull-Up(4)
BLE_On: core supply ON, device programmed by firmware	High	High	Programmed by firmware for each pin: Enabled or Disabled (Hi-Z) (5), when Enabled driving 0 or 1	Opposite of output driver state: Disabled or Enabled (5)	Programmed by firmware for each pin: Enabled or Disabled, Pull-Up or Pull-Down (5)
Ultra_Low_Power: core supply on for always-on domain, core supply off for switchable domains	High	High	Retains previous state (4) for each pin: Enabled or Disabled (Hi-Z), when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled (5)	Retains previous state(6) for each pin: Enabled or Disabled, Pull-Up or Pull-Down

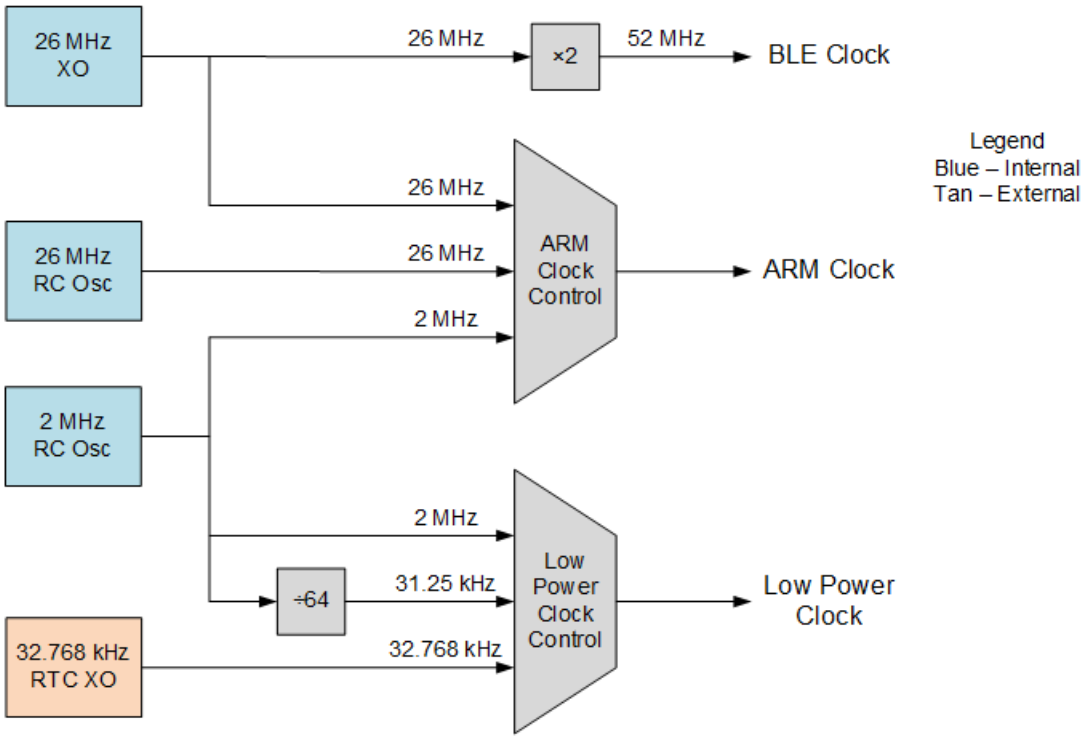
Note:

1. This table applies to all three types of I/O pins (digital switchable domain GPIOs, digital always-on/ wake-up GPIO, and mixed-signal GPIOs) unless otherwise noted.
2. Pull-up/down resistor value is 96 kOhm ±10%.
3. In Power-on Reset state pull-up resistor is enabled at always-on/wake-up GPIO only.
4. In Power-on Default state input drivers and pull-up/down resistors are disabled in the mixed-signal GPIOs only (mixed-signal GPIOs are defaulted to analog mode).
5. Mixed-signal GPIOs can be programmed to be in Analog or Digital mode for each pin. When programmed to Analog mode (default) the output driver, input driver, and pull-up/down resistors are disabled.
6. In Ultra_Low_Power state always-on/wake-up GPIO does not have retention capability and behaves same as in BLE_On states, also for mixed-signal GPIOs programming analog mode overrides retention functionality for each pin.

7. Clocking

The following figure provides an overview of the clock tree and clock management blocks.

Figure 7-1. Clock Architecture



The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I^2C). The recommended MCU clock speed is 26 MHz. The Low Power Clock is used to drive all the low-power applications like the BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26 MHz Crystal Oscillator (XO) is used for the BLE operations or in an event. A very accurate clock is required for the ARM subsystem operations.

The 26 MHz integrated RC oscillator is used for most of the general purpose operations on the MCU and its peripherals. In the cases, when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±40% over process, voltage, and temperature.

The frequency variation of 2 MHz RC oscillator is up to ±50% over process, voltage, and temperature.

The 32.768 kHz RTC Crystal Oscillator (RTC XO) is used for BLE operations as it reduces power consumption by providing the best timing for wake-up precision, allowing circuits to be in low-power Sleep mode for as long as possible until they need to wake up and connect during the BLE connection event.

7.1 26 MHz Crystal Oscillator

The following table provides the values for ATBTLC1000 26 MHz crystal oscillator parameters.

Table 7-1. ATBTLC1000 26 MHz Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Units
Crystal resonant frequency	N/A	26	N/A	MHz
Crystal equivalent series resistance		50	80	Ω
Stability - Initial offset (1)	-50		50	ppm
Stability - Temperature and aging	-40		40	ppm

Note:

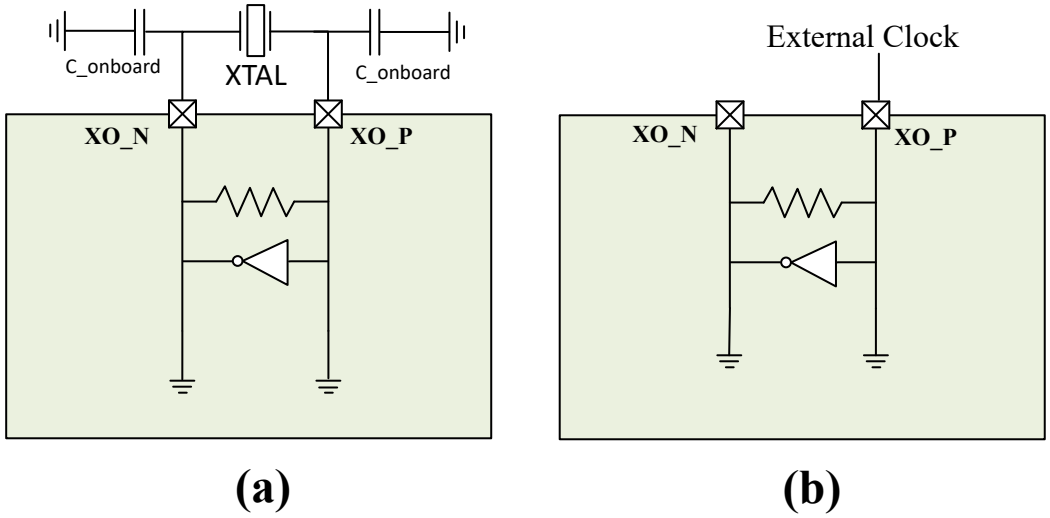
1. The initial offset must be calibrated to maintain ±25 ppm in all operating conditions. This calibration is performed during final production testing and calibration offset values are stored in eFuse. For more details, see the calibration application note.

The following block diagram (reference (a)) shows how the internal Crystal Oscillator (XO) is connected to the external crystal.

To bypass the crystal oscillator, 10 pF external signal can be applied to the XO_P terminal, as shown in reference (b). The required external bypass capacitors depend on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance. When bypassing XO_P from an external clock, XO_N must be floating.

It is recommended that only crystals specified for Clock (CL) at 8 pF can be used in customer designs, since this affects the sleep/wake-up timing of the device. CL other than 8 pF requires upgraded firmware and device re-characterization.

Figure 7-2. ATBTLC1000 Connections to XO



(a) Crystal Oscillator is Used

(b) Crystal Oscillator is Bypassed

WARNING **External Clock signal must be limited between 0 V and 1.2 V. If exceeded, damage is caused to the XO_P pin.**

The following table specifies the electrical and performance requirements for the external clock.

Table 7-2. ATBTLC1000 XO Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	26	26	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.75	1.2	V_{pp}	
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)		<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

7.2 32.768 kHz RTC Crystal Oscillator

The ATBTLC1000 has a 32.768 kHz RTC oscillator that is used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock must be within ±500 ppm. Because of the high accuracy of the 32.768 kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power Sleep mode for as long as possible, until they need to wake up for the next connection timed event.

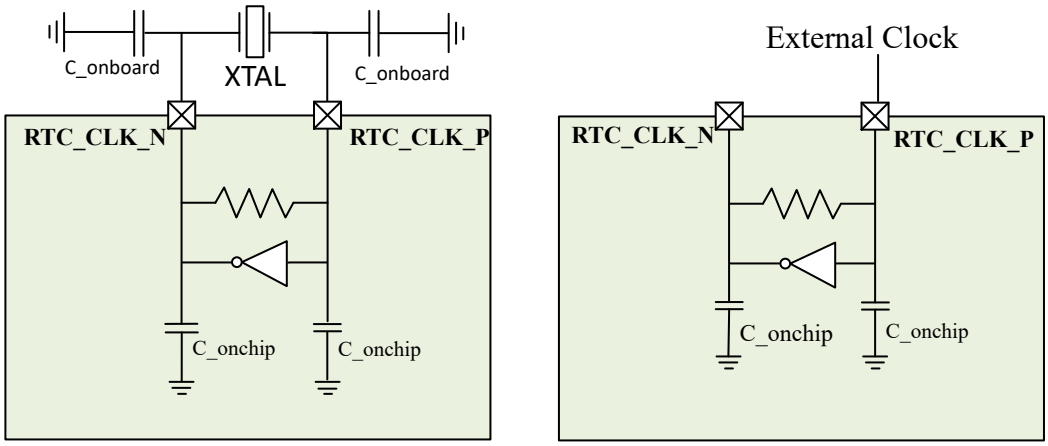
The following block diagram (reference (a)) shows how the internal low-frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15 pF on each terminal, RTC_CLK_P, and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~1 pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal, as shown in reference (b).

The need for external bypass capacitors depends on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and consider the on-chip capacitance. When bypassing RTC_CLK_P from an external clock, RTC_CLK_N is required to be floating.

Alternatively, if an external 32.768kHz clock is available, it can be used to drive the RTC_CLK_P pin instead of using a crystal. The XO has 6pF internal capacitance on the RTC_CLK_P pin. To bypass the crystal oscillator, an external signal capable of driving 6pF can be applied to the RTC_CLK_P terminal as shown in Figure (b). RTC_CLK_N must be left unconnected when driving an external source into RTC_CLK_P. Refer to the Table 7-1 for the specification of the external clock to be supplied at RTC_CLK_P.

Figure 7-3. ATBTLC1000 Connections to RTC XO



(a) **(b)**

(a) Crystal Oscillator is Used

(b) Crystal Oscillator is Bypassed

WARNING **External Clock signal must be limited between 0 V and 1.2 V. If exceeded, damage is caused to the XO_P pin.**

Note: Refer to the *BluSDK BLE API Software Development Guide* for details on how to enable the 32.768 kHz clock output and tune the internal trimming capacitors.

Table 7-3. 32.768 kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	Cl_onchip [pF]
0000	0.0
0001	1.0
0010	2.0
0011	3.0
0100	4.0
0101	5.0
0110	6.0
0111	7.0
1000	8.0
1001	9.0

.....continued	
Register: pierce_cap_ctrl[3:0]	**Cl_onchip [pF]**
1010	10.0
1011	11.0
1100	12.0
1101	13.0
1110	14.0
1111	15.0

7.2.1 RTC XO Design and Interface Specification

The RTC consists of two main blocks:

1. Programmable Gm stage
2. Tuning capacitors

The programmable Gm stage is used to guarantee oscillation startup and to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with a supply voltage of 1.2 V.

Table 7-4. RTC XO Interface

Pin Name	Function	Register Default
Digital control pins		
Pierce_res_ctrl	Control feedback resistance value: • 0 is 20 MOhm feedback resistance • 1 is 30 MOhm feedback resistance	0X4000F404<15>=’1’
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700 fF: • 0000 is 700 fF • 1111 is 11.2 pF Refer to the crystal datasheet to check for optimum tuning capacitance value.	0X4000F404<23:20>=”1000”
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: • 0011 for crystal with shunt cap of 1.2 pF • 1000 for crystal with shunt cap > 3 pF	0X4000F404<19:16>=”1000”
VDD_XO	1.2 V	

7.2.2 RTC Characterization with Gm Code Variation

The following graphs show the RTC total drawn current and the XO accuracy versus different tuning capacitors and different Gm codes, at a supply voltage of 1.2 V and temperature at 25°C.

Figure 7-4. RTC Drawn Current vs. Tuning Caps at 25°C

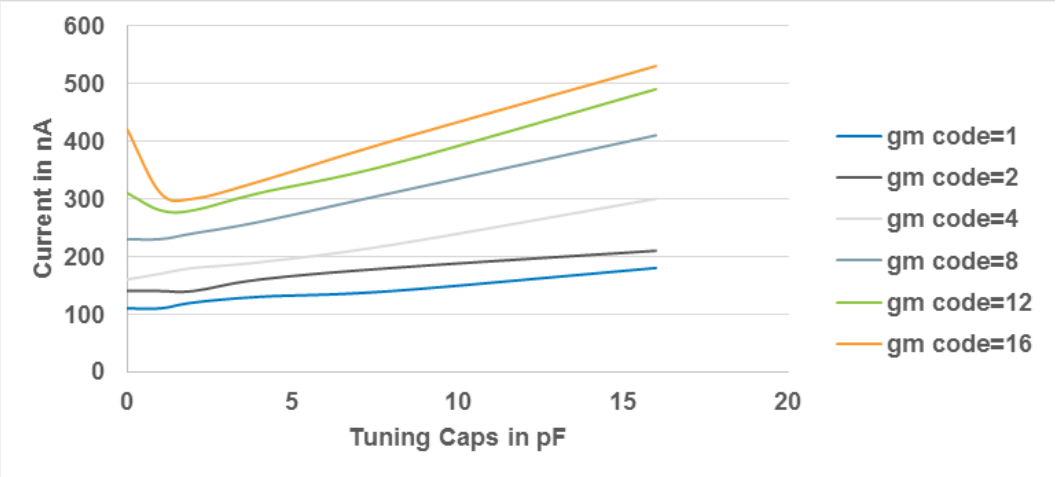
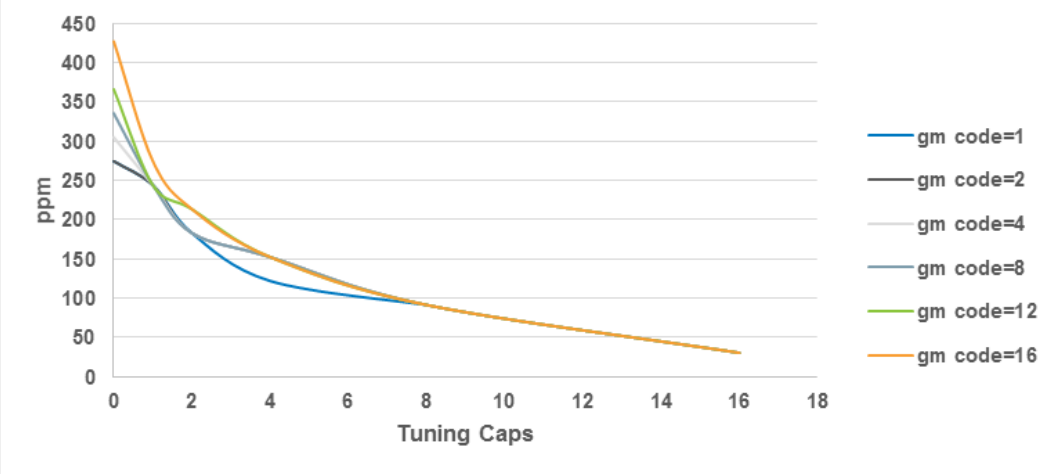


Figure 7-5. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



7.2.3 RTC Characterization with Supply Variation and Temperature

The following graphs show the RTC total drawn current versus different supply voltage and different GM codes, at a temperature of 25°C.

Figure 7-6. RTC Drawn Current vs. Supply Variation

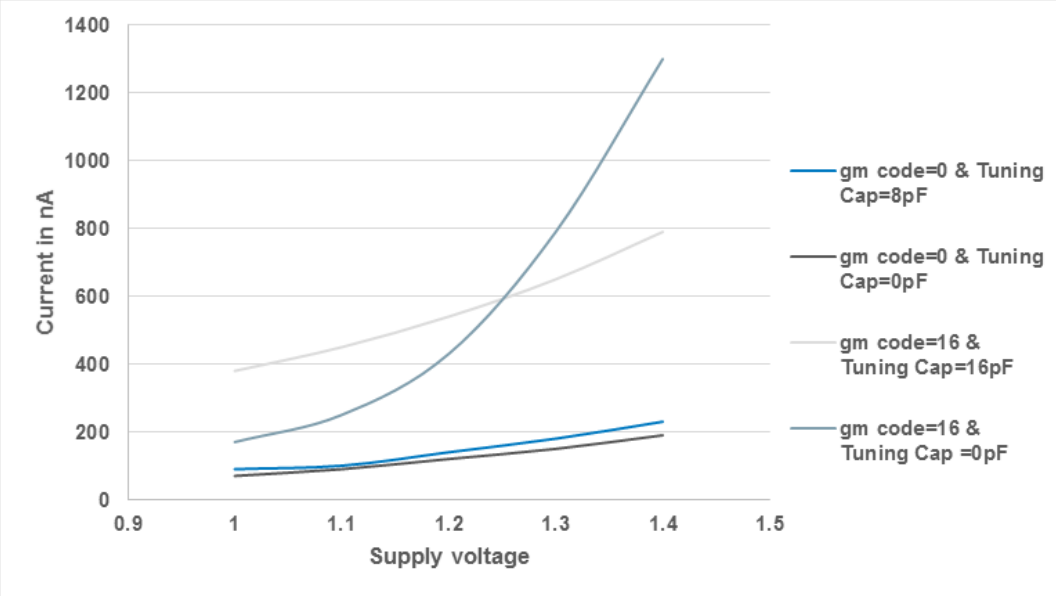
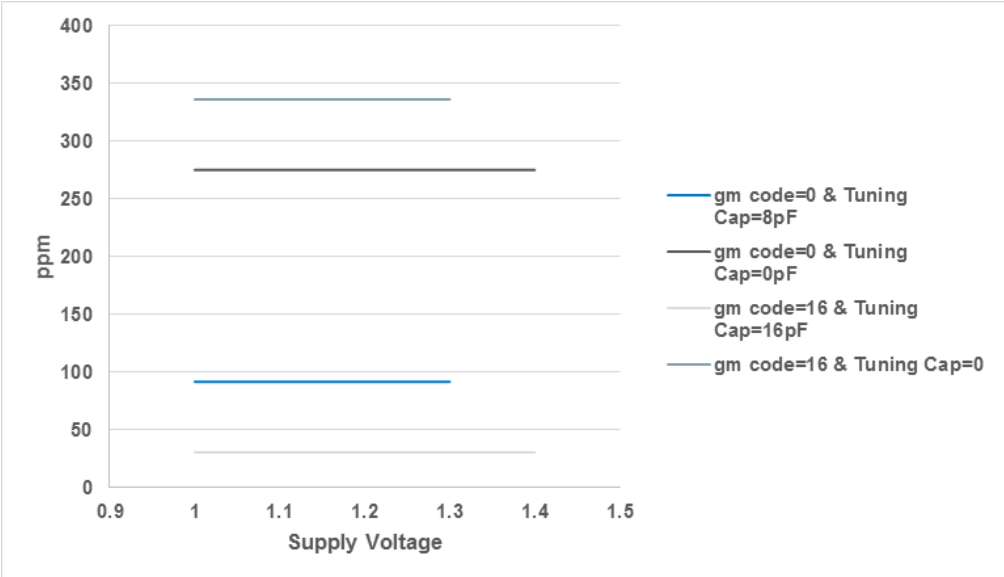


Figure 7-7. RTC Frequency Deviation vs. Supply Voltage



7.3 2 MHz and 26 MHz Integrated RC Oscillators

The 2 MHz integrated RC oscillator circuit without calibration has a frequency variation of 50% over process, temperature, and voltage variation. The calibration over process, temperature, and voltage is required to maintain the accuracy of this clock.

Figure 7-8. 32 kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

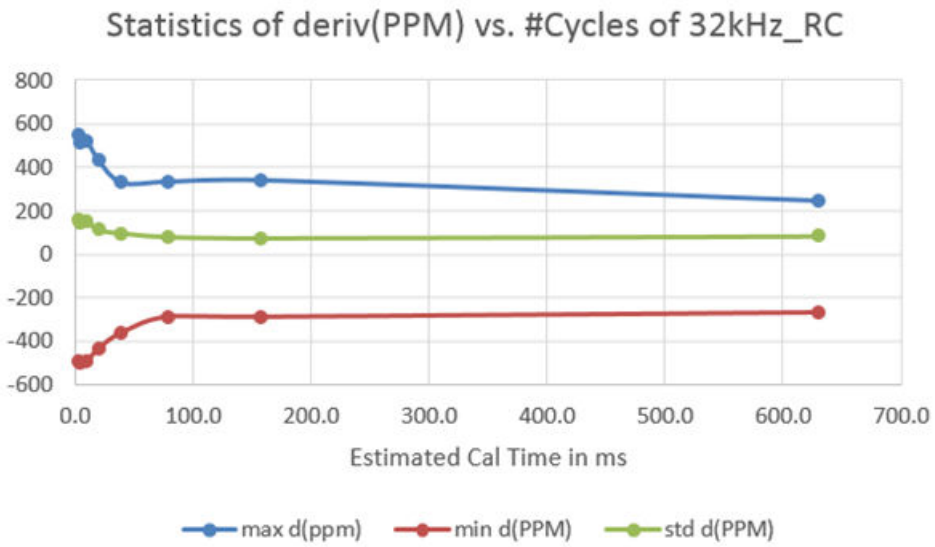
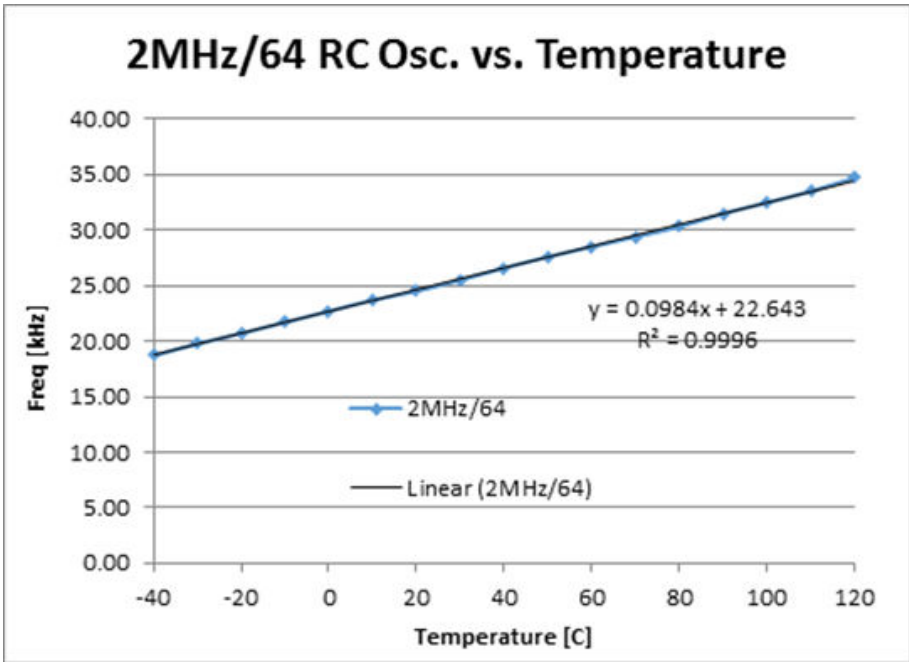


Figure 7-9. 32 kHz RC Oscillator Frequency Variation over Temperature



The 26 MHz integrated RC oscillator circuit has a frequency variation of 50% over process, temperature, and voltage variation.

8. CPU and Memory Subsystem

This chapter describes the ARM Cortex-M0 32-bit processor and memory subsystem of the ATBTLC1000.

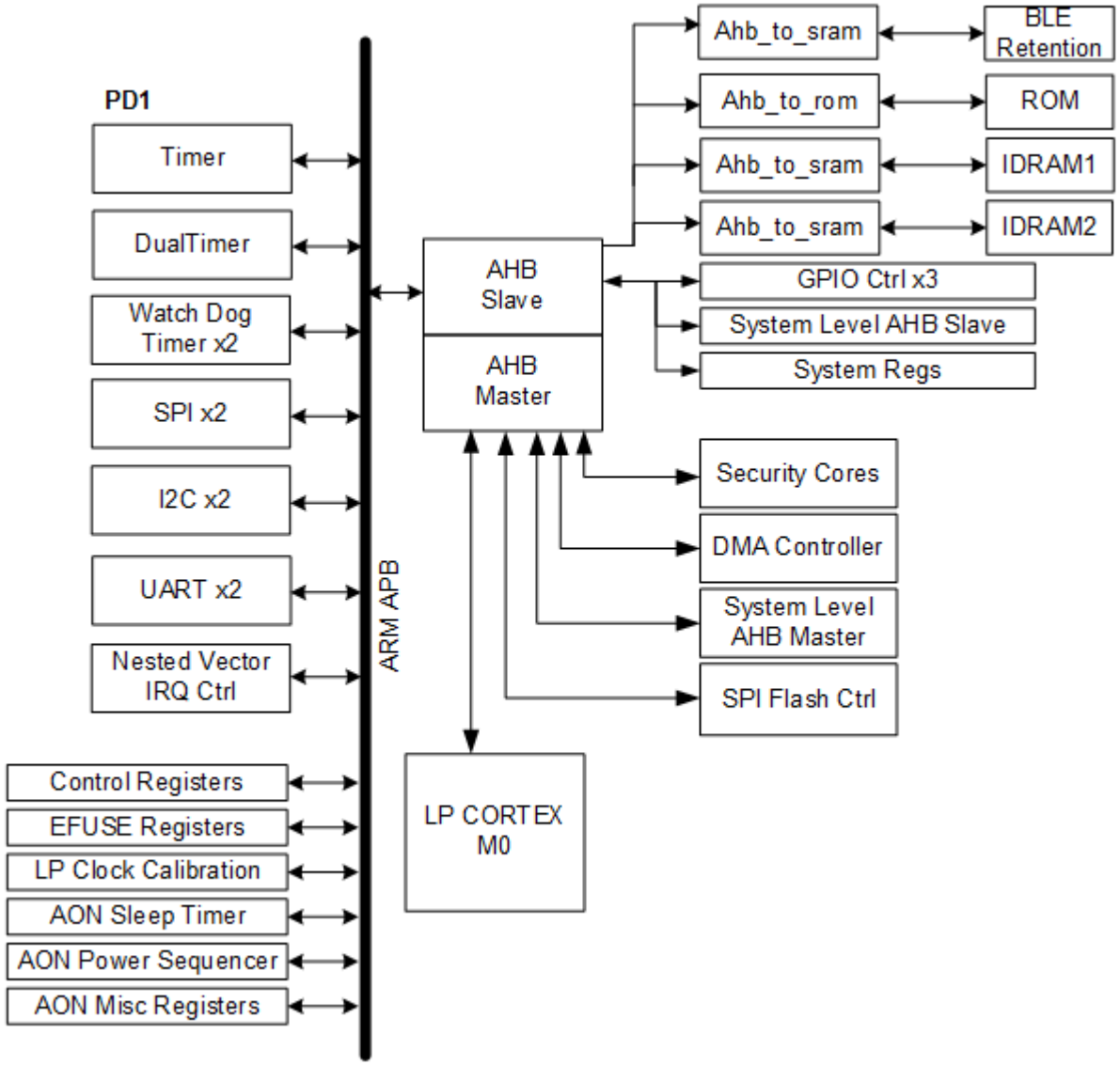
8.1 ARM Subsystem

The ATBTLC1000 has an ARM Cortex-M0 32-bit processor. The processor controls the BLE subsystem and handles all application features. The Cortex-M0 Microcontroller consists of a full 32-bit processor which can address 4 GB of memory. It has a RISC-like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology, which provides high speed and low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution, with four hardware breakpoint and two watchpoint options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port for microcontrollers and other small package devices.

Figure 8-1. ATBTLC1000 ARM Cortex-M0 Subsystem



8.1.1 Features

The following are the processor features and benefits:

- Integrated with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated Sleep modes using a wake-up interrupt controller for low-power consumption
- Deterministic and high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

8.1.2 Module Descriptions

The various modules of ATBTLC1000 are detailed in the following sections.

8.1.2.1 Timer

The 32-bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation and time tracking.
Note: Usage of this peripheral is not supported by the SDK. This datasheet will be updated once support for this feature is added in SDK.

8.1.2.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in the free-running, periodic, or one-shot mode.
Note: Usage of this peripheral is not supported by the SDK. This datasheet will be updated once support for this feature is added in SDK.

8.1.2.3 Watchdog Timer

The two watchdog blocks allow the CPU to be interrupted, if it has not interacted with the watchdog timer before it expires. In addition, this interrupt is an output of the core so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This allows the CPU to return to a known state in the event a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure to recover from software crashes.

The Watchdog Timer is being used by the BLE stack. It cannot be used by user application.

8.1.2.4 Wake-Up Timer

The wake-up timer is a 32-bit countdown timer that operates on a 32 kHz sleep clock. It can be used as a general purpose timer for the ARM or as a wake-up source for the chip. It has the ability to be a one-time programmable timer, as it generates an interrupt/wake-up on expiration and stop the operation. It also has the ability to be programmed in an auto reload fashion where it generates an interrupt/wake up and then proceeds to start another countdown sequence.
Note: Usage of this peripheral is not supported by the SDK. The datasheet will be updated once support for this feature is added in SDK.

8.1.2.5 SPI Controller

For detailed information on SPI controller, refer to 10.2 SPI Master/Slave Interface.
Note: Usage of this peripheral is not supported by the SDK. The datasheet will be updated once support for this feature is added in SDK.

8.1.2.6 I^2C Controller

For detailed information on I^2C controller, refer to 10.1 I2C Master/Slave Interface.
Note: Usage of this peripheral is not supported by the SDK. The datasheet will be updated once support for this feature is added in SDK.

8.1.2.7 UART

For detailed information on UART, refer to 10.3 UART Interface.
Note: Accessing and controlling the registers of this peripheral is not supported by the SDK. The datasheet will be updated once support for this feature is added in SDK.

8.1.2.8 DMA Controller

The Direct Memory Access (DMA) controller allows certain hardware subsystems to access main system memory of the Cortex-M0 Processor, independently.

The following are the DMA features and benefits:

- Supports any address alignment
- Supports any buffer size alignment

- Peripheral flow control, including peripheral block transfer
- Supports the following modes:
  - Peripheral-to-peripheral transfer
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Register-to-memory
- Interrupts for both TX and RX done in memory and peripheral mode
- Scheduled transfers
- Endianness byte swapping
- Watchdog Timer
- Four-channel operation
- 32-bit data width
- AHB MUX (on read and write buses)
- Supports command lists
- Usage of tokens

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.9 Nested Vector Interrupt Controller

External interrupt signals connect to the Nested Vector Interrupt Controller (NVIC), and the NVIC prioritizes the interrupts. The software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little-endian. Any attempt to read or write a half-word or byte individually is unpredictable.

The NVIC allows the CPU to individually enable, disable each interrupt source, and hold each interrupt until it is serviced and cleared by the CPU.

Table 8-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

For the description of each register, see the Cortex-M0 documentation from ARM.

8.1.2.10 GPIO Controller

The AHB GPIO is a general-purpose I/O interface unit allowing the CPU to independently control all input or output signals on ATBTLC1000. These can be used for a wide variety of functions pertaining to the application.

The AHB GPIO provides a 16-bit I/O interface with the following features:

- Programmable interrupt generation capability
- Programmable masking support
- Thread-safe operation by providing separate set and clear addresses for control registers
- Inputs are sampled using a double flip-flop to avoid meta-stability issues

Note: Usage of this peripheral is not supported by the SDK. The datasheet will be updated once support for this feature is added in SDK.

8.2 Memory Subsystem

The Cortex-M0 core uses a 128 KB instruction/boot ROM along with a 128 KB shared instruction and data RAM.

8.2.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data that is used by the ARM processor. The size of IDRAM1 and IDRAM2 that can be used for BLE subsystem for the user application is 128 KB. The IDRAM1 contains three 32 KB and IDRAM2 contains two 16 KB memories that are accessible to the ARM processor and used for instruction/data storage.

8.2.2 ROM

The ROM is used to store the boot code and BLE firmware, stack, and selected user profiles. The ROM contains the 128 KB memory that is accessible to the ARM.

8.2.3 BLE Retention Memory

The BLE functionality requires 8 KB or more, depending on the application state, instruction, and data to be retained in memory when the processor either goes into the Sleep mode or Power Off mode. The RAM is separated into specific power domains to allow trade-off in power consumption with retention memory size.

8.3 Non-Volatile Memory

The eFuse memory for ATBTLC1000 is described to indicate the parameters that are programmed from factory, which are available for customer use. The ATBTLC1000 have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This memory region is one-time-programmable. It is partitioned into six 128-bit banks. Each bank is divided into four blocks with each block containing 32 bits of memory locations. This non-volatile, one-time-programmable memory is used to store customer specific parameters as listed below.

- 26 MHz XO Calibration information
- BT address

The bit map for the block containing the above parameters is detailed in the following figures. For the procedure to write eFuse memory location, refer to section “Hardware Flow Control for 4-Wire Mode eFuse” in the *ATBTLC1000 BluSDK Example Profiles Application User’s Guide* (http://www.microchip.com/DS50002640)

Figure 8-2. Bank 5 Block 0

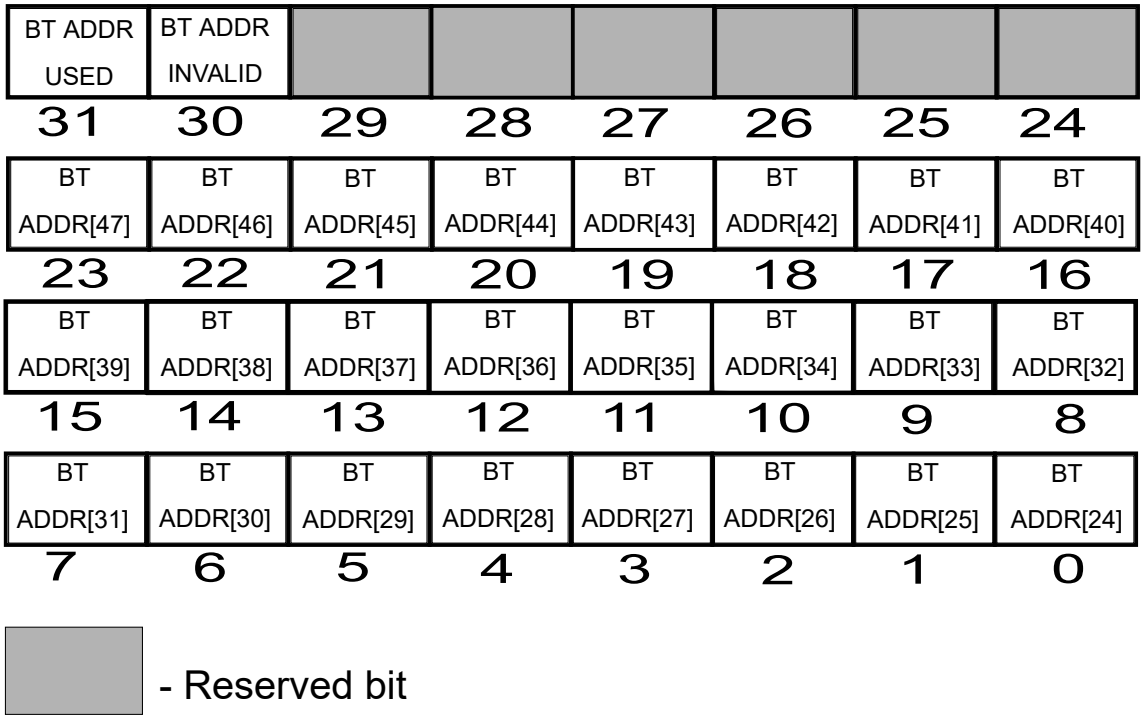


Figure 8-3. Bank 5 Block 1

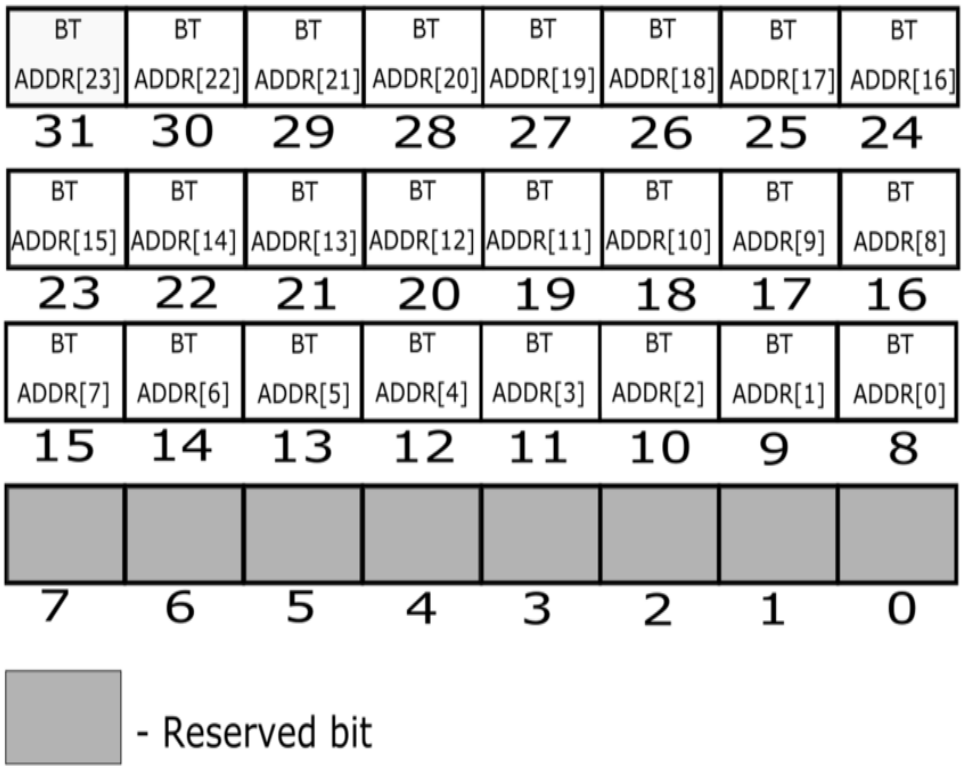
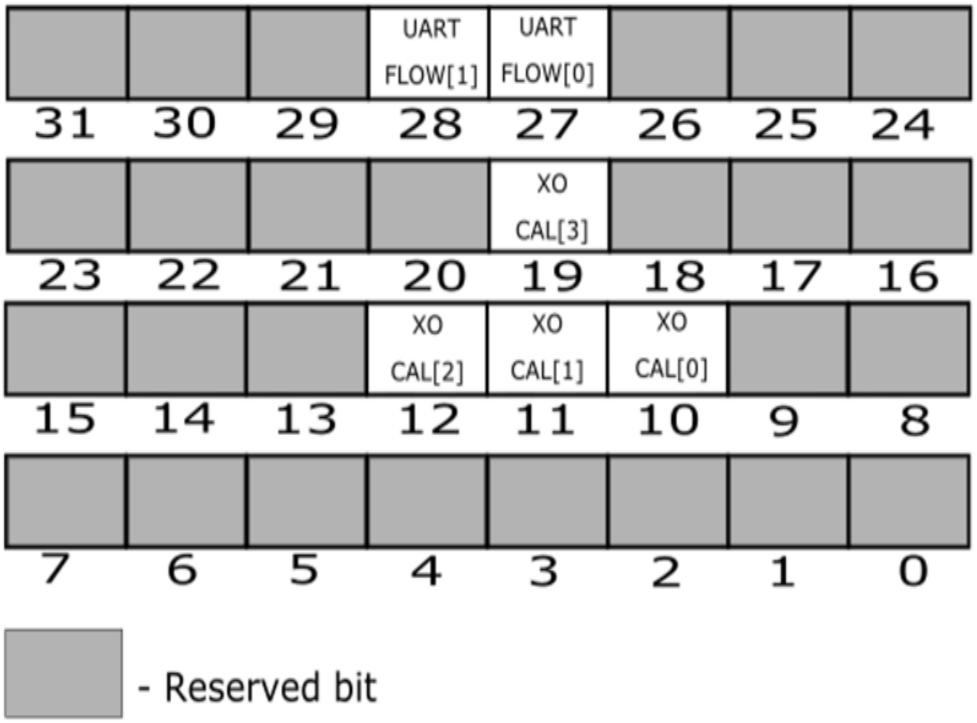


Figure 8-4. Bank 5 Block 3



The bits that are not depicted in the above register description are all reserved for future use.

8.3.1 26 MHz XO Calibration information

Information for ATBTLC1000 must be programmed by the user in production.

8.3.2 UART Hardware Flow Control Pin Selection

These bits determine the LP_GPIO pins to be used as the hardware flow control pins (RTS and CTS) of the UART interface with host MCU. For the ATBTLC1000, these bits have a default value of 0b00, which corresponds to the device being configured in 6-Wire mode. The following are the possible values for these bits and the corresponding configuration.

Table 8-2. UART Flow control Bank 5 Block 3

UART Flow control Bank 5 Block 3[28:27]	UART RTS	UART CTS
0b01	LP_GPIO_18	LP_GPIO_16
0b10	LP_GPIO_9	LP_GPIO_8
0b11	LP_GPIO_5	LP_GPIO_4

8.3.3 BT Address

These bits contain the BT address used by the user application. For ATBTLC1000, user must purchase the MAC address from IEEE® and store it in the non-volatile memory section of the host MCU. During initialization of ATBTLC1000, the BLE address can be set by the host MCU. For more details, refer to the API User Manual available in the BluSDK release package.

Programming Bit 31 of Bank 5 Block 0 (BT_ADDR_USED) with a value of 1 indicates that the BT address in the eFuse memory location is intended to be used.

Programming Bit 30 of Bank 5 Block 0 (BT_ADDR_INVALID) with a value of 1 indicates that the BT address in the eFuse memory location is invalid.

9. Bluetooth Low Energy Subsystem

The Bluetooth Low Energy (BLE) subsystem implements all the critical real-time functions required for full compliance with specifications of the Bluetooth System, v5.0, Bluetooth SIG. It consists of a Bluetooth baseband controller (core), radio transceiver and the Microchip Bluetooth Smart Stack, the BLE software platform.

9.1 BLE Core

The baseband controller consists of a modem and a Medium Access Controller (MAC). It schedules frames, and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control.

The core performs Link Control Layer management supporting the main BLE states, including advertising and connection.

9.1.1 Features

- Broadcaster, Central, Observer, Peripheral
- Simultaneous master and slave operation with up to eight connections
- Frequency hopping
- Advertising/data/control packet types
- Encryption (AES-128, SHA-256)
- Bitstream processing (CRC, whitening)
- Operating clock 52 MHz

9.2 BLE Radio

The radio consists of a fully-integrated transceiver, including Low Noise Amplifier (LNA), Receive (RX) down converter, analog baseband processing, Phase Locked Loop (PLL), Transmit (TX) Power Amplifier, and Transmit/Receive switch. At the RF front end, no external RF components on the PCB are required other than the antenna and a matching component.

Table 9-1. ATBTLC1000 BLE Radio Features and Properties

Feature	Description
Part Number	ATBTLC1000
BLE standard	Bluetooth V5.0 – Bluetooth Low Energy
Frequency range	2402 MHz to 2480 MHz
Number of channels	40
Modulation	GFSK
PHY Data rate	1 Mbps

9.2.1 Microchip BluSDK

BluSDK offers a comprehensive set of tools, including reference applications for several Bluetooth SIG defined profiles and custom profile. This helps the user to quickly evaluate, design and develop BLE products with ATBTLC1000.

The ATBTLC1000 have a complete integrated Bluetooth Low Energy stack on-chip, fully qualified, mature, and Bluetooth V5.0 compliant.

Customer applications interface with the BLE protocol stack through the adaptor library API, which supports direct access to the GAP, SMP, ATT, GATT client / server, and L2CAP service layer protocols in the embedded firmware.

The stack includes numerous BLE profiles for applications like:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Key fob

Together with the Atmel Studio Software Development environment, additional customer profiles can be easily developed.

Refer to BluSDK release notes for more details on the supported host MCU architecture and compilers.

9.2.2 Direct Test Mode Example Application

One among the reference application offered in BluSDK is a Direct Test Mode (DTM) example application. Using this application, the user can configure the device in the different test modes as defined in the Bluetooth Low Energy Core 5.0 specification (Vol6, Part F Direct Test Mode). Refer the examples in the getting started guide available in the BluSDK release package.

10. External Interfaces

The ATBTLC1000 external interfaces include:

- Two SPI Master/Slave (SPI0 and SPI1)
- Two I^2C Master/Slave (I^2C0 and I^2C1)
- Two UART (UART1 and UART2)
- One SPI Flash
- One SWD
- General Purpose Input/Output (GPIO) pins

⚠ CAUTION Usage of the above mentioned peripherals is not supported by the SDK. The datasheet will be updated once support is added in SDK. The UART is the host interface with flow control; refer to Host Microcontroller Interface for the configurations.

The following table provides the different peripheral functions that are software-selectable for each pin. This allows for maximum flexibility of mapping desired interfaces on GPIO pins. The MUX1 option allows for any MEGAMUX option from ATBTLC1000 Software Selectable MEGAMUX Options to be assigned to a GPIO.

Table 10-1. ATBTLC1000 Pin-MUX Matrix of External Interfaces

Pin Name	Pin No.	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_0	4	Up/Down	GPIO 0	MEGAMUX 0	SWD CLK					TEST OUT 0
LP_GPIO_1	5	Up/Down	GPIO 1	MEGAMUX 1	SWD I/O					TEST OUT 1
LP_GPIO_2	6	Up/Down	GPIO 2	MEGAMUX 2	UART1 RXD		SPI1 SCK	SPI0 SCK		TEST OUT 2
LP_GPIO_3	7	Up/Down	GPIO 3	MEGAMUX 3	UART1 TXD		SPI1 MOSI	SPI0 MOSI		TEST OUT 3
LP_GPIO_8	8	Up/Down	GPIO 8	MEGAMUX 8	I^2C0 SDA			SPI0 SSN		TEST OUT 8
LP_GPIO_9	9	Up/Down	GPIO 9	MEGAMUX 9	I^2C0 SCL			SPI0 MISO		TEST OUT 9

.....continued

Pin Name	Pin No.	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_10	10	Up/Down	GPIO 10	MEGAMUX 10	SPI0 SCK					TEST OUT 10
LP_GPIO_11	11	Up/Down	GPIO 11	MEGAMUX 11	SPI0 MOSI					TEST OUT 11
LP_GPIO_12	12	Up/Down	GPIO 12	MEGAMUX 12	SPI0 SSN					TEST OUT 12
LP_GPIO_13	13	Up/Down	GPIO 13	MEGAMUX 13	SPI0 MISO					TEST OUT 13
LP_GPIO_16	25	Up/Down	GPIO 16	MEGAMUX 16			SPI1 SSN	SPI0 SCK		TEST OUT 16
LP_GPIO_18	27	Up/Down	GPIO 18	MEGAMUX 18			SPI1 MISO	SPI0 SSN		TEST OUT 18
AO_GPIO_0	24	Up	GPIO 31	WAKEUP	RTC CLK IN	32 KHZ CLK OUT				
GPIO_MS1[1]	17	Up/Down	GPIO 47							
GPIO_MS2[1]	18	Up/Down	GPIO 46							

Note:

1. If analog functionality for this pin is enabled, the digital functionality is disabled.

The following table shows the various ATBTLC1000 software-selectable MEGAMUX options that correspond to specific peripheral functionality.

Table 10-2. ATBTLC1000 Software Selectable MEGAMUX Options

MUX_Sel	Function	Notes
0	UART1 RXD	
1	UART1 TXD	

.....continued

MUX_Sel	Function	Notes
2	UART1 CTS	
3	UART1 RTS	
4	UART2 RXD	
5	UART2 TXD	
6	UART2 CTS	
7	UART2 RTS	
8	I^2C0 SDA	
9	I^2C0 SCL	
10	I^2C1 SDA	
11	I^2C1 SCL	
12	PWM 1	
13	PWM 2	
14	PWM 3	
15	PWM 4	
16	LP CLOCK OUT	32 kHz clock output (RC Oscillator or RTC XO)
17	Reserved	
18	Reserved	
19	Reserved	
20	Reserved	
21	Reserved	
22	Reserved	
23	Reserved	
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	

.....continued		
MUX_Sel	**Function**	**Notes**
29	QUAD DEC X IN A	
30	QUAD DEC X IN B	
31	QUAD DEC Y IN A	
32	QUAD DEC Y IN B	
33	QUAD DEC Z IN A	
34	QUAD DEC Z IN B	

The following example shows the peripheral assignment using these MEGAMUX options.

- I^2C0 pin-MUXed on LP_GPIO_8, LP_GPIO_9 connected via MUX1, and MEGAMUX is set at 8 and 9.
- I^2C1 pin-MUXed on LP_GPIO_0, LP_GPIO_1 connected via MUX1, and MEGAMUX is set at 10 and 11.
- PWM pin-MUXed on LP_GPIO_16 via MUX1, and MEGAMUX is set at 12.

The following example shows the available options for LP_GPIO_3 pin, depending on the selected pin-MUX option.

- MUX0 – This pin functions as bit 3 of the GPIO bus and is controlled by the GPIO controller in the ARM subsystem.
- MUX1 – Any option from the MEGAMUX table can be selected, for example, it can be a quad_dec, pwm, or any of the other functions listed in the MEGAMUX table.
- MUX2 – This pin functions as UART1 TXD. This can also be achieved with the MUX1 option via MEGAMUX, but the MUX2 option allows a shortcut for the recommended pinout.
- MUX3 – This option is not used and thus defaults to the GPIO option (same as MUX0).
- MUX4 – This pin functions as SPI1 MOSI (this option is not available through MEGAMUX).
- MUX5 – This pin functions as SPI0 MOSI (this option is not available through MEGAMUX).
- MUX7 – This pin functions as bit 3 of the test output bus, providing access to various debug signals.

10.1 I^2C Master/Slave Interface

The ATBTLC1000 provides and I^2C interface that can be configured as slave or master. The I^2C interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The ATBTLC1000 I^2C supports I^2C bus Version 2.1 - 2000 and can operate in the following speed modes.

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- High-Speed mode (3.4 Mbps)

The I^2C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I^2C -Bus Specification, Ver2.1”.

10.2 SPI Master/Slave Interface

The ATBTLC1000 provides a Serial Peripheral Interface (SPI) that can be configured as master or slave. The SPI interface pins are mapped as shown in the following table. The SPI interface is a full-duplex slave-synchronous serial interface. When the SPI is not selected, that is, when SSN is high, the SPI interface does not interfere with data transfers between the serial-master and other serial-slave devices. When the serial-slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line. The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

Table 10-3. ATBTLC1000 SPI Interface Pin Mapping

Pin Name	SPI Function
SSN	Active Low Slave Select
SCK	Serial Clock
MOSI	Master Out Slave In (Data)
MISO	Master In Slave Out (Data)

10.2.1 SPI Interface Modes

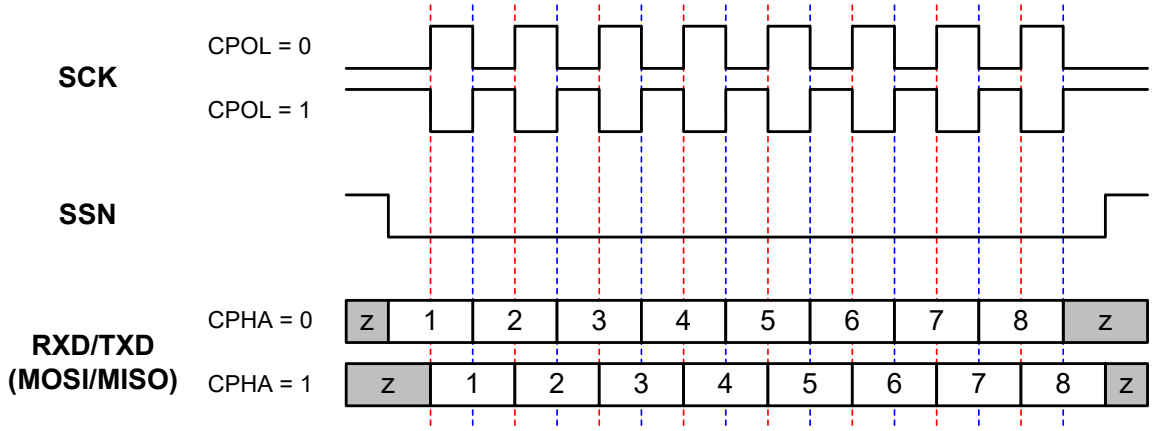
The SPI interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Table 10-4. ATBTLC1000 SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The red lines in the following figure correspond to Clock Phase at 0 and the blue lines correspond to Clock Phase at 1.

Figure 10-1. ATBTLC1000 SPI Clock Polarity and Clock Phase Timing



10.3 UART Interface

The ATBTLC1000 provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem has two UART interfaces:

- A 2-pin interface for data transfer only (TX and RX)
- A 4-pin interface for hardware flow control handshaking (RTS and CTS), and data transfer (TX and RX).

The UART interfaces are compatible with the RS-232 standard, where ATBTLC1000 operates as Data Terminal Equipment (DTE).

Important: The RTS and CTS are used for hardware flow control, they must be connected to the host MCU UART and enabled for the UART interface to be functional.

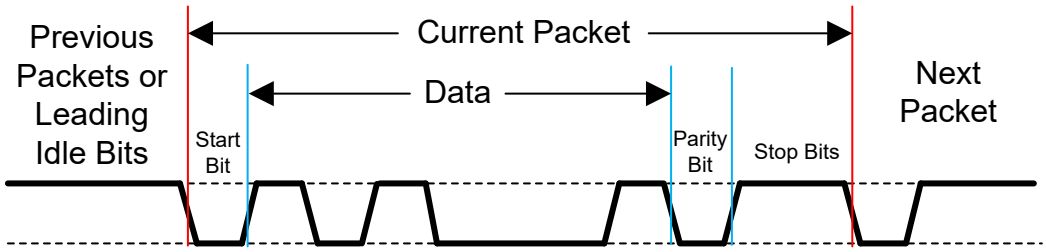
The pins associated with each UART interfaces can be enabled on several alternative pins by programming their corresponding pin-MUX control registers (see Pin-MUX Matrix of External Interfaces table and the Software Selectable MEGAMUX Options table for available options).

The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 26 MHz, 13 MHz, 6.5 MHz, and 3.25 MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 26 MHz/8.0 = 3.25 MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well as the ability to generate interrupts based on these status bits.

The following figure shows an example of UART receiving or transmitting a single packet. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 10-2. Example of UART RX or TX Packet



10.4 GPIOs

The ATBTLC1000 has 15 General Purpose Input/Output (GPIO) pins, labeled as LP_GPIO, GPIO_MS, and AO_GPIO, are available for application-specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output. The host or internal processor can program the output values.

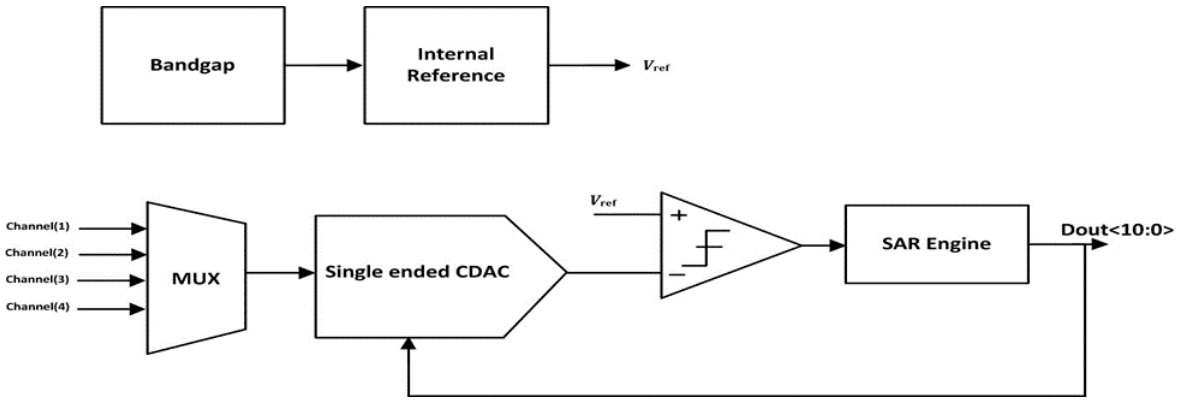
The LP_GPIO are digital interface pins, GPIO_MS are mixed signal/analog interface pins, and AO_GPIO is an always-on digital interface pin that can detect interrupt signals while in deep sleep mode for wake-up purposes.

The LP_GPIO pins have interrupt capability, but only when in the active/standby mode. In Sleep mode, they are turned off to save power consumption.

10.5 Analog-to-Digital (ADC) Converter

The ATBTLC1000 has an integrated Successive Approximation Register (SAR) Analog-to-Digital Converter with 11-bit resolution and variable conversion speed up to 1 MS/s. The key building blocks are the capacitive Digital-to-Analog Converter (DAC), comparator and synchronous SAR engine, as shown in the following figure.

Figure 10-3. ATBTLC1000 SAR ADC Block Diagram



The ADC reference voltage can be either generated internally or set externally via one of the two available mixed-signal GPIO pins on the ATBTLC1000.

There are two modes of operation:

1. High resolution (11-bit) – Set the reference voltage to half the supply voltage or below. In this condition the input signal dynamic range is equal to twice the reference voltage (ENOB is 10 bit).
2. Medium resolution (10-bit) – Set the reference voltage to any value below supply voltage (up to 300 mV supply voltage) and in this condition, the input dynamic range is from zero to the reference voltage (ENOB is 9 bit).

Four input channels are time multiplexed to the input of the SAR ADC. However, on the ATBTLC1000, only two channel inputs are accessible from the outside, through pins 17 and 18 (Mixed-Signal GPIO pins).

In Power-Saving mode, the internal reference voltage is completely OFF and the reference voltage is set externally.

The ADC characteristics are summarized in the following table.

Table 10-5. SAR ADC Characteristics

Conversion Rate	1ks → 1MS
Selectable resolution	10 → 11bit
Power consumption	13.5 µA (at 100 KS/s) (1)

Note: 1. With an external reference.

10.5.1 Timing

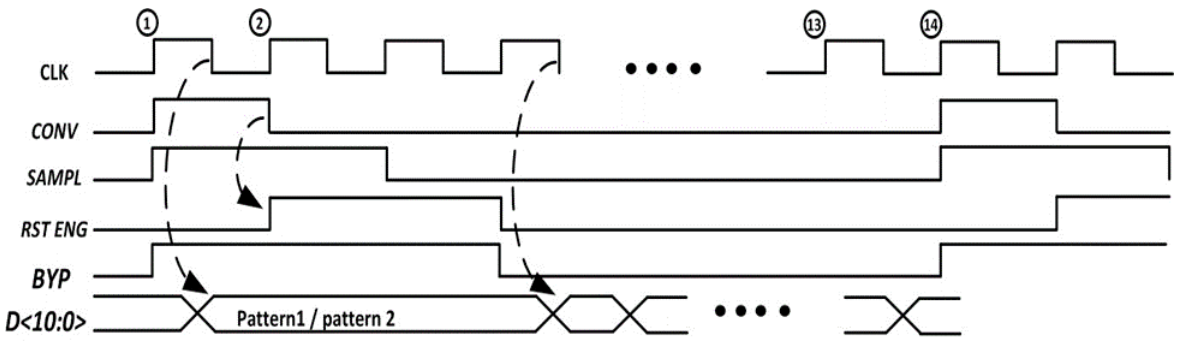
The ADC timing is shown in the following figure. The input signal is sampled twice. In the first sampling cycle the input range is defined either to be above or below reference voltage, and in the second sampling instant the ADC starts its normal operation.

The ADC takes two sampling instants and N-1 conversion cycle (N is ADC resolution) and one cycle to sample the data out. Therefore, for the 11-bit resolution, it takes 13 clock cycles to do one sample conversion.

The input clock equals N+2 the sampling clock frequency (N is the ADC resolution).

1. CONV signal – Indicates end of conversion.
2. SAMPL – The input signal is sampled when this signal is high.
3. RST ENG – When High SAR Engine is in the Reset mode (SAR engine output is set to mid-scale).

Figure 10-4. SAR ADC Timing



10.6 Software Programmable Timer and Pulse Width Modulator

The ATBTLC1000 contains four individually configurable Pulse Width Modulator (PWM) blocks to provide external control voltages. The base frequency of the PWM block (f_{PWM_base}) is derived from the XO clock (26 MHz) or the RC oscillator followed by a programmable divider.

The frequency of each PWM pulse (f_{PWM}) is programmable in steps according to the following relationship:

$$f_{PWM} = \frac{f_{PWM\_base}}{64*2^{i}} \qquad i = 0,1,2,...,8$$

The duty cycle of each PWM signal is configurable with 10-bit resolution (minimum duty cycle is 1/1024 and the maximum is 1023/1024).

The $f_{PWM_{base}}$ can be selected to have different values according the following table. The minimum and maximum frequencies supported for each clock selection are also listed in the following table.

Table 10-6. f_{PWM} Range for Different f_{PWM} Base Frequencies.

$f_{PWM_{base}}$	f_{PWM} max.	f_{PWM} min.
26 MHz	406.25 kHz	1.586 kHz
13 MHz	203.125 kHz	793.25 Hz
6.5 MHz	101.562 kHz	396.72 Hz
3.25 MHz	50.781 kHz	198.36 Hz

10.7 Clock Output

The ATBTLC1000 has an ability to output a clock. The clock can be output to any GPIO pin via the test MUX.

Note: This feature requires the ARM and BLE power domains to stay ON.

If BLE is not used, the clocks to the BLE core are gated OFF, resulting in small leakage. The following two methods can be used to output a clock. For more information on how to enable the 32.768kHz clock output refer the BluSDK BLE API Software Development Guide.

10.7.1 Variable Frequency Clock Output Using Fractional Divider

The ATBTLC1000 can output the variable frequency ADC clock using a fractional divider of the 26 MHz oscillator. This clock must be enabled using bit 10 of the `lpmcu_clock_enables_1` register. The clock frequency can be controlled by the divider ratio using the sens_adc_clk_ctrl register (12-bits integer part, 8-bit fractional part).The division ratio can vary from 2 to 4096 delivering output frequency between 6.35 kHz to 13 MHz. This is a digital divider with pulse swallowing implementation so the clock edges may not be at exact intervals for the fractional ratios. However, it is exact for integer division ratios.

10.7.2 Fixed Frequency Clock Output

The ATBTLC1000 can output the following fixed-frequency clocks:

- 52 MHz derived from XO
- 26 MHz derived from XO

- 2 MHz derived from the 2 MHz RC oscillator
- 31.25 kHz derived from the 2 MHz RC oscillator
- 32.768 kHz derived from the RTC XO
- 26 MHz derived from 26 MHz RC oscillator
- 6.5 MHz derived from XO
- 3.25 MHz derived from 26 MHz RC oscillator

For clocks 26 MHz and above, ensure that the external pad load on the board is minimized to get a clean waveform.

10.8 Three-Axis Quadrature Decoder

The ATBTLC1000 has a three-axis quadrature decoder (X, Y, and Z) that can determine the direction and speed of movement on three axes, required in total six GPIO pins to interface with the sensors. The sensors are expected to provide pulse trains as inputs to the quadrature decoder.

Each axis channel input has two pulses with ±90 degrees phase-shift depending on the direction of movement. The decoder counts the edges of the two waveforms to determine the speed, and uses the phase relationship between the two inputs to determine the direction of motion.

The decoder is configured to interrupt ARM based on independent thresholds for each direction. Each quadrature clock counter (X, Y, and Z) is an unsigned 16-bit counter and the system clock uses a programmable sampling clock ranging from 26 MHz, 13 MHz, 6.5 MHz, to 3.25 MHz.

If a wake up is desired from threshold detection on an axis input, the always-on GPIO needs to be used (there is only one always-on GPIO on the ATBTLC1000).

11. Electrical Characteristics

There are voltage ranges where different VDDIO levels are applied. The reason for this separation for the I/O drivers whose drive strength is directly proportional to the I/O supply voltage. In the ATBTLC1000 products, there is a large gap in the I/O supply voltage range (1.8 to 4.3 V). A guarantee on drive strength across this voltage range is intolerable to most vendors who only use a subsection of the I/O supply range. Therefore, these voltages are segmented into three manageable sections, such as $VDDIO_L$, $VDDIO_M$, and $VDDIO_H$.

11.1 Absolute Maximum Ratings

The values listed in this section are the ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Table 11-1. ATBTLC1000 Absolute Maximum Ratings

Symbol	Characteristics	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	5.0	V
VBATT	Battery Supply Voltage	-0.3	5.0	
V_{IN} (1)	Digital Input Voltage	-0.3	VDDIO	
V_{AIN} (2)	Analog Input Voltage	-0.3	1.5	
T_A	Storage Temperature	-65	150	°C

Note:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to all the analog pins, RFIO, VDD_RF, VDD_AMS, VDD_SXDIG, VDD_VCO, XO_N, XO_P, TPP, RTC_CLK_N, and RTC_CLK_P.

11.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for ATBTLC1000.

Table 11-2. ATBTLC1000 Recommended Operating Conditions

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	I/O Supply Voltage Low Range	1.62	1.80	2.00	V
$VDDIO_M$	I/O Supply Voltage Mid-Range	2.00	2.50	3.00	
$VDDIO_H$	I/O Supply Voltage High Range	3.00	3.30	3.60	
VBATT	Battery Supply Voltage [1]	1.80	3.60	4.30	
	Operating Temperature	-40		85	°C

Note:

1. VBATT must not be less than VDDIO.
2. When powering up the device, VBATT must be greater or equal to 1.9 V to ensure that BOD does not trigger. BOD threshold is typically 1.8 V and the device is held in reset if VBATT is near this threshold on startup. After startup, BOD can be disabled and the device can operate down to 1.8 V.

11.3 DC Characteristics

The following table provides the DC characteristics for the ATBTLC1000 digital pads.

Table 11-3. ATBTLC1000 DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage VIL	-0.30		0.60	V
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			
$VDDIO_M$	Input Low Voltage VIL	-0.30		0.63	
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			
$VDDIO_H$	Input Low Voltage VIL	-0.30		0.65	
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			
All	Output Loading			20	pF
	Digital Input Load			6	

.....continued

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Pad drive strength (regular pads(1))	1.7	2.5		mA
$VDDIO_M$	Pad drive strength (regular pads)	3.4	6.6		
$VDDIO_H$	Pad drive strength (regular pads)	10.5	14		
$VDDIO_L$	Pad drive strength (high-drive pads(1))	3.4	5.0		
$VDDIO_M$	Pad drive strength (high-drive pads)	6.8	13.2		
$VDDIO_H$	Pad drive strength (high-drive pads)	21	28		

Note:

1. The GPIO_8, and GPIO_9 are high-drive pads and all other pads are regular.

11.4 Current Consumption in Various Device States

The following table provides the current consumption details in different device states.

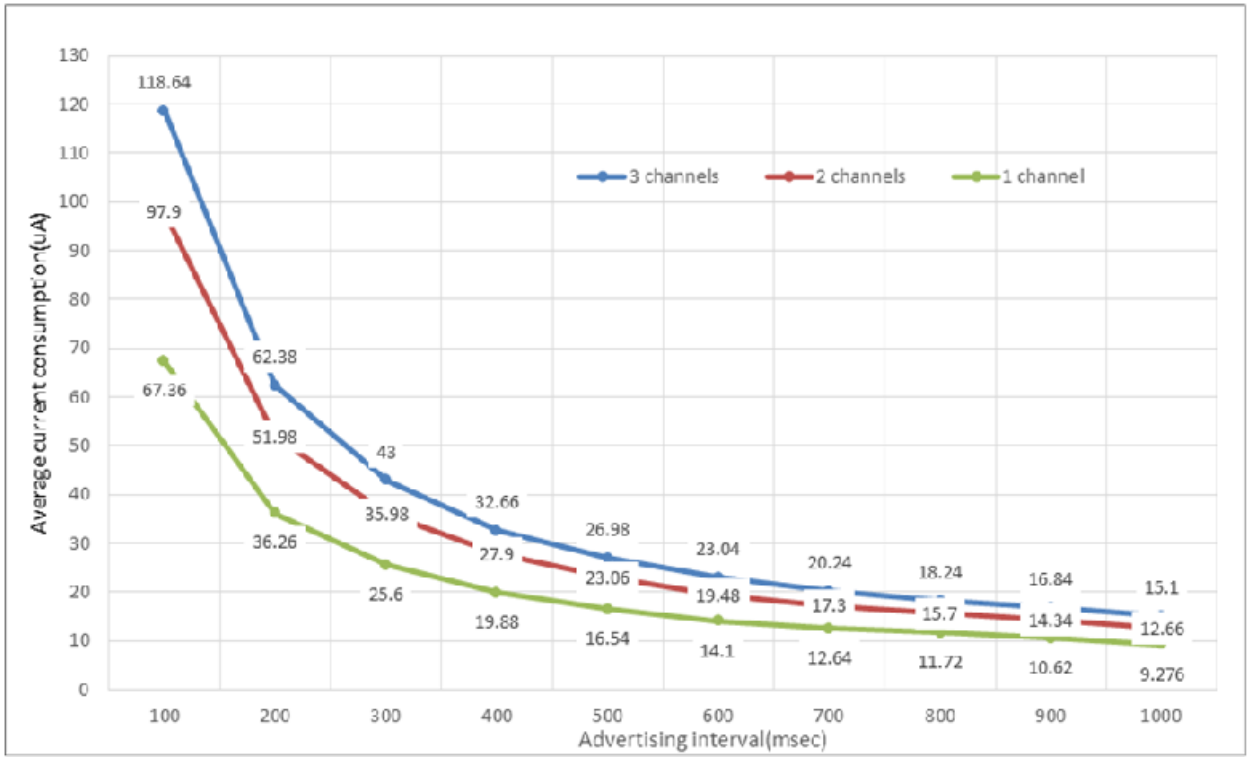
Table 11-4. ATBTLC1000 QFN Device State Current Consumption

Device State	C_EN	VDDIO	$I_{VBAT}+I_{VDDIO}$ (typical) (2)
Power_Down	Off	On	0.05 µA
Ultra_Low_Power with BLE timer, with RTC (1)	On	On	2.01 µA
BLE_On_Receive at channel 37 (2402 MHz)	On	On	5.24 mA
BLE_On_Transmit, 0 dBm output power at channel 37 (2402 MHz)	On	On	3.91 mA
BLE_On_Transmit, 0 dBm output power at channel 39 (2480 MHz)	On	On	3.78 mA
BLE_On_Transmit, 3 dBm output power at Channel 37 (2402 MHz)	On	On	4.74 mA
BLE_On_Transmit, 3 dBm output power at Channel 39 (2480 MHz)	On	On	4.60 mA

Note:

1. Sleep clock derived from external 32.768 kHz crystal specified for CL=7 pF, using the default on-chip capacitance only, without using external capacitance.
2. Measurement conditions
   - VBAT=3.3V
   - VDDIO=3.3V
   - Temperature=25°C
   - These measurements are taken with FW BluSDK V6.1.7072

Figure 11-1. ATBTLC1000 Average Advertising Current



Note:

1. The average advertising current is measured at VBAT = 3.3 V, VDDIO = 3.3 V, TX output power=0 dBm. Temperature=25°C
2. Advertisement data payload size - 31 octets
3. Advertising event type - Connectable Undirected
4. Advertising channels used in 2 channel - 37 and 38
5. Advertising channels used in 1 channel - 37

11.5 Receiver Performance

The following table explains the ATBTLC1000 BLE Receiver performance.

Table 11-5. ATBTLC1000 BLE Receiver Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz

.....continued

Parameter	Minimum	Typical	Maximum	Unit
Sensitivity with on-chip DC/DC	-94.5	-93		dBm
Maximum receive signal level		+5		
CCI		12.5		dB
ACI (N±1)		0		
N+2 Blocker (Image)		-20		
N-2 Blocker		-38		
N+3 Blocker (Adj. Image)		-35		
N-3 Blocker		-43		
N±4 or greater		-45		
Intermod (N+3, N+6)		-32		dBm
OOB (2 GHz < f < 2.399 GHz)	-15			dBm
OOB (f < 2 GHz or f > 2.5 GHz)	-10			

All measurements are performed at 3.6 V VBATT and 25°C, with tests following the Bluetooth standard tests.

11.6 Transmitter Performance

The transmitter has fine step power control with P_{out} variable in <3 dB steps below 0 dBm and in <0.5 dB steps above 0 dBm.

Table 11-6. ATBTLC1000 BLE Transmitter Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Output power range	-55	0	3.5	dBm
Maximum output power		3.5		
In-band spurious (N±2)		-45		
In-band spurious (N±3)		-50		
2^{nd} harmonic P_{out}	-41			
3^{rd} harmonic P_{out}	-41			
4^{th} harmonic P_{out}	-41			
5^{th} harmonic P_{out}	-41			
Frequency deviation		±250		kHz

Note:

1. At 0 dBm TX output power.

All measurements are performed at 3.6V VBATT and 25°C, with tests following the Bluetooth standard tests.

11.7 ADC Characteristics

The following table details the static performance of SAR ADC.

Table 11-7. Static Performance of SAR ADC

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0		VBAT	V
Resolution			11		bits
Sample rate			100	1000	KSps
Input offset	Internal VREF	-10		+10	mV
Gain error	Internal VREF	-4		+4	%
DNL	100 KSps. Internal VREF=1.6 V. Same result for external VREF.	-0.75		+1.75	LSB
INL	100 KSps. Internal VREF=1.6 V. Same result for external VREF.	-2		+2.5	
THD	1 kHz sine input at 100 KSps		73		dB
SINAD	1 kHz sine input at 100 KSps		62.5		
SFDR	1 kHz sine input at 100 KSps		73.7		
Conversion time			13		cycles
Current consumption	Using external VREF, at 100 KSps		13.5		µA
	Using internal VREF, at 100 KSps		25.0		
	Using external VREF, at 1 MSps		94		
	Using internal VREF, at 1 MSps		150		
	Using internal VREF, during VBATT monitoring		100		
	Using internal VREF, during temperature monitoring		50		
Internal reference voltage	Mean value using VBAT at 2.5 V		1.026 (1)		V
	Standard deviation across parts		10.5		mV
VBATT sensor accuracy	Without calibration	-55		+55	
	With offset and gain calibration	-17		+17	

.....continued

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature sensor accuracy	Without calibration	-9		+9	°C
	With offset calibration	-4		+4	

Note:

1. Effective VREF is 2x internal reference voltage.

T_c = 25°C, V_{BAT} = 3.0 V, unless otherwise noted.

Figure 11-2. INL of SAR ADC

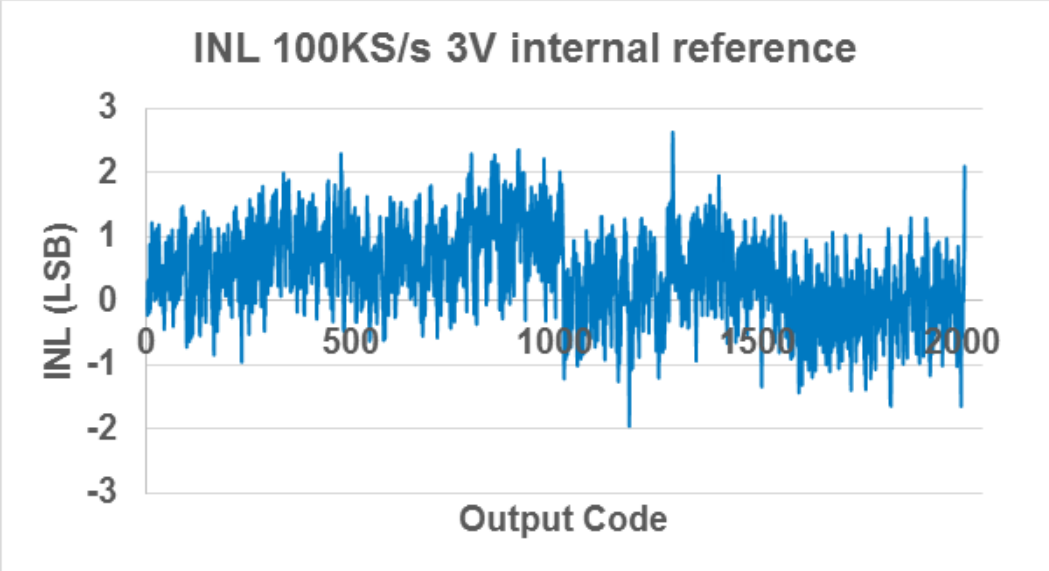


Figure 11-3. DNL of SAR ADC

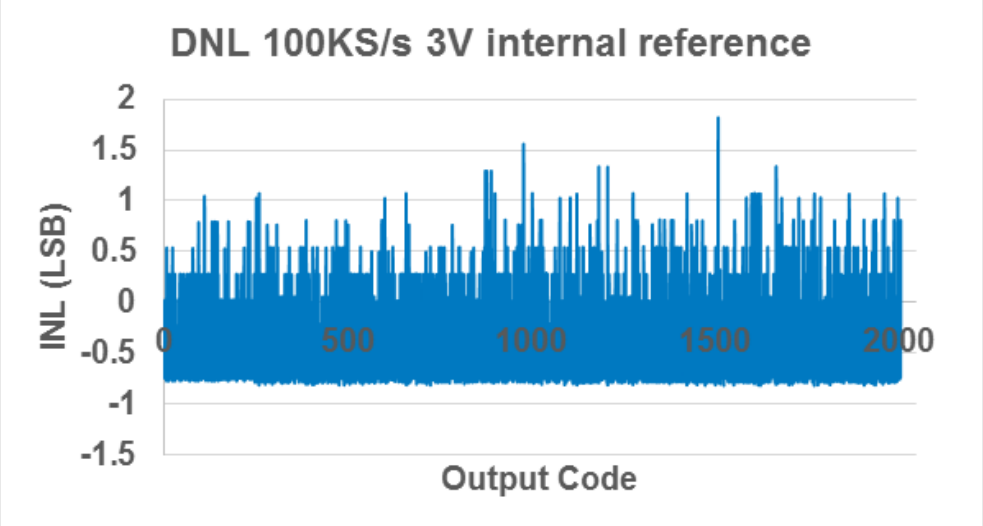


Figure 11-4. Sensor ADC Dynamic Measurement with Sinusoidal Input

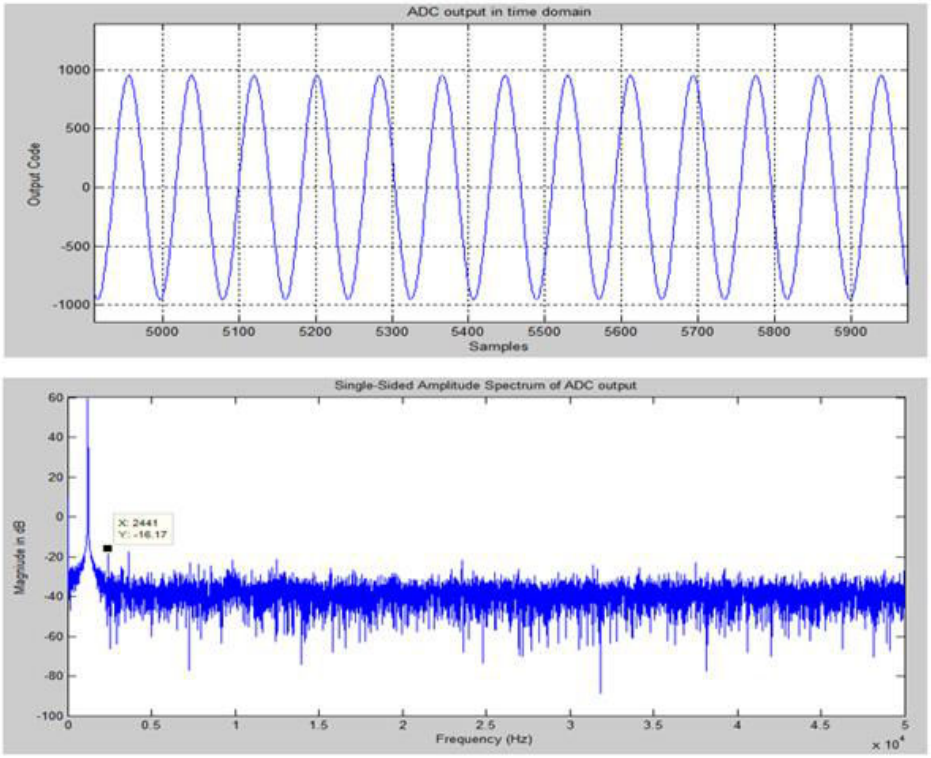
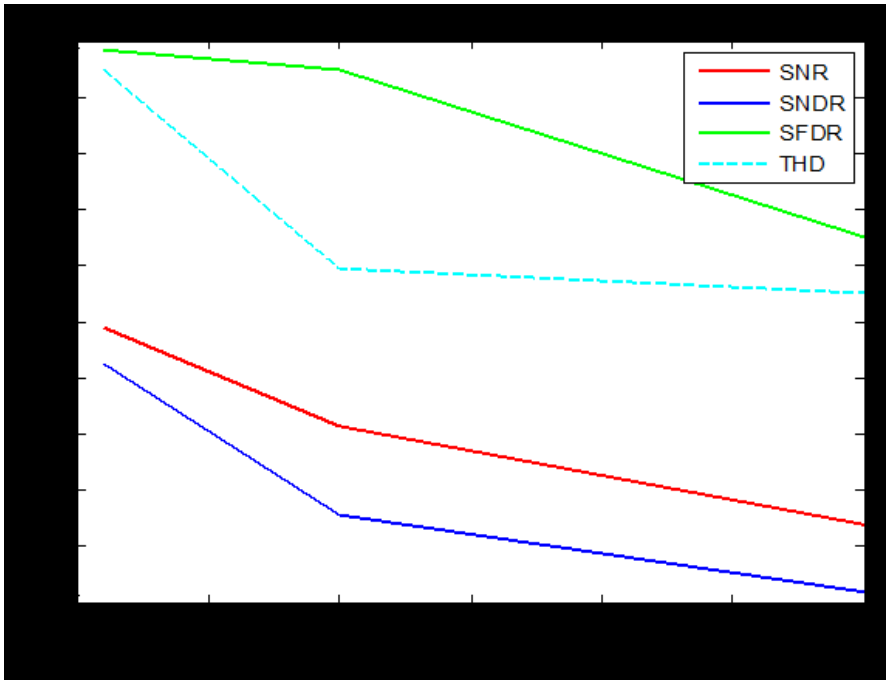


Figure 11-5. Figure 10-11. Sensor ADC Dynamic Performance Summary at 100 KSps



11.8 Timing Characteristics

This section provides timing characteristics of various interfaces.

11.8.1 I²C Interface Timing

The I²C interface timing (common to slave and master) is provided in the following figure. The timing parameters for Slave and Master modes are specified in the following tables, respectively.

Figure 11-6. ATBTLC1000 I²C Slave Timing Diagram

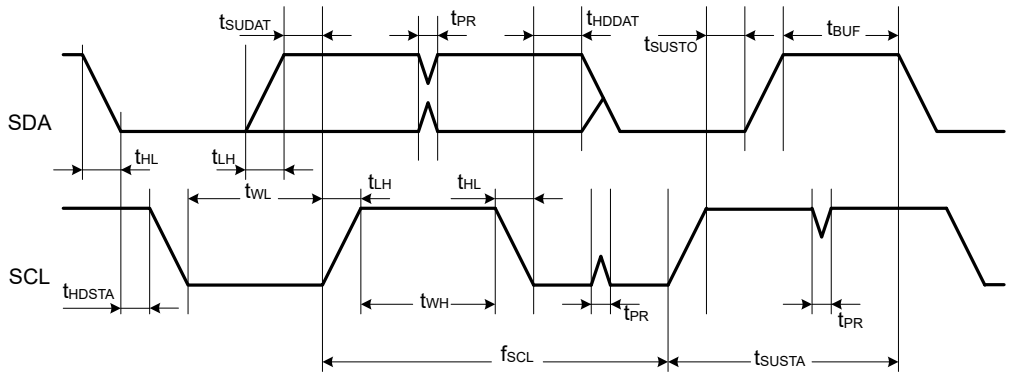


Table 11-8. ATBTLC1000 I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus free time between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

Table 11-9. ATBTLC1000 I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup Time	t_{SUSTO}	4		0.6		0.16		µs
Bus free time between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

11.8.2 SPI Slave Timing

The SPI slave timing is provided in the following figure and table.

Figure 11-7. ATBTLC1000 SPI Slave Timing Diagram

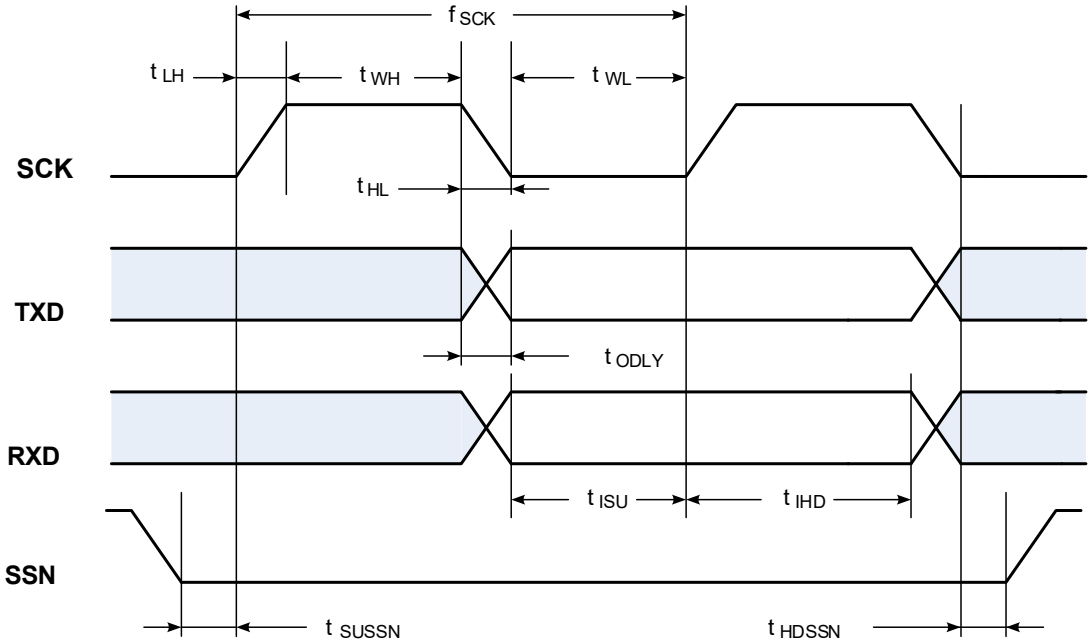


Table 11-10. ATBTLC1000 SPI Slave Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency (2)	f_{SCK}		2	MHz
Clock Low Pulse Width	t_{WL}	55		ns
Clock High Pulse Width	t_{WH}	55		
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay (3)	t_{ODLY}	7	28	
RXD Input Setup Time	t_{ISU}	5		
RXD Input Hold Time	t_{IHD}	10		
SSN Input Setup Time	t_{SUSSN}	5		
SSN Input Hold Time	t_{HDSSN}	10		

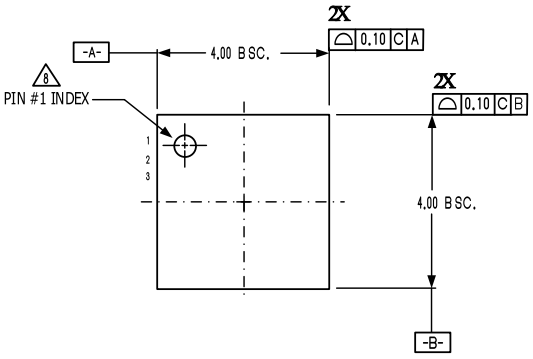
Note:

1. Timing is applicable to all SPI modes.
2. Specified maximum clock frequency is limited by the SPI slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15 pF output loading.

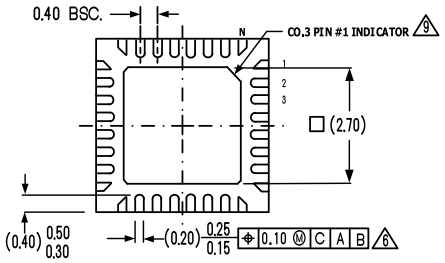
12. Package Drawing

The ATBTLC1000-QFN package is RoHS/green compliant.

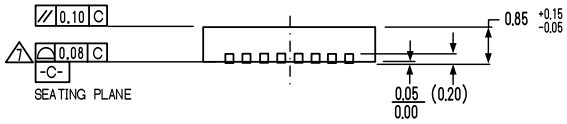
Figure 12-1. ATBTLC1000 4x4 QFN 32 Package Outline Drawing



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES:

1. PACKAGE DIMENSION CONFORM TO EDEC MO-220.
2. DIMENSIONING AND TOLERANCEING CONFORM TO ASME Y 14.5m – 1994.
3. ALL DIMENSION ARE IN MILLIMETER ( ) IS REFERENCE.
4. MAXIMUM ALLOWABLE BURR SHALL NOT EXCEED 0.05MM
5. LEAD NUMBERS START WITH THE #1 AND CONTINUE COUNTERCLOCKWISE TO LEAD #32 FROM THE TOP.
6. LEAD WIDTH IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE LEAD TIP.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
8. PIN #1 INDEX MUST BE INDICATED BY LASER MARK.
9. PAD MUST BE SOLDERED TO GND.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS			
SCALE: NONE	DATE: 10/11/11		TITLE: VQFN 4 X 4 MM, 32 LEAD (SAW TYPE) EPP 2.70 X 2.70MM PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS		
PROJECTION UNLESS SPECIFIED	FRAC: ±0.10 .XX ±0.05 .XXX ±0.03 ANGLE ±1°		

13. Reference Design

Figure 13-1. ATBTLC1000 QFN Reference Design (4-wire)

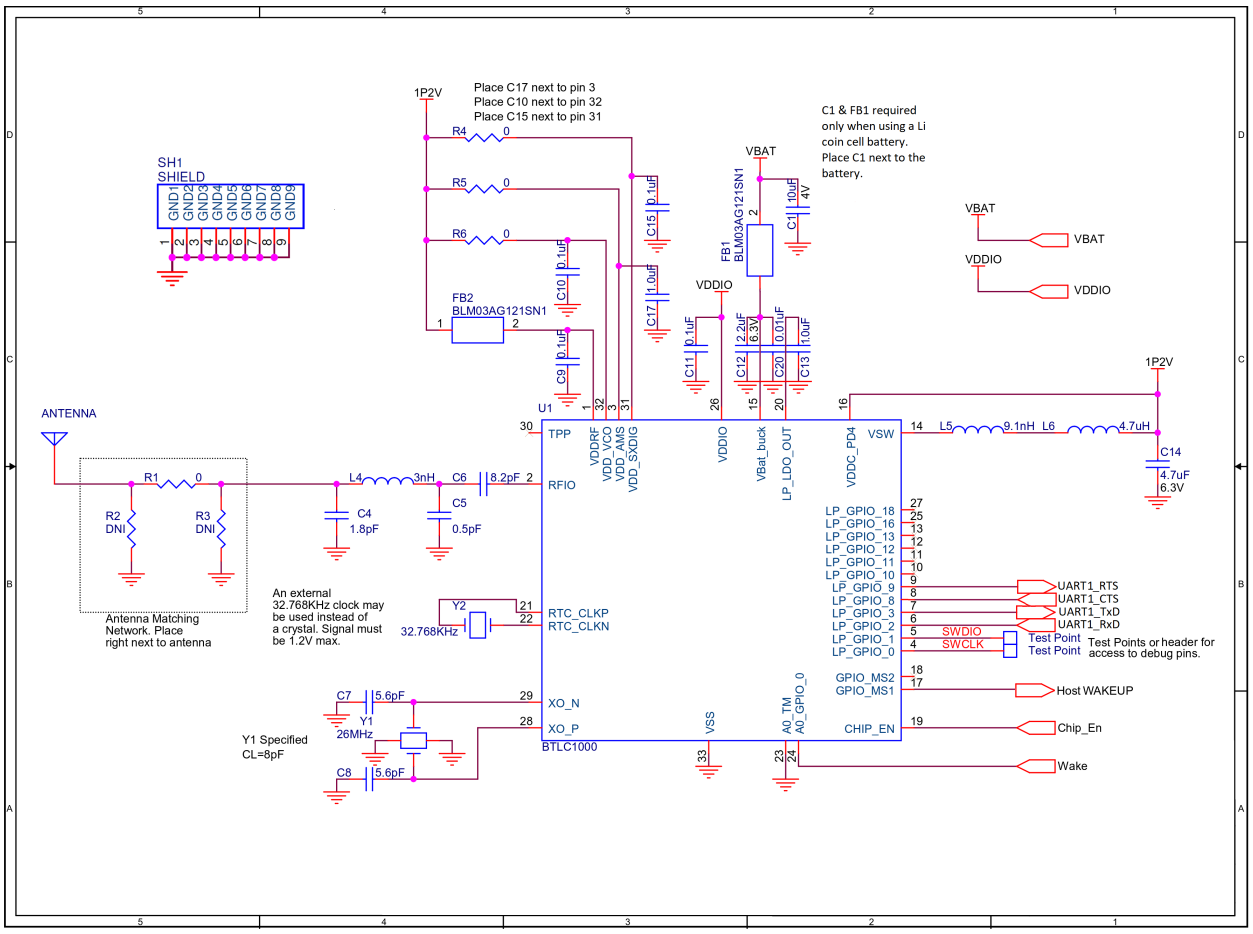
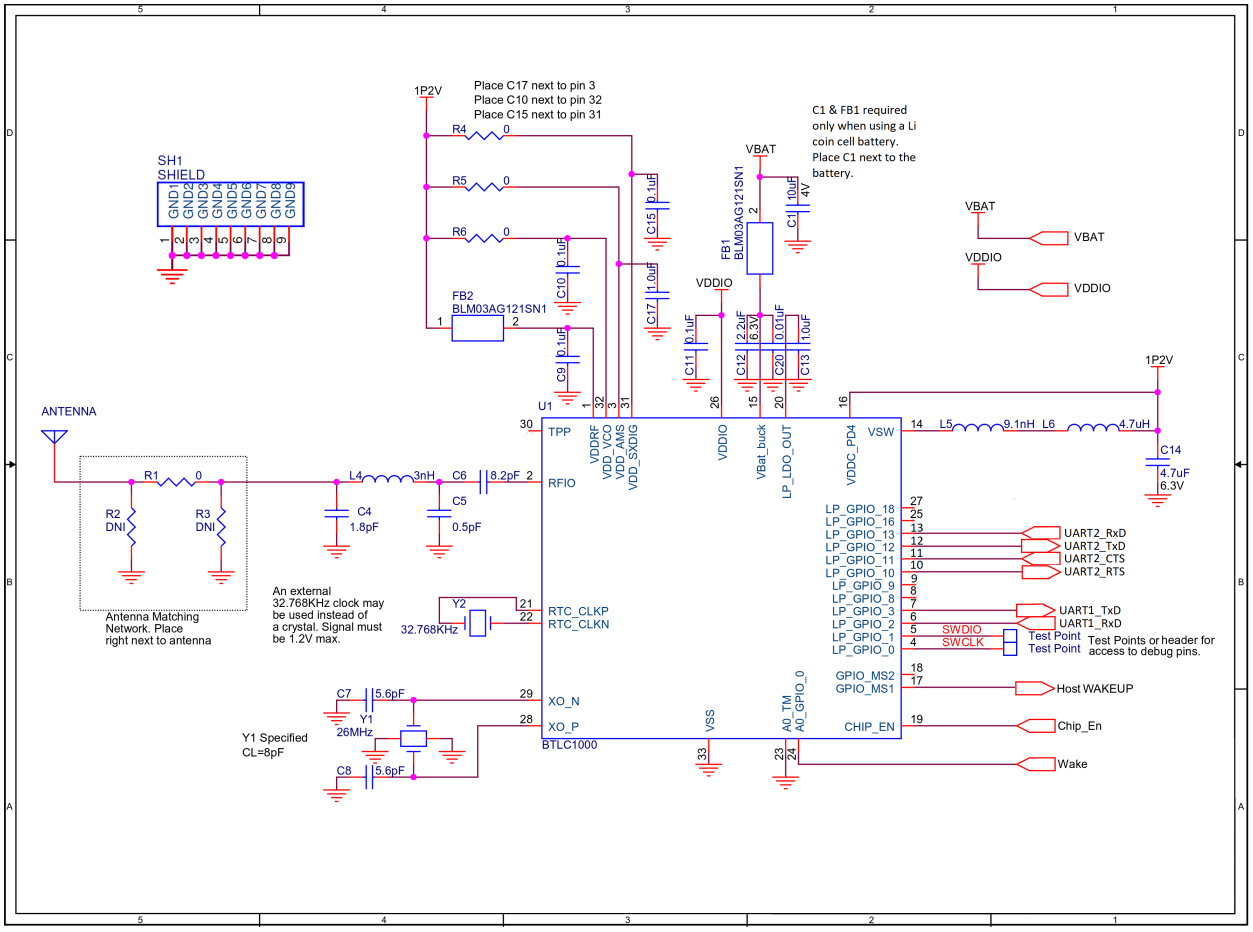


Figure 13-2. ATBTLC1000 QFN Reference Design (6-wire)



14. Bill of Material

Table 14-1. ATBTLC1000 QFN BOM

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
1	1	ANTENNA		Antenna, 2.4-2.5 GHz, 50 ohm, -40-+85°C		
2	4	R1, R4, R5, R6	0	RESISTOR, Thick Film, 0 ohm, 0201	Panasonic®	ERJ-1GN0R00C
3	2	R2, R3	DNI	RESISTOR, Thick Film, 0 ohm, 0201	Panasonic®	ERJ-1GN0R00C
4	1	C1	10 µF	CAP, CER, 10 µF, 20%, X5R, 0402, 4V, -55-125 °C	TDK Corporation	C1005X5R0G106M
5	1	C4	1.8 pF	CAP, CER, 1.8 pF, 0.1 pF, NPO, 0201, 25V, -55-125 °C	TDK Corporation	C0603C0G1E1R8C
6	1	C5	0.5 pF	CAP, CER, 0.5 pF, 0.1 pF, NPO, 0201, 25V, -55-125 °C	Murata	GRM0335C1ER50BA0
7	1	C6	8.2 pF	CAP, CER, 8.2 pF, 0.1 pF, NPO, 0201, 25V, -55-125 °C	Murata	GRM0335C1E8R2DDC1
8	2	C7, C8	5.6 pF	CAP, CER, 5.6 pF, 0.5 pF, NPO, 0201, 25V, -55-125 °C	TDK Corporation	C0603C0G1E5R6D030BA

.....continued

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
9	4	C9, C10, C11, C15	0.1 µF	CAP, CER, 0.1 µF, 10%, X5R, 0201, 6.3V, -55-85 °C	Murata	GRM033R60J104KE19D
10	1	C12	2.2 µF	CAP, CER, 2.2 µF, 10%, X5R, 0402, 6.3V, -55-85 °C	TDK Corporation	C1005X5R0J225K
11	2	C13, C17	1.0 µF	CAP, CER, 1.0 µF, 20%, X6S, 0201, 4V, -55-85 °C	Murata	GRM033C80G105MEA2D
12	1	C14	4.7 µF	CAP, CER, 4.7 µF, 10%, X5R, 0402, 6.3V, -55-85 °C	TDK Corporation	C1005X5R0J475K050BC
13	1	C20	0.01 µF	CAP, CER, 0.01 µF, 10%, X5R, 0201, 10V, -55-85 °C	Murata	GRM033R61A103KA01D
14	2	FB1, FB2	BLM03AG121SN1	FERRITE, 120 OHM at 100 MHz, 200 mA, 0201, -55-125 °C	Murata	BLM03AG121SN1
15	1	L4	3 nH	Inductor, 3 nH, 0.2 nH, Q=13 at 500 MHz, SRF=8.1 GHz, 0201, -55-125 °C	Taiyo Yuden Co., Ltd.	HKQ0603S3N0C-T

.....continued

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
16	1	L5	9.1 nH	INDUCTOR, Multilayer, 9.1 nH, 5%, 300 mA, 0.26 ohms Q=8 at 100 MHz, -55C-125 ° C, 0402	Murata	LQG15HS9N1J02D
17	1	L6	4.7 µH	INDUCTOR, unshielded, 4.7 µH, 20%, 120 mA Saturation, 0.5 ohms, SRF=80 MHz, 0603, -55-125 °C	TDK Corporation	MLZ1608M4R7WT000
18	1	SH1	SHIELD	Shield, 9 pin		
19	1	U1	BTLC1000	IC, BLE, 32QFN	Microchip Technology Inc.	ATBTLC1000A-MU-T
20	1	Y2	32.768kHz	CRYTSAL, 32.768 kHz, +/-20 ppm, -40-+85 °C, CL=7 pF, 2 lead, SM	ECS	ECS-.327-7-34B-TR
21	1	Y1	26 MHz	CRYSTAL, 26 MHz,CL=8 pF, 20 ppm temp., -40-85 °C, ESR=80, 2.5x2 mm	Taitien	A0183-X-001-3
22	2	TP1, TP2	Non-component	Test point, Surface Mount, 0.040"sw w/ 0.25" hole	40x40_SM_TEST_POINT	

15. ATBTLC1000-QFN Design Considerations

15.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias.
- To avoid electromagnetic field blocking, keep any large metal objects as far away from the antenna as possible.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4 GHz to 2.5 GHz frequency band away from the antenna, and shield those components if possible. Any noise radiated from the host board in this frequency band degrades the sensitivity of the module.

15.1.1 Power and Ground

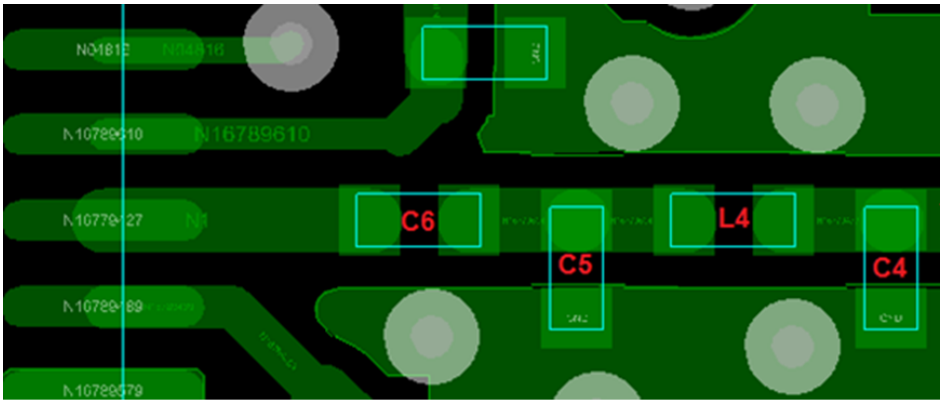
- Dedicate the layer immediately below the layer containing the RF traces from the ATBTLC1000 for ground. Make sure that this ground plane does not get broken up by routes.
- Power traces can be routed on all layers except the ground layer.
- Power supply routes must be heavy copper fill planes to insure low inductance.
- The power pins of the ATBTLC1000 must have a via directly to the power plane, close to the power pin.
- Decoupling capacitors must have a via next to the capacitor pin and this via must be directly connected to the power plane. Avoid long trace for this connection.
- The ground pad of the decoupling capacitor must have a via directly to the ground plane.
- Each decoupling capacitor must have its own via directly to the ground plane and directly to the power plane next to the pad.
- The decoupling capacitors must be placed as close as possible to the pin that it is filtering.

15.1.2 RF Traces and Components

- The RF trace from RFIO (pin 2) of the ATBTLC1000 to the antenna feed point must be 50Ω single ended controlled impedance trace. This trace must be routed in reference to the ground plane. This ground reference plane must extend entirely under the ATBTLC1000 QFN package.
- Discuss with the PCB vendor to get the available PCB stack-ups and determine the trace dimensions for achieving 50Ω single ended controlled impedance.
- Do not have any signal traces below/adjacent to the RF trace in the PCB.
- Be sure that the route from RFIO (pin 2) to the antenna is as short as possible to reduce path losses and to mitigate the trace from picking-up noise.
- Place guard ground vias on eiter side of the RF trace running from module to the antenna feed point, in the PCB.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended to have a 3x3 grid of ground vias solidly connecting the exposed ground paddle of the ATBTLC1000 to the ground plane on the inner/other layers of the PCB. This will act as a good ground and thermal conduction path for the ATBTLC1000.

- Be sure to place the DC blocking capacitor (C4) and matching components (C5, L4, C4) as close to the RFIO pin as possible. The following figure shows the placement and routing of these components.

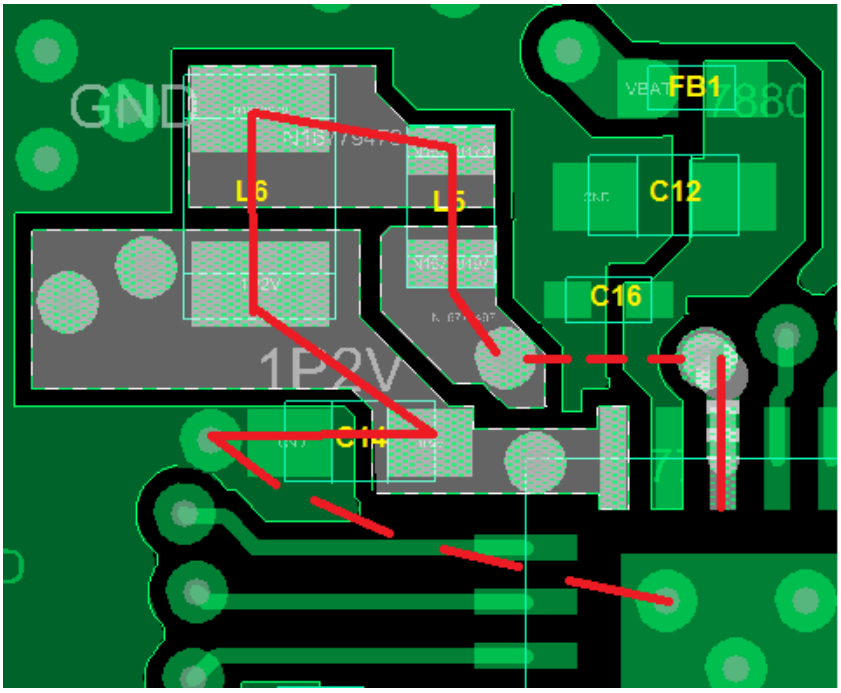
Figure 15-1. Placement and Routing of DC Blocking Cap and Matching Components



15.1.3 Power Management Unit

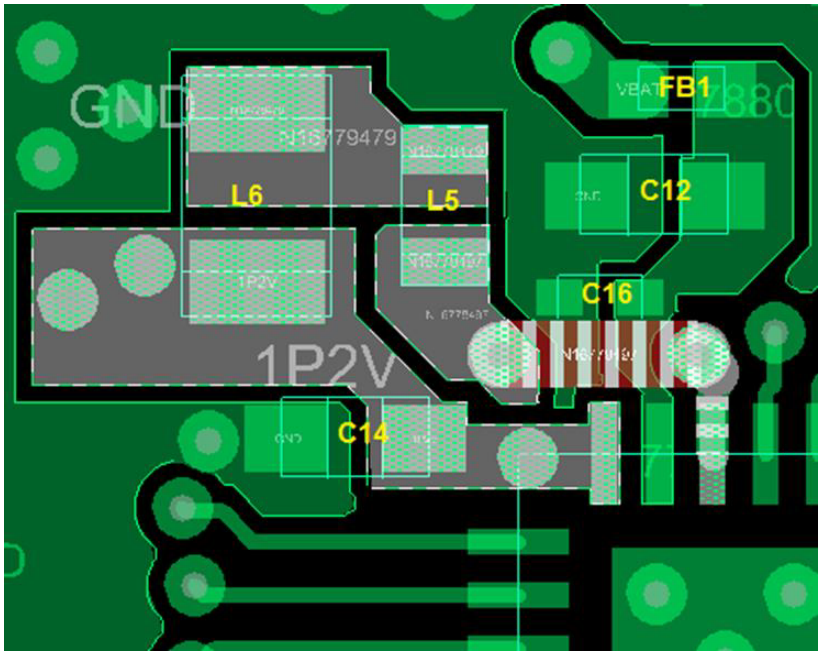
The ATBTLC1000 contains an on-chip switching regulator, which regulates the VBAT supply down to approximately 1.2V for supplying the rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise, which can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, L5 = 15nH and L6 = 4.7µH and a capacitor, C14 = 4.7µF. These components must be placed as close as possible to ATBTLC1000 pin 14. The smaller inductor, L5, must be placed closest to pin 14. Current will flow from pin 14, through L5, then L6, and then through C14 to ground and back to the center ground paddle of the ATBTLC1000 package. Place components so this current loop is as small as possible. Make sure there is a ground via to the inner ground plane right next to the ground pin of C14. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATBTLC1000 ground pad will result in incorrect operation of the on-chip switching regulator. The following figure shows an example placement and routing of these components.

Figure 15-2. Placement and Routing of PMU Components



The current loop described above is indicated by the red line, with the dashed portions indicating the path on inner layers. The route from pin 14 to L5 is on an inner layer and is shown in the following figure in red/white.

Figure 15-3. Inner Layer PMU Route



Placement of FB1, C12, and C16 should be as close as possible to the VBAT_BUCK pin (pin 15), with the smaller capacitor, C16, placed closest to the pin. Again, the route should be as heavy as possible to provide a low-impedance path. The placement and routing of these components is shown in Figure 15-2.

Note that the PMU is a switching regulator and produces noise within the 2.4 GHz receive band. Therefore it is essential that the RF route, components, and antenna be kept as far away from the PMU and its components (L5, L6, and C14) as possible.

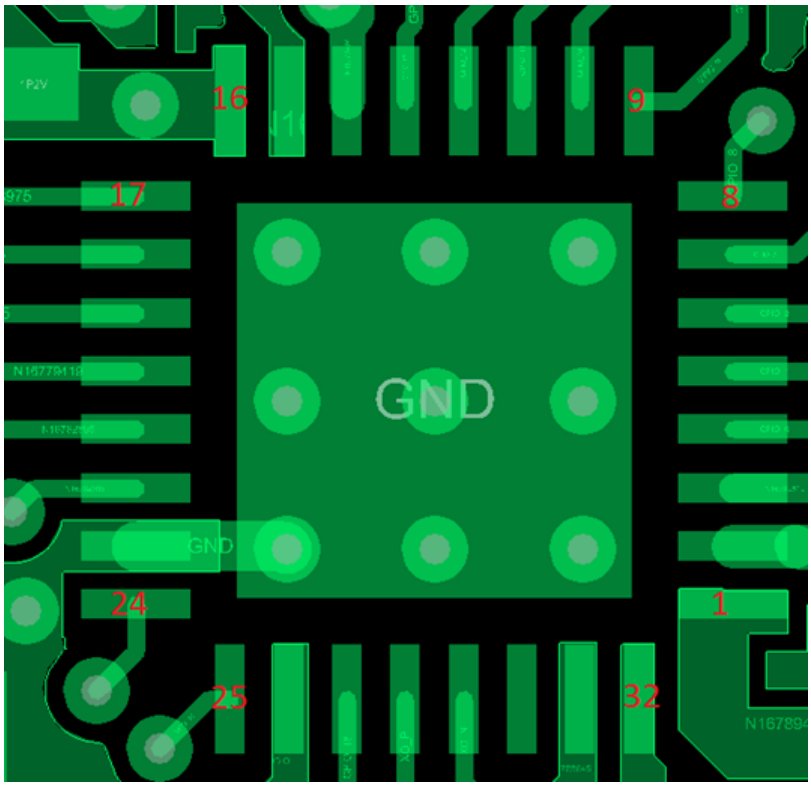
The same goes for the VBAT_Buck supply. This is the supply for the PMU and noise from the PMU feeds back to this supply pin. FB1 is used to suppress this noise to keep it from radiating from the supply route. Therefore, the RF route should also be kept away from the VBAT_Buck supply route and FB1, C12, and C16.

A shield should be placed over the ATBTLC1000 and PMU components to keep any RF radiation from being picked up by the antenna.

15.1.4 Ground

The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias. These ground vias must surround the perimeter of the pad. One of these ground vias must be in the center pad as close as possible to pin 2 (RFIO). This ground via serves as the RF ground return. There must also be a ground via in the center pad as close as possible to pin 14. This is the ground return for the PMU. See the following figure for an example of the recommended grounding of the center pad.

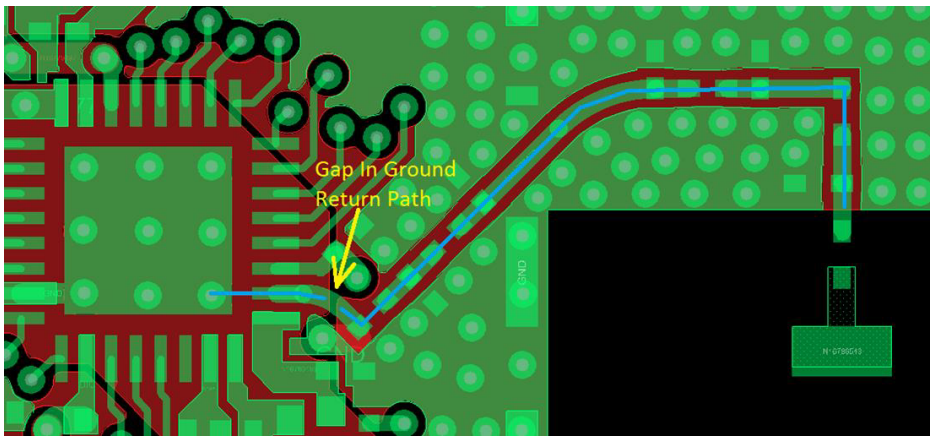
Figure 15-4. Proper Grounding of Center Ground Pad



As mentioned in 15.1.1 Power and Ground, one inner layer should be dedicated as a ground plane. It is important that the ground return currents have direct low-impedance path back to the device ground. This is critical for the RF and PMU ground returns. The following figure shows the top layer RF path route superimposed over an example of an incorrect second layer ground. In the following figure the top layer is shown in green and the second layer is shown in red. The RF route is indicated as a blue line. The RF return current will flow back along this path to the package ground pin closest to the RFIO pin (pin 2); however, as shown in the following figure, a gap exists in the ground plane blocking the return current.

This discontinuity in the ground will affect the RF performance and must be avoided. This example also shows the placement of ground vias in the center paddle. Note that there is a ground via placed directly next to the RFIO pin.

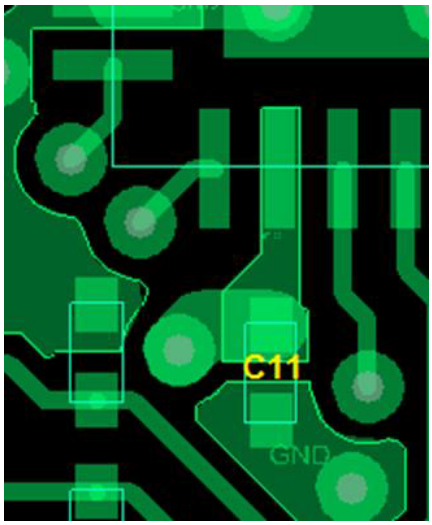
Figure 15-5. Example of an Incorrect Ground Plane



15.1.5 VDDIO

The VDDIO (pin 26) is a supply input pin and the trace to this pin must be of adequate width. The decoupling capacitor for this supply (C11) should be placed as close as possible to the pin. The following figure shows the placement of the decoupling capacitor and the trace to this power pin.

Figure 15-6. VDDIO Route and Decoupling Capacitor Placement



15.1.6 LP_LDO_OUT

LP_LDO_OUT (pin20) is the output of an on-chip regulator. It requires a 1µF ceramic capacitor (C13) to be placed as close as possible to the pin.

15.1.7 Sensitive Traces

The following pins are sensitive to noise and the trace to these pins must be as short as possible. Keep these traces isolated from all other signals by routing them far away from other traces or by using guard ground vias to shield them. On layers above and below these traces, avoid routing any noisy signals:

- XO_N (pin 29)
- XO_P (pin 28)

- RFIO (pin 2)

15.1.8 Supply Pins

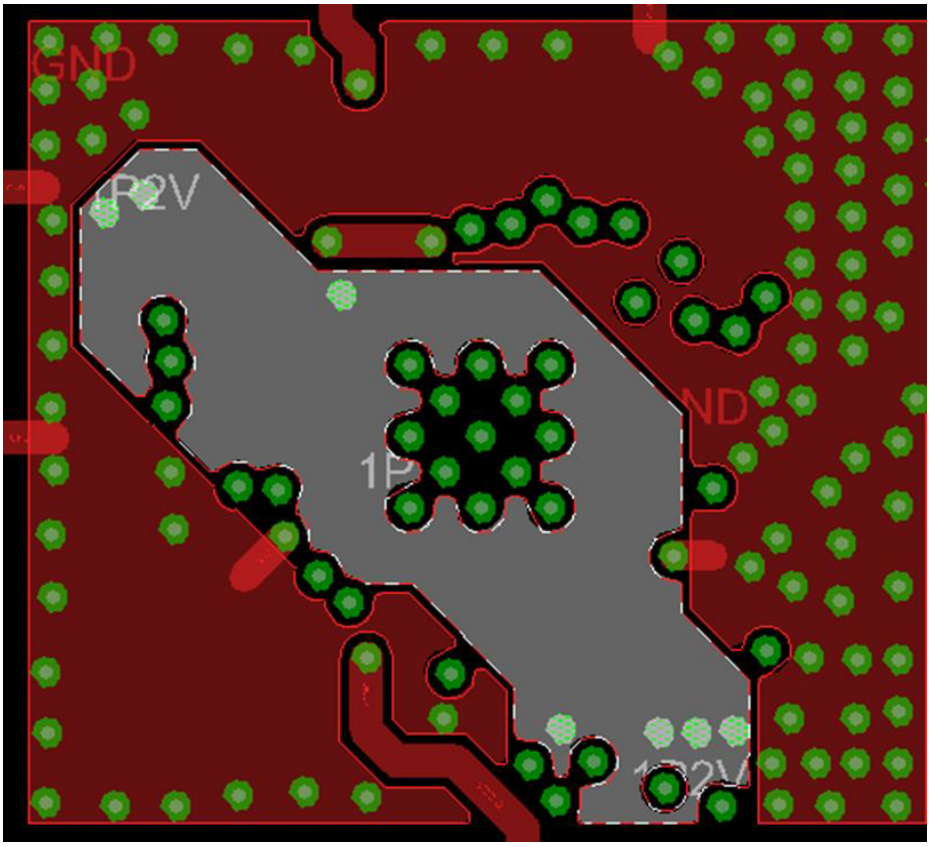
The following are power supply pins for the ATBTLC1000. They are supplied with approximately 1.2V by the on-chip PMU. It is important that the decoupling capacitors for these supplies are placed as close to the ATBTLC1000 pin as possible. It is necessary to reduce the trace inductance between the capacitor and ATBTLC1000 power pin:

- VDD_RF (pin 1)
- VDD_AMS (pin 3)
- VDDC_PD4 (pin16)
- VDD_SXDIG (pin 31)
- VDD_VCO (pin 32)

Place one 0.1µF capacitor as close as possible to pins 31 and 32. Place a 1µF capacitor as close as possible to pin 3.

The route going from C14 in the reference schematic to pins 1, 3, 16, 31, and 32 is a power route. It should be as short and thick as possible. Try to route it as a power plane on an inner layer. An example of a route of this supply on an inner layer of a PCB is shown in grey in the following figure. The three vias in the upper left portion go to C14 and the 1.2V route on the top layer, visible in Figure 15-2. The via below and to the right goes to ATBTLC1000 pin 16 and vias in the bottom right go to pins 1, 3, 31, and 32.

Figure 15-7. Routing of 1P2V Supply



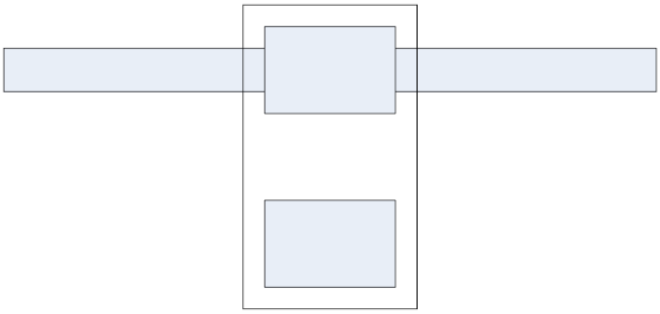
Additionally, while the VBAT_BUCK (pin 15) supply is not sensitive to picking up noise, it is a noise-generating supply. Therefore, keep the decoupling capacitors for this supply pin as close as possible to

the VBAT_BUCK pin and make sure that the route for this supply stays far away from sensitive pins and supplies.

15.1.9 Additional Suggestions

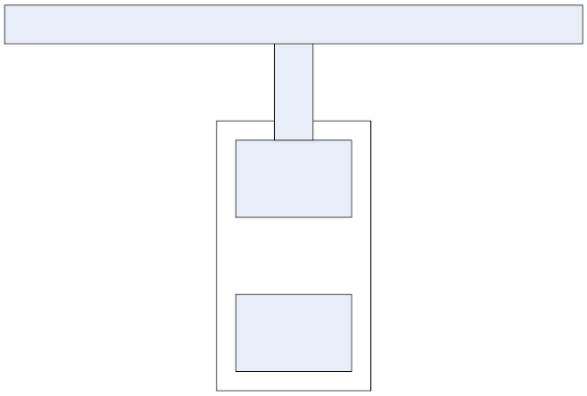
Make sure that traces route directly through the pads of all filter capacitors and not by a stub route. The following figure shows the correct way to route through a capacitor pad.

Figure 15-8. Correct Routing Through Capacitor Pad



The following figure shows a stub route to the capacitor pad. This should be avoided, as it adds additional impedance in series with the capacitor.

Figure 15-9. Incorrect Stub Route To Capacitor Pad



15.2 Interferers

One of the major problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise-generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also, make sure that no traces route underneath the RF portion of the ATBTLC1000, and no traces route underneath any of the RF traces from the antenna to the ATBTLC1000 input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

15.3 Antenna

Be sure to choose an antenna that covers the frequency band 2.400 GHz to 2.500 GHz and is designed for a 50Ω feed point.

Follow the antenna vendor’s recommendations for pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad.

Finally, make sure that the antenna matching components are placed as close to the antenna pad as possible.

16. Assembly Information

This section provides storage conditions, banking conditions and guidelines for reflow processes in soldering the ATBTLC1000 to the customer's design.

16.1 Storage Conditions

16.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored at a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product is 12 months from the date the bag is sealed.

16.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

16.2 Baking Conditions

The ATBTLC1000 is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours as long as the devices are held at ≤ 30ºC/60% RH or stored at <10% RH.

The ATBTLC1000 requires baking before mounting if:

- The sealed bag has been open for more than 168 hours
- Humidity indicator card reads more than 10%
- SIPs need to be baked for eight hours at 125ºC

16.3 Reflow Profile

For reflow process guidelines, refer to the *Solder Reflow Recommendation Application Note* (http://ww1.microchip.com/downloads/en/appnotes/00233d.pdf).

17. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 17-1. Reference Documents

Title	Content
Datasheet	This document
ATBTLC1000 BluSDK Release Package	This package contains the software development kit and all the necessary documentation including getting started guides for interacting with different hardware devices, device drivers, and API call references.
ATBTLC1000 BluSDK BLE API SW Development Guide	This user guide details the functional description of Bluetooth Low Energy (BLE) Application Peripheral Interface (API) programming model. This also provides the example code to configure an API for Generic Access Profile (GAP), Generic Attribute (GATT) Profile, and other services using the ATBTLC1000.
ATBTLC1000 Platform Porting Guide	This document guides the user to port the Application Peripheral Interface (API) into a new platform.
ATBTLC1000 BluSDK Example Profiles Application User's Guide	This document describes how to get started with different example applications for ATBTLC1000.
Solder Reflow Recommendation Application Note (DS00233D)	This Application Note focuses on solder reflow recommendations for packages with Matte Tin and Tin/Lead finishes.

Note: For a complete listing of development support tools and documentation, visit http://www.microchip.com/, or go to the Customer Support section for options to find the nearest Microchip field representative.

18. Document Revision History

Revision	Date	Section	Description
DS70005391A	03/2019	Document	• New Microchip document number. • Change of document style. • Change the name to incorporate all the ATBTLC1000 devices. • Various editorial changes to match the new document style.

Rev. C - 01/2016

Section	Changes
Features	• Updated numbers in feature list. • Revised Sensitivity values.
Pinout Information	• Added UART flow control to LP_GPIO pins in Pin Description table.
Power Management	• Removed 1µH Row and updated cap and ripple values in DC/DC Converter Allowable Onboard Inductor and Capacitor Values table. • Removed 1µH Row and updated cap and ripple values in Figure 6-2. • Updated BLE on Transmit/BLE on Receive values in Device State Current Consumption table. • Updated text in describing BOD handling in Power On Reset (POR) and Brown Out Detector (BOD) section • Removed BGR block from diagram in ATBTLC1000 POR and BOD Block Diagram. • Added Brownout Thresholds and POR time table.

.....continued

Section	Changes
Clocking	• Updated oscillator variations in Overview section, 2MHz and 26MHz Integrated RC Oscillators section, and 32kHz RC Oscillator Frequency Variation over Temperature figure. • Removed Supply Pins row in RTC XO Interface table. • Revised Sensitivity values in the Clocking Overview and 7.4 2MHz and 26MHz Integrated RC Oscillators sections. • Added text to Clocking Overview section regarding BLE sleep and connections. • Updated XO and RTC Clock figures. • Revised Device State Current Consumption table for consistency.
Bluetooth Low Energy (BLE) Subsystem	• Updated TX peak current values in BLE Transmitter Performance table. •
Reference Design	• Updated Reference Design schematic.
Reference BOM	• Updated BOM.
Electrical Characteristics	• Added note 2 to Recommended Operating Conditions table. • Corrected title in DC Electrical Characteristics table.
Errata	Added Errata area.
Document	Miscellaneous editorial corrections.

Rev. B - 09/2015

Section	Changes
Features	• Updated current numbers in the feature list.
Power Management	• Updated current numbers and added comments in Device State Current Consumption table. • Updated average advertising current chart.

.....continued

Section	Changes
Clocking	• Updated capacitance value in 26MHz Crystal Oscillator (XO) section. • Updated voltage value in XO Bypass Clock Specification table. • Updated capacitance value and text in 32.768kHz RTC Crystal Oscillator section. • Added 32kHz RC Oscillator performance charts in 7.4 2MHz and 26MHz Integrated RC Oscillators section.
Bluetooth Low Energy (BLE) Subsystem	• Updated Receiver performance numbers and comments in BLE Radio section. • Updated Transmitter performance numbers and comments in BLE Radio section.
External Interfaces	• Updated ADC power consumption and added comment in SAR ADC Characteristics table. • Replaced the Static Performance of SAR ADC table. • Replaced ADC performance charts: INL of SAR ADC and DNL of SAR ADC. • Added new ADC performance charts: Sensor ADC Dynamic Measurement with Sinusoidal Input and Sensor ADC Dynamic Performance Summary at 100KSPS.
Document	• BTLC1000 corrected to ATBTLC1000

Rev. A - 09/2015

Section	Changes
Document	Initial document release.

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