Features

- Operating Voltage: 3.3V
- Access Time: 40 ns
- Very Low Power Consumption

 Active: 160 mW (Max)
 - Standby: 70 µW (Typ)
- Wide Temperature Range: -55 °C to +125 °C
- MFP 32 leads 400 Mils Width Package
- TTL Compatible Inputs and Outputs
- Asynchronous
- Designed on 0.35µm Process
- No Single Event Latch-up below a LET threshold of 80 MeV/mg/cm²@125 °C
- Radiation Tolerance⁽¹⁾
 - Tested up to a Total Dose of 300 krad (Si)
- RHA capability of 100 krad (Si) according to MIL STD 883 Method 1019
 Quality grades: QML Q or V with SMD 5962-02501
- Notes: 1. tolerance to MBU's may need to be enhanced by the application

Description

The M65609E is a very low power CMOS static RAM organized as 131,072 x 8 bits.

Utilizing an array of six transistors (6T) memory cells, the M65609E combines an extremely low standby supply current with a fast access time at 40 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The M65609E is processed according to the methods of the latest revision of the MIL PRF 38535 and ESCC 9000.

It is produced on the same process as the MH1RT sea of gates series.



Rad Hard 128K x 8 3.3-volt Very Low Power CMOS SRAM

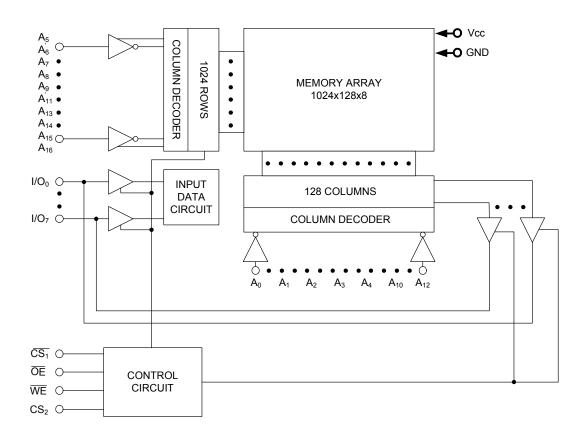
M65609E

4158J-AERO-11/13





Block Diagram



Pin Assignment

Figure 1. 32 pins Flatpack 400 MILS

VCC A4 I/02 A7 I/01 A3 A6 A8 A0 A1 CS2 I/05 A2 WE I/06	□ 1 □ 2 □ 4 □ 5 □ 6 □ 7 8 9 □ 10 11 12 13 □ 14 □ 15	~	32 31 30 29 28 27 26 27 26 27 26 21 20 19 18 18	A5 A16 I/03 A15 A12 I/04 A13 A14 A9 A10 I/08 A11 OE I/07 GND
	□ 15 □ 16			

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Pin Description

Name	Description
A0 - A16	Address Inputs
I/O1 - I/O8	Data Input/Output
CS ₁	Chip Select 1
CS ₂	Chip Select 2
WE	Write Enable
OE	Output Enable
V _{CC}	Power
GND	Ground

Table 1. Truth Table

CS ₁	CS ₂	WE	OE	Inputs/ Outputs	Mode
н	Х	Х	Х	Z	Deselect/ Power-down
Х	L	Х	Х	Z	Deselect/ Power-down
L	Н	Н	L	Data Out	Read
L	Н	L	Х	Data In	Write
L	Н	Н	Н	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.





Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage to GND Potential0.5V + 5V
DC Input Voltage GND - 0.3V to V_{CC} + 0.3V
DC Output Voltage High Z State GND - 0.3V to V_{CC} + 0.3V
Storage Temperature65.C to + 150.C
Output Current Into Outputs (Low) 20 mA
Electro Statics Discharge Voltage > 500V
(MIL STD 883D Method 3015.3)

*NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Military Operating Range

Operating Voltage	Operating Temperature
3.3V <u>+</u> 0.3V	-55·C to + 125·C

Recommended DC Operating Conditions

Parameter	Description	Min	Тур	Max	Unit
V _{cc}	Supply voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
V _{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V _{IH}	Input high voltage	2.2	_	V _{CC} + 0.3	V

Capacitance

Parameter	Description	Min	Тур	Max	Unit
C _{IN} ⁽¹⁾	Input low voltage	_	_	8	pF
C _{OUT} ⁽¹⁾	Output high voltage	-	-	8	pF

Note: 1. Guaranteed but not tested.

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DC Parameters

DC Test Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
IIX ⁽¹⁾	Input leakage current	-1	_	1	μΑ
IOZ ⁽¹⁾	Output leakage current	-1	_	1	μΑ
VOL ⁽²⁾	Output low voltage	-	_	0.4	V
VOH ⁽³⁾	Output high voltage	2.4	_	_	V

Gnd < Vin < V_{CC} , Gnd < Vout < V_{CC} Output Disabled. V_{CC} min. IOL = 4 mA. V_{CC} min. IOH = -2 mA. 1.

2.

3.

Consumption

Symbol	Description	65609E-40	Unit	Value
ICCSB ⁽¹⁾	Standby supply current	1.5	mA	max
ICCSB ₁ ⁽²⁾	Standby supply current	1	mA	max
ICCOP ⁽³⁾	Dynamic operating current	45	mA	max

1.

2.

 $\begin{array}{l} \overline{CS}_1 \geq \text{VIH or } CS_2 \leq \text{VIL and } \overline{CS}_1 \leq \text{VIL}. \\ \overline{CS}_1 \geq V_{CC} - 0.3 \text{V or, } CS_2 \leq \text{Gnd} + 0.3 \text{V and } \overline{CS}_1 \leq 0.2 \text{V} \\ \overline{F} = 1/T_{\text{AVAV}}, \ \overline{I_{\text{OUT}}} = 0 \text{ mA}, \ \overline{W} = \overline{\text{OE}} = \text{VIH}, \ \text{Vin} = \text{Gnd or } V_{CC}, \ V_{CC} \text{ max}. \end{array}$ 3.





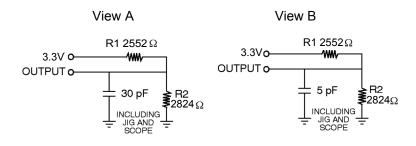
AC Parameters

Test Conditions

Temperature Range	55 +125 °C
Supply Voltage:	3.3 <u>+</u> 0.3V
Input and Output Timing Reference Levels	1.5V

Test Loads and Waveforms

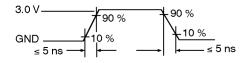




Equivalent to : THEVENIN EQUIVALENT

1340<u>Ω</u> OUTPUT **o_____0** 1.73V

Figure 3. CMOS Input Pulses



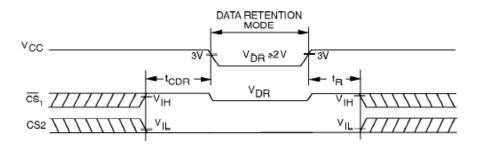
6

Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

- 1. During data retention $\overline{\text{CS1}}$ must be held high within V_{CC} to V_{CC} 0.2V or chip select $\overline{\text{CS2}}$ must be held down within GND to GND +0.2V.
- 2. Output Enable (\overline{OE}) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
- 3. During power-up and power-down transitions $\overline{\text{CS1}}$ and $\overline{\text{OE}}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}, or with BS between GND and GND -0.3V.
- 4. The RAM can begin operation > t_R ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 4. Data Retention Timing



Data Retention Characteristics

Parameter	Description	Min	Typical T _A = 25⋅C	Мах	Unit
V _{CCDR}	V_{CC} for data retention	2.0	-	-	V
T _{CDR}	Chip deselect to data retention time	0.0	-	-	ns
t _R	Operation recovery time	t _{AVAV} ⁽¹⁾	-	-	ns
I _{CCDR1} ⁽²⁾	Data retention current at 2.0V	_	0.010	1.0	mA

Notes: 1. \underline{TAVAV} = Read Cycle Time 2. $\overline{CS1}$ = V_{CC} or CS2 = $\overline{CS1}$ = \overline{GND} , V_{IN} = $\overline{GND/V_{CC}}$.





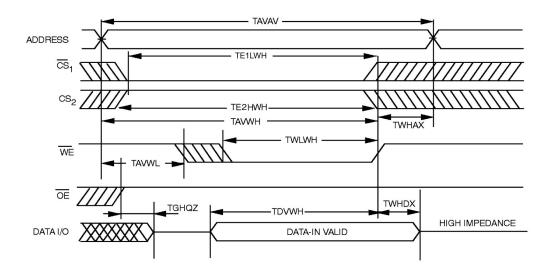
Write Cycle

Symbol	Parameter	65609E-40	Unit	Value
t _{AVAW}	Write cycle time	35	ns	min
t _{AVWL}	Address set-up time	0	ns	min
t _{AVWH}	Address valid to end of write	28	ns	min
t _{DVWH}	Data set-up time	18	ns	min
t _{E1LWH}	$\overline{\text{CS}}_1$ low to write end	28	ns	min
t _{E2HWH}	CS ₂ high to write end	28	ns	min
t _{WLQZ}	Write low to high Z ⁽¹⁾	15	ns	max
t _{wLWH}	Write pulse width	28	ns	min
t _{whax}	Address hold from to end of write	3	ns	min
t _{WHDX}	Data hold time	0	ns	min
t _{WHQX}	Write high to low Z ⁽¹⁾	0	ns	min

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see view B on Figure 2 on page 6).

Write Cycle 1

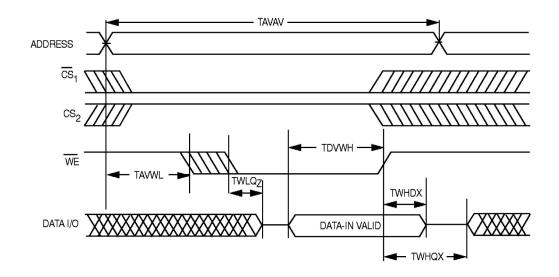
$\overline{\text{WE}} \text{ Controlled. } \overline{\text{OE}} \text{ High During Write}$



8

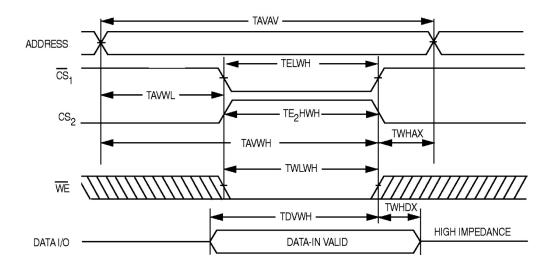


WE Controlled. OE Low





CS1 or CS2 Controlled⁽¹⁾



Note: 1. The internal write time of the memory is defined by the overlap of CS1 LOW and CS2 HIGH and W LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write. Data out is high impedance if OE = V_{IH}.



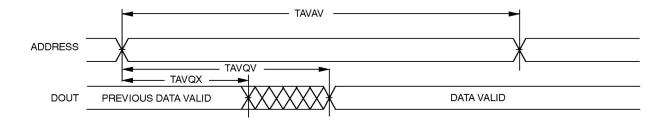


Read Cycle

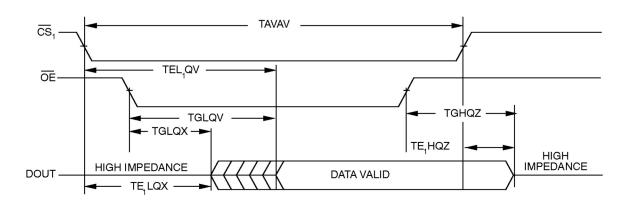
Symbol	Parameter	65609E-40	Unit	Value
t _{AVAV}	Read cycle time	40	ns	min
t _{AVQV}	Address access time	40	ns	max
t _{AVQX}	Address valid to low Z	3	ns	min
t _{E1LQV}	Chip-select ₁ access time	40	ns	max
t _{E1LQX}	$\overline{\text{CS}}_1$ low to low Z ⁽¹⁾	3	ns	min
t _{E1HQZ}	$\overline{\text{CS}}_1$ high to high Z ⁽¹⁾	15	ns	max
t _{E2HQV}	Chip-select ₂ access time	40	ns	max
t _{E2HQX}	CS ₂ high to low Z ⁽¹⁾	3	ns	min
t _{E2LQZ}	CS ₂ low to high Z ⁽¹⁾	15	ns	max
t _{GLQV}	Output Enable access time	12	ns	max
t _{GLQX}	OE low to low Z ⁽¹⁾	0	ns	min
t _{GHQZ}	\overline{OE} high to high Z ⁽¹⁾	10	ns	max

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see view B on Figure 2 on page 6).

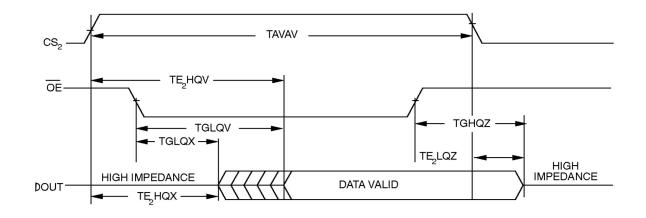
Read Cycle 1



Read Cycle 2



Read Cycle 3







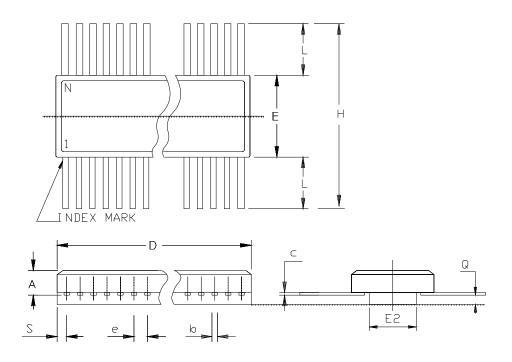
Ordering Information

Part Number	Temperature Range	Speed	Package	Flow
MMDJ-65609EV-40-E	25 °C	40 ns	FP32.4	Engineering Samples
5962-0250101QXC	-55 to +125 °C	40 ns	FP32.4	QML Q
5962-0250101VXC	-55 to +125 °C	40 ns	FP32.4	QML V
5962R0250101VXC	-55 to +125 °C	40 ns	FP32.4	QML V RHA
SMDJ-65609EV-40SCC	-55 to +125° C	40 ns	FP32.4	ESCC
MM0 -65609EV-40-E ⁽¹⁾	25 °C	40 ns	Die	Engineering Samples
MM0 -65609EV-40SV ⁽¹⁾	-55 to +125 °C	40 ns	Die	QML V

Note: 1. Contact Atmel for availability.

Package Drawing

32-pin Flat Pack (400 Mils)



	ММ		I NCH	
	Min	Max	Min	Max
A	1.78	2. 72	. 070	.107
b	0.38	0.48	. 015	. 019
С	0.076	0.18	. 003	.007
D	20.62	21.03	. 81 2	. 828
E	10.26	10.57	. 404	. 416
E5	6.96	7.26	. 274	. 286
e	1.27 BSC		.050 BSC	
L	7.00	8.50	. 276	. 335
н	25. 6	26. 2	1.008	1.031
Q	0.51	0.76	. 020	. 030
S		1.14		.045
N	32		32	





Document Revision History

Changes from Rev. I to Rev. J

Add-on: MBU's note in features section Update: radiation tolerance specification in features section Update: block diagram Update: AC test conditions section Update: package drawing



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