Rad. Hard 0.18 µm CMOS Cell-based ASIC for Space Use

ATC18RHA

Features

- **Comprehensive Library of Standard Logic and I/O Cells**
- **Up to 6.5 usable Mgates equivalent NAND2**
- **Operating voltage 1.8V for core and 3.3V or 2.5V for I/O's**
- **Memory Cells Compiled or synthesized to the Requirements of the Design**
- **EDAC Library**
- **Cold Sparing Buffers**
- **High Speed LVDS Buffers (655Mbps)**
- **PCI Buffers**
- **MQFP Package Up to 352 Pins (336 Signal Pins)**
- **MLGA Packages Up to 625 Pins (575 Signal Pins)**
- **ESD better than 2000V for I/O and better than 1000V for PLL**
- **Predefined Die Sizes to Accommodate Standardized Packages**
- **Space Multi Project Wafer - SMPW - possibility**
- **No single event latch-up below a LET threshold of 95 Mev/mg/cm² at 125°C**
- **SEU hardened flip-flops**
- **Tested up to a total dose of 300 krads (Si) according to Mil Std 883 Test Method 1019**
- **Quality Grades: QML-Q and QML-V with 5962-06B02, ESCC 9000**

Description

The ATC18RHA asic family provides high-performance and high-density solutions for space applications. ATC18RHA is fabricated on a 0.18 µm, five-metal-layers CMOS process intended for use with a supply voltage of 1.8V for core. It offers up to 6.5 million routable gates and more than 800 pads.

The ATC18RHA family is supported by a combination of state-of-art third-party and proprietary design tools: Synopsys, Mentor and Cadence are the reference front end and back end tools suppliers.

The ATC18RHA asic family is available in several quality assurance grades, such as Mil-Prf 38535 QML-Q and QML-V and ESCC 9000.

4261G–AERO–02/11

Overview

Introduction

The ASIC "ATC18RHA Design Manual" presents all the required information and flows for 0.18µm designs for aerospace applications, allowing users to view Atmel specific or standard commercial tool kits and methodological details for actual implementations.

This offering is a 0.18µm CMOS technology based, specified with the 3.3V or 2.5V range for the periphery (it should be noticed that mixed supply is not allowed), and with the 1.8V range for the core. The technology parameters and some extra features are described here after.

Periphery

Buffers Description

The peripheral buffer, so called pad, is the electrical interface between the external signals (voltage range from 2.3 to 3.6V) and the internal core signals (from 1.65 to 1.95V).

All I/O pads are **Cold Sparing** and **tolerant**, they contains:

- Bidirectional pads
- Tristate Output pads
- Output Only pads
- Input Only pads *(Inverting,Non-Inverting,Schmitt Trigger)*

Furthermore the Bidirectional, Tristate Ouputs and Input Only pads are available with or without Pull-Up or Pull-Down structures.

Specific pads have been developed in 3.3V and 2.5V:

- **LVDS** transmitter and Receiver differential pads

Cold sparing and tolerant only when they are disabled (ien='1' or oen='1')

- **LVPECL** Receiver differential pads

And, in 3.3V only:

- Cold sparing **PCI** Bidirectional, Tristate Output and Output Only pads

Clusters

The periphery of the chip (pad ring) can be split into several I/O segments *(I/O clusters), s*ome clusters can be unpowered while others are active.

A specific Power control line is distributed inside the cluster to be able to force all the I/Os of the cluster in tristate mode whatever their initial state is (ie: an output only buffer will also be turned to HiZ mode).

Double Pad Ring

In order to increase the number of programmable I/O's, Atmel proposes the double pad ring configuration. The number of pads on the inner ring will be tailored to the actual need of each design.

Core supplies are automatically routed to the inner ring. As long as the inner ring of the double pad ring configuration is used only for core supply pads, the designs are produceable to space quality levels. During feasibility study, an investigation will be conducted to evaluate if additional pads, and how many, can be added in the inner ring to be used as I/O's and still be produced in space quality level. Anyhow, the resulting total number of pads in the inner ring will not go above maximum number given in table 2.

Core

Standard cell library

The Atmel Standard Cell Library contains a comprehensive set of a combination of logic and storage cells, including cells that belong to the following categories:

- Buffers and Gates
- PLL
- Multiplexers
- Standard and SEU Hardened Flip-flops
- Standard and SEU Hardened Scan Flip-flops
- Latches
- Adders and Subtractors

Memory Hard Blocks

The ATC18RHA memory libraries are developed from Virage memory compilers. All these memories are synchronous.

It can compile single-port synchronous SRAM, dual port (2RW) synchronous SRAM and Two-port (1W,1R) synchronous Register-File.

For maximum block sizes, see the design manual.

Array Organization

Though ATC18RHA is a standard cell library, pre-defined matrix sizes and pad frames have been set so as to ease the assembly of every individual ASIC design by sticking to presently available package cavity sizes and layouts. These are close in size to MH1RT matrix sizes.

The following tables give, for each matrix, for a single or a double pad ring configuration, the maximum number of pads on the outer ring, the maximum number of pads implementable on the inner ring, and the resulting typical gate count capability of each matrix.

Table 1. Single Pad Ring Standard Arrays Dimensions and Integration Capabilities

Name	MH1RT Equivalence	Size (mm)	Pads	Usable Gates (typ)
ATC18RHA95_216	NA	6.19x6.19	216	1M
ATC18RHA95_324	MH1099E	8.76x8.76	324	2.2M
ATC18RHA95_404	MH1156E	10.66x10.66	404	3.5M
ATC18RHA95_504	MH1242E	13.03x13.03	504	5.5M
ATC18RHA95_544	NA	14.03x14.03	544	6.5M

Table 2. Double Pad Ring Standard Arrays Dimensions and Integration Capabilities

Name	Outer Ring Programmable Pads	Inner Ring Max Number of Pads	Size (mm)	Usable Gates (typ)
ATC18RHA95_216D	216	88	6.19x6.19	0.725M
ATC18RHA95_324D	324	140	8.76x8.76	1.8M
ATC18RHA95_404D	404	180	10.66x10.66	2.97M
ATC18RHA95_504D	504	232	13.03x13.03	4.83M
ATC18RHA95_544D	544	252	14.03x14.03	5.71M

Design Management

Introduction

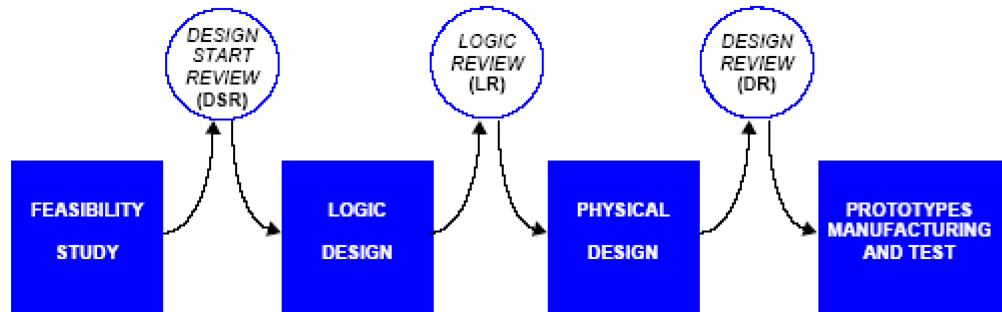
Atmel used to propose different design modes, where each mode indicated the designer responsibilities, the design location and the design tools. With designs becoming more complex, timing and power constraints more severe, and design behaviour more technology dependent, Atmel believes that any design must be a close cooperation between the customer and the manufacturer. Therefore, only one design scenario is retained: the ASIC chip is designed by the customer, at his site with a set of design tools supported by Atmel.

Design Phases

The development of an ASIC chip can be split into 4 main phases.

A meeting is set between each phase.

Figure 1. *Design Management Phases*



During the review meetings, the conformity of the design to Atmel rules is checked and acknowledged in formal documents, and the data is transferred to the next phase. The content of each phase and responsibilities are described in the 'ATC18RHA design manual'.

Deliverables

Table 3. Deliverables at the end of each phase

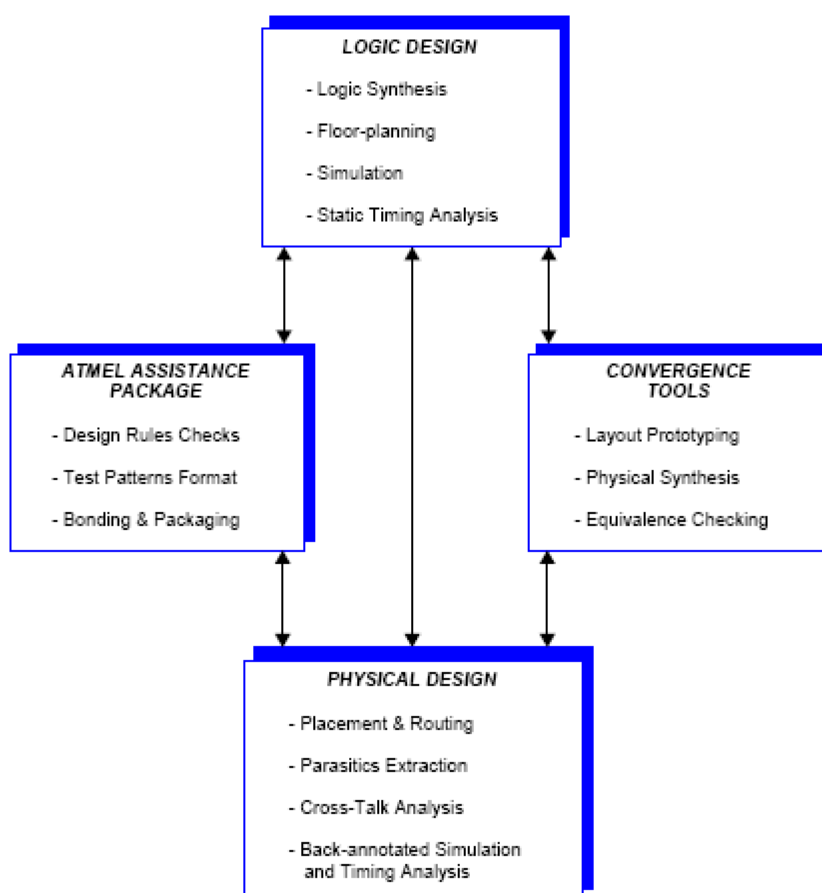
DESIGN PHASE	DELIVERABLE	WHO
FEASIBILITY STUDY	ASIC feasibility study report (APF-tc-FSR-project code). Design start review document (APF-tc-DSR-project code).	Atmel
LOGIC DESIGN	ASIC logic review document (APF-tc-LR-project code) + Files as required in the document.	CUSTOMER
	Updated DSR document	Atmel
PHYSICAL DESIGN	ASIC design review document (APF-tc-DR-project code) + Files as required in the document.	CUSTOMER
	Updated DSR document	Atmel
PROTOTYPES MANUFACTURING & TEST	Packaged parts and associated documents	Atmel

Design Flows

Introduction

This chapter summarizes the design flow with reference to different platforms used for Cell based chip design. For further details, refer to the ATC18RHA design manual.

Figure 2. Global design flow



Atmel Package Assistant is running on SUN stations under SOLARIS and on LINUX PC (Red-Hat distribution from version 7.0). Design Kits are compatible with both platforms depending on third party tools availability. Hardware platform memory requirement is design dependant.

Design Kit

The use of both external and internal ICCAD tools requires the modelization of each library element. The set of required files for all the supported CAD tools relevant to the ATC18RHA family is called the *ATC18RHA Design Kit*. These files describe the functionality, including or not timings and other attributes, with respect to each targeted tools modelization features and methods.

The design kit contains relevant descriptions of standard cells and peripheral cells, given for different pre-defined ranges of temperature, voltage and process.

Design flow

The Design flow can be described in two sections.

The front-end done at the customer's premises

The following table lists the activities and tools that will be used during the front-end design.Tools in bold are included in the 'ATC18RHA design kit'.

Table 4. Front-end tools

Function	Tool	Supplier
RTL simulation	MODELSIM	MENTOR
Code coverage	VHDL-COVER	TRANSEDA
HDL synthesis	DESIGN-COMPILER	SYNOPSYS
Physical synthesis	DC TOPO, ICC	SYNOPSYS
Power optimization	POWER-COMPILER	SYNOPSYS
Power analysis	PrimetimePX	SYNOPSYS
DFT tools	DFTC	SYNOPSYS
	DFT SUITE	MENTOR
Gate level simulation	MODELSIM	MENTOR
Design rules check	**STAR**	Atmel

The back-end at Atmel Technical Centers

Provided that the front-end activity has been validated and accepted by Atmel during the Logic Review (LR) meeting, the following table lists the activities and the tools that will be used during the back-end design

Table 5. Back-end tools

Activities	Function	Tool	Supplier
Bonding diagram	Array Definition	**Mgtechgen**	Atmel
	Bonding diagram	**Pimtool**	Atmel
	Pads pre-placement	**P2def**	Atmel
	Periphery check	**COP**	Atmel
	IBIS model	**Genibis**	Atmel
Physical implementation	Blocks Preplacement	**Silver**	Atmel
	Virtual Layout Prototyping	First Encounter	CADENCE
	Physical Knowledgeable Synthesis	FE OPT.	CADENCE
	Power routing	**Snow**	Atmel
	Placement	FE Place	CADENCE
	Scan chains ordering	FE Place	CADENCE
	Clock tree synthesis	FE CTS	CADENCE
	Routing	Nanoroute	CADENCE
	Final violation fix	FE OPT.	CADENCE
	Eco Place and route	FE	CADENCE
	Layout edition	**Silver**	Atmel
	3D extraction	Star-RCXT	SYNOPSYS
Final verifications	Static timing analysis	Prime time	SYNOPSYS
	Equivalence checking	Formality	SYNOPSYS
	Back-annotated simulation	Modelsim	MENTOR
		Nc-sim	CADENCE
	Consumption analysis	PrimetimePX	SYNOPSYS
	Power scheme check	Voltagestorm	CADENCE
	Cross talk analysis	Celtic	CADENCE
	Cross talk errors fix	Nanoroute	CADENCE
	Final analysis	Celtic-NDC	CADENCE
	Test patterns	**TVT**	Atmel
	GDSII generation	**SE2GDS**	Atmel

Space Multi Project Wafer

Atmel proposes a Multi Projects Wafer service, so called SMPW, in order to decrease the cost of reticules and silicon by sharing them over several designs. Specific milestones have been created to coordinate the activities and guarantee that there will be no interaction between customer designs.

Main milestones are the Logic Review Closing Date (LRCD) and the Design Review Closing Date (DRCD). The LR meeting must be held prior to LRCD and the DR meeting prior to DRCD. For each SMPW, those dates are known in advance.

Any questions related to SMPW service can be addressed to the hotline, at smpw-atc18@nto.atmel.com.

Advanced Packaging

The ATC18RHA Series are offered in ceramic packages: multi layers quad flat packs (MQFP) with up to 352 pins and a multi layer land grid array (MLGA) with up to 625 lands.

The following table provides the standard matrix / package combination in single and double ring configuration.

In addition, Atmel proposes custom packages development for specific requirements.

Table 6. Dice/Packages standardized combinations

	ATC18RHA95 _216	ATC18RHA95 _324	ATC18RHA95 _404	ATC18RHA95 _504	ATC18RHA95 _544
MQFPT352		X	X	X	
MQFPF256	X	X	X	X	
MQFPF196	X	X			
MQFPF160	X	X			
MQFPF100	X				
AIN MLGA625					X
MLGA625				X	X
MLGA472			X	X	
MLGA349		X	X	X	

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be

performed. Since a digital tester must control all the clocks during the testing of chip, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of the chip, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Radiation Hardness

ATC18RHA Asics are designed and processed to be Rad-Hard. The ATC18RHA standard cell library encompasses all the specific functions and buffers necessary for space designs, such as LVDS transmitters and receivers, PCI buffers, SEU hardened DFFs and cold sparing buffers. Key radiation-tolerance parameters are controlled and monitored.

Table 7. Radiation-Tolerance key parameters

Parameter	Radiation Hardness Assurance
TID (1,2) Total Ionizing Dose	100 krads(Si)
SEU(1, 3) Single Event Upset	$< 4.10^{-11}$ errors/bit-day
SEL (1, 4) Single Event Latch-up	LET > 95 MeV/mg/cm² at 125°C

Notes:

(1) Report available under request, after Non-Disclosure Agreement

(2) Co-60 testing, in compliance with Mil-Std 883 TM 1019.5: Tested at 25°C, with a total dose rate of 300 rad/h and a total dose of 300 krad(Si)

(3) Based on hardened DFF included in a SEC (Standard Evaluation Circuit), at 1.65V for core, 3V for I/O's and 25°C.

(4) In worst case: 1.95V for core, 3.6V for I/O's

Electrical Characteristics

Absolute Maximum Ratings

Core Supply Voltage VDD ....-0.3V to +2V Buffer Supply Voltage VCC...................................-0.3V to +4V Buffer Input Voltage.. -0.3V to +4V Storage Temperature.................................... -65°C to +150°C ESD for I/O..>2000V ESD for PLL ....>1000V	*NOTICE: This absolute maximum ratings voltage is the maximum voltage that guarantees that the device will not be burned if those maximum voltages are applied during a very limited period of time. This is not a guarantee of functionality or reliability. The users must be warned that if a voltage exceeding the maximum voltage (nominal +10%) and below this absolute maximum rating voltages, is applied to their devices, the reliability of their devices will be affected.

Recommended Operating Conditions

Core Supply Voltage VDD	1.65V to 1.95V
3.3V Buffer Supply Voltage VCC	3.0V to 3.6V
2.5V Buffer Supply Voltage VCC	2.3V to 2.7V
Buffer Input Voltage	0V to VCC
Storage Temperature	-65°C to +150°C

Consumption

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Ta	Operating Temperature	-55	25	125	°C	
VDD	Supply Voltage	1.65	1.8	1.95	V	core
ICCSBA	Leakage current per gate		0.145	5.5	nA	
ICCOPA	Dynamic current per gate			8.8	nA/MHz	Duty cycle = 20%

I/O DC at 3.3V Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD	Supply Voltage	1.65	1.8	1.95	V	core
VCC	Buffer Supply voltage	3.0	3.3	3.6	V	IOs
IIL	Low Level Input Current	-1		1	µA	Vin=Vss
	Pull-up resistor	110	220	400	µA	
	Pull-down resistor	-5		5	µA	
IIH	High Level Input Current	-1		1	µA	Vin=Vcc
	Pull-up resistor	-5		5	µA	
	Pull-down resistor	140	320	600	µA	
IOZ	High Impedance State Output Current	-1		1	µA	Vin=Vcc or Vss no pull resistor
VIL	Low-Level Input Voltage	-0.3		0.8	V	
VIH	High- Level Input Voltage	2		Vcc+0.3	V	
Vhyst	Hysteresis		400		mV	
IICS	Cold Sparing leakage input current	-1		1	µA	Vcc=Vss=0V Vin=0 to Vcc
IOCS	Cold Sparing leakage output current	-1		1	µA	Vcc=Vss=0V Vout=0 to Vcc
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA
VOL	Low level output voltage			0.4	V	IOL=2,4,8,12,16mA
VOH	High level output voltage	vcc-0.4			V	IOH=2,4,8,12,16mA
IOS (1)	Output Short circuit current IOSN (nn=1) IOSP (nn=1)			 23 23	 mA mA	 Vout=Vcc Vout=Vss

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 23,46,92,138,184 mA for nn=1,2,4 ,6,8

I/O DC at 2.5V Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD	Supply Voltage	1.65	1.8	1.95	V	core
VCC	Buffer Supply voltage	2.3	2.5	2.7	V	IOs
IIL	Low Level Input Current	-1		1	µA	Vin=Vss
	Pull-up resistor	60	130	260	µA	
	Pull-down resistor	-5		5	µA	
IIH	High Level Input Current	-1		1	µA	Vin=Vcc
	Pull-up resistor	-5		5	µA	
	Pull-down resistor	75	180	360	µA	
IOZ	High Impedance State Output Current	-1		1	µA	Vin=Vcc or Vss no pull resistor
VIL	Low-Level Input Voltage	-0.3		0.7	V	
VIH	High- Level Input Voltage	2		Vcc+0.3	V	
Vhyst	Hysteresis		350		mV	
IICS	Cold Sparing leakage input current	-1		1	µA	Vcc=Vss=0V Vin=0 to Vcc
IOCS	Cold Sparing leakage output current	-1		1	µA	Vcc=Vss=0V Vout=0 to Vcc
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA
VOL	Low level output voltage			0.4	V	IOL=1.5,3,6,9,12mA
VOH	High level output voltage	vcc-0.4			V	IOH=1.5,3,6,9,12mA
IOS (1)	Output Short circuit current IOSN (nn=1) IOSP (nn=1)			 14 14	 mA mA	 Vout=Vcc Vout=Vss

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 14,28,56,84,112 mA for nn=1,2,4 ,6,8

PCI Characteristics

DC specifications

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Tests conditions
VCC	Buffer Supply voltage	3.0	3.3	3.6	V	
VIH	High Input Level	0.5 Vcc		Vcc + 0.3	V	
VIL	Low Input Level	-0.3		0.3 Vcc	V	
IOH	High Level Current	16	32		mA	VOH=Vcc - 0.4V
IOL	Low Level Current	16	32		mA	VOL=0.4V
IOS (1)	Output Short Current		112	184	mA	VOH=0 VOL=Vcc
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

LVPECL Receiver characteristics

DC specifications

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Tests conditions
VCC	Buffer Supply voltage	3.0	3.3	3.6	V	
VCC	Buffer Supply voltage	2.3	2.5	2.7	V	
IIN	Input Leakage	-10		10	µA	
ICCstat	Static Consumption(ien=0)		2.5	4	mA	VCC=3.3+/-0.3V
ICCstdby	Static Consumption(ien=1)			10	µA	VCC=3.3+/-0.3V
ICCstat	Static Consumption(ien=0)		1.5	2.3	mA	VCC=2.5 +/- 0.25V
ICCstdby	Static Consumption(ien=1)			5.8	µA	VCC=2.5 +/- 0.25V

LVDS Reference characteristics

DC specifications

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	MIN	TYP	MAX	Unit	Tests conditions
VCC	Buffer Supply voltage	3.0	3.3	3.6	V	
VCC	Buffer Supply voltage	2.3	2.5	2.7	V	
Vref	Input Voltage	1.25 - 5%	1.25	1.25 + 5%	V	
Rpd	Pull Down resistance	140	200	260	kOhm	VIN=1.25V
ICCstat	Static Consumption (ien=”0”)		260	320	µA	VCC=3.3+/-0.3V
ICCsdby	Static Consumption (ien=”1”)			2	µA	VCC=3.3+/-0.3V
ICCstat	Static Consumption (ien=”0”)		150	184	µA	VCC=2.5 +/- 0.25V
ICCsdby	Static Consumption (ien=”1”)			1.2	µA	VCC=2.5 +/- 0.25V

LVDS Transmitter characteristics

DC specifications

Applicable over recommended operating temperature and voltage range unless otherwise noted.

<table>
<tr><th>Symbol</th><th>Parameter</th><th>MIN</th><th>TYP</th><th>MAX</th><th>Unit</th><th>Tests conditions</th></tr>
<tr><td>VCC</td><td>Buffer Supply voltage</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td><td></td></tr>
<tr><td>VCC</td><td>Buffer Supply voltage</td><td>2.3</td><td>2.5</td><td>2.7</td><td>V</td><td></td></tr>
<tr><td>|VOD|</td><td>Output Differential Voltage</td><td>247</td><td>350</td><td>454</td><td>mV</td><td>Rload = 100 ohms</td></tr>
<tr><td>VOS</td><td>Output offset Voltage</td><td>1.125</td><td>1.25</td><td>1.375</td><td>V</td><td>Rload = 100 ohms</td></tr>
<tr><td>|ΔVOD| (1)</td><td>Change in |VOD|</td><td></td><td></td><td>50</td><td>mV</td><td>Rload = 100 ohms</td></tr>
<tr><td rowspan="2">|ΔVOS| (1)</td><td>Change in VOS - steady state</td><td rowspan="2"></td><td rowspan="2"></td><td>50</td><td rowspan="2">mV</td><td rowspan="2">Rload = 100 ohms</td></tr>
<tr><td>Change in VOS - dynamic state</td><td>150</td></tr>
<tr><td rowspan="2">IOS</td><td rowspan="2">Output short current</td><td></td><td>7</td><td>24</td><td>mA</td><td>Drivers shorten to ground or VCC</td></tr>
<tr><td></td><td>4.5</td><td>12</td><td>mA</td><td>Drivers shorten together</td></tr>
<tr><td>ICCstat</td><td>Static Consumption (ien=”0”)</td><td></td><td>4</td><td>6</td><td>mA</td><td>VCC=3.3+/-0.3V</td></tr>
<tr><td>ICCsdby</td><td>Static Consumption (ien=”1”)</td><td></td><td></td><td>10</td><td>µA</td><td>VCC=3.3+/-0.3V</td></tr>
<tr><td>ICCstat</td><td>Static Consumption (ien=”0”)</td><td></td><td>2.3</td><td>3.5</td><td>mA</td><td>VCC=2.5 +/- 0.25V</td></tr>
<tr><td>ICCsdby</td><td>Static Consumption (ien=”1”)</td><td></td><td></td><td>5.8</td><td>µA</td><td>VCC=2.5 +/- 0.25V</td></tr>
</table>

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

LVDS Receiver characteristics

DC specifications

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	MIN	TYP	MAX	Unit	Tests conditions
VCC	Buffer Supply voltage	3.0	3.3	3.6	V	
VCC	Buffer Supply voltage	2.3	2.5	2.7	V	
VID	Input Differential Voltage	200		600	mV	
VCM	Common Mode Input Voltage	0.05		2.35	V	
IIN	Input Leakage	-10		10	µA	
ICCstat	Static Consumption (ien=”0”)		3.5	6	mA	VCC=3.3+/-0.3V
ICCsdby	Static Consumption (ien=”1”)			10	µA	VCC=3.3+/-0.3V
ICCstat	Static Consumption (ien=”0”)		2	3.5	mA	VCC=2.5 +/- 0.25V
ICCsdby	Static Consumption (ien=”1”)			5.8	µA	VCC=2.5 +/- 0.25V

Document Revision History

Changes from Rev. 4261B-06/05 to 4261C-04/06

1. Added double pad ring configuration
2. Clarification of paragraphs concerning ESD and array organization
3. Tools update (moved from Hyperextract to Star-RCXT)

Changes from Rev. 4261C-04/06 to 4261D-07/07

1. Remove 1.8V I/O offering

Changes from Rev. 4261D-07/07 to 4261E-10/07

1. Added I/O33 supplied at 2.5V offering and LVDS/LVPECL 2.5V

Changes from Rev. 4261E-10/07 to 4261F-08/08

1. Added note to MCGA625 product offering

Changes from Rev. 4261F-08/08 to 4261G-02/11

1. Removed informations already included in the ‘ATC18RHA design manual’
2. Added MLGA packages up to 625 lands - removed MCGA packages
3. Added ATC18RHA95_544 die
4. Added a note on dual voltage on periphery - page 2
5. Corrections on LVDS data
6. Typo: For core, supply is Vdd and for buffers is Vcc
7. Add radiation tolerance paragraph

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