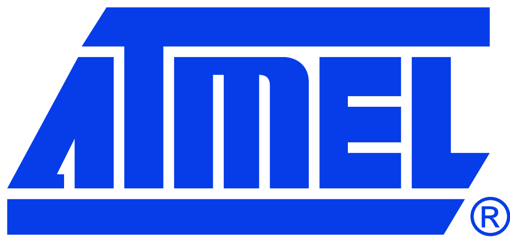

PS-AT17LV010

revision A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 1 MEGABIT SERIAL EEPROM, MONOLITHIC SILICON

Revision	Written by	Approved by	Date
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Date of update	Revision letter	modifications

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1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data of the 1 megabit serial EEPROM named AT17LV010. It also defines the specific requirement for space and military applications with high reliability.

1.2 Identification

Part number	Description	Access Time	Case	Application
AT17LV010-10DP-MQ	1 megabit serial eeprom	60ns	Flat pack 400 mils 28 leads	Military application
AT17LV010-10DP-SV	1 megabit serial eeprom	60ns	Flat pack 400 mils 28 leads	Space application

1.3 Absolute maximum ratings

Supply voltage range (V_{DD}) .... -0.5V to 7V
Output voltage range (V_{OUT})... -0.1V dc to V_{DD} + 0.5V dc
Power dissipation (Pd) 0,1W
Storage temperature .... -65°C to 150°C
Maximum junction temperature (T_J) .... 175°C
Thermal resistance junction to case (Θjc) :........................ 9°C/W
Lead temperature (soldering @ 1/16 in, 10 s) .... 260°C
Endurance.. 50,000 write cycles
Data retention .... 10 years

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) .... 3 V dc to 3.6 V dc
Ambient operating temperature (T_A) .... -55°C to 125°C
Storage temperature .... 30°C, 20 to 65% RH, dust free, original packing

1.5 Radiation features

Tested up to a Total Dose of (according to MIL STD 883 Method 1019) :

(dose rate 0.1 rad/s).. 20 kRads (Si) Read Only Mode, when biased
.... 60 kRads (Si) Read Only Mode, when un-biased

No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm^2

1.6 Handling precautions

These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, shipment and any handling.
ESD (Rzap = 1.5 kΩ, Czap = 100 pF) .... 2000 V (class 3)

2 APPLICABLE DOCUMENTS

MIL-PRF-38535 ....Integrated Circuits, Manufacturing, General Specification for.
MIL-STD-883 ....Test Method Standard Microcircuits.
ASTM Standard F1192-95 ....Standard guide for the measurement of single event phenomena from heavy ion irradiation of semiconductor devices
JEDEC Standard EIA/JESD78..................IC latch-up test
ATMEL Aerospace Products Quality Flows

In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

3 REQUIREMENTS

3.1 Design, construction, and physical dimensions.

The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.1.1 Package type.

The package shall be a flat pack 400 mils, 28 leads (figure1). The case shall be hermetically sealed and have a ceramic body. The leads shall be brazed.

3.1.2 Terminal connections.

The terminal connections shall be as specified on figure 2 .

3.1.3 Block diagram.

The block diagram shall be as specified on figure 3 .

3.1.4 Timing waveforms.

The timing waveforms shall be as specified on figure 4.

3.2 Marking

Each component shall be marked in respect of :
(a) Lead Identification
(b) Component Number
(c) Traceability Information
(d) Manufacturer's Component Number

3.2.1 Lead Identification

An index shall be located at the top of the package in the position defined in Figure 1.

3.2.2 Component Number

Each component shall bear the component number which shall be constituted and marked as follows :

3.2.3 Traceability Information

Each component shall be marked in respect of traceability information : lot number and date code.

3.3 Electrical characteristics

The parameters to be measured with respect of electrical characteristics are scheduled in Table 1. The measurements shall be performed at T_{amb}=22 ± 3°C, T_{high}=125 (+0/-5)°C and T_{low} = -55 (+5/-0)°C respectively.

3.4 Burn-in test

3.4.1 Electrical circuit

Circuit for use in performing the power burn-in is shown in figure 5, in accordance with the intent specified in test method 1015 of MIL-STD-883.

3.4.2 Parameters drift value

For space application, the parameter drift values applicable to burn-in are specified in Table 2 of this specification. Unless otherwise stated, measurements shall be performed at + 22 ± 3 ° C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded.

In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 1 shall not be exceeded.

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3.5 Environmental and Endurance Tests

3.5.1 Electrical Circuit for Operating LifeTest

The circuit for operating life testing shall be as specified for power burn in (figure 5).

3.5.2 Electrical Measurements at Completion of Environmental and endurance tests

The parameters to be measured are scheduled in Table 1. Unless otherwise stated, the measurements shall be performed at t_{amb} = 22±3°C.

3.5.3 Conditions for Operating LifeTest

The conditions for operating life testing shall be as specified for power burn in.

3.6 Total dose irradiation testing

3.6.1 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

3.6.2 Electrical Measurements

The parameters to be measured prior to, during and on completion of irradiation texture are scheduled in Table 1 of this specification.

4 QUALITY ASSURANCE PROVISIONS

4.1 Wafer lot acceptance test

Compliant with ATMEL Quality Management System.

For space application, Wafer Lot is accepted by a SEM performed according to PAQC0016 (PAQC0016 referred to MIL-Std-883 method 2018 and 21400 ESCC specification).

4.2 Sampling and inspection.

Sampling and inspection procedures shall be in accordance with MIL-PRF-38535.

4.3 Screening.

Screening equivalent to MIL-PRF-38535. Screening shall be conducted on all devices prior to qualification and technology conformance inspection

- The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in accordance with MIL-PRF-38535.
- Additional screening for space application devices shall be as specified in MIL-PRF-38535, appendix B.

4.4 Quality conformance inspection

Qualification inspection for high reliability and space applications devices shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections.

4.4.1 Group A inspection.

- Tests shall be as specified in table 1 herein.
- Subgroups 7 and 8 of table I of method 5005 of MIL STD 883 shall include verifying the functionality of the device.
- O/V (latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device.
- Capacitance measurement shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failure, and all input and output terminals tested.

4.4.2 Group C inspection.

The group C inspection end-point electrical parameters shall be as specified in table 1 herein.

4.4.3 Group D inspection.

The group D inspection end-point electrical parameters shall be as specified in table 1 herein.

4.5 Delta measurements

Delta measurements, as specified in table 2, shall be made and recorded before and after the required burn-in screens to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table 2. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7 and 9.

5 PACKAGING

5.1 Packaging requirements

The requirements for packaging shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test method Mil-Std-883	Conditions $-55°C \leq T_C \leq +125°C$ $+3\ V \leq V_{DD} \leq +3.6\ V$ unless otherwise specified	Limits		Unit	Note
				Min	Max		
High level input voltage	V_{IH}	3013	V_{DD} = 3.6 V	**2**		V	4
Low level input voltage	V_{IL}	3013	V_{DD} = 3.0 V		**0.8**	V	4
High level output voltage	V_{OH}	3007	V_{DD} =3 V, I_{OH} = -2 mA V_{SS} =0V	**2.4**		V	3
Low level output voltage	V_{OL}	3007	V_{DD} =3 V, I_{OL} = 3 mA V_{SS} =0V		**0.4**	V	3
Low level Input current	I_{IL}	3009	V_{IN} =0 V_{DD} = 3.6V V_{SS} =0V	**-10**		µA	3
High level Input current	I_{IH}	3009	V_{IN} =V_{DD} = 3.6V V_{SS} =0V		**10**	µA	3
Supply current Active mode	I_{CCA}	3005	V_{DD} = 3.6V V_{SS} =0V		**5**	mA	3
Supply current Standby mode	I_{CCS}	3005	V_{DD} = 3.6V V_{SS} =0V		**150**	µA	3
Input capacitance	C_{IN}	3012	V_{IN} = 0 V V_{SS} =0V T_C = 25°C f_{IN} = 1.0 MHz		**12**	pF	5
Output capacitance	C_{OUT}	3012	V_{OUT} = 0 V V_{SS} =0V T_C = 25°C f_{IN} = 1.0 MHz		**12**	pF	5
Maximum clock frequency	F_{MAX}				10	MHz	
$\overline{CE}$ setup time to CLK (to guarantee proper counting)	T_{SCE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	35		ns	3
$\overline{CE}$ hold time to CLK (to guarantee proper counting)	T_{HCE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	0		ns	3
CLK low time	T_{LC}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	25		ns	4
CLH high time	T_{HC}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	25		ns	4
OE high time (to guarantee counter is reset)	T_{HOE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	25		ns	4
OE to data delay (1)	T_{OE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		55	ns	3
CLK to data delay (1)	T_{CAC}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		60	ns	3
Data hold from $\overline{CE}$, OE or CLK	T_{OH}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}	0		ns	3, 6
$\overline{CE}$ or OE to data float delay (2)	T_{DF}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		50	ns	4
$\overline{CE}$ to data delay (1)	T_{CE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		60	ns	3

CLK to data float delay when cascading (2)	T_{CDF}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		50	ns	4
CLK to $\overline{CEO}$ delay when cascading (1)	T_{OCK}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		55	ns	3
$\overline{CE}$ to $\overline{CEO}$ delay when cascading (1)	T_{OCE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		40	ns	3
$\overline{RESET}$ /OE to $\overline{CEO}$ delay when cascading (1)	T_{OOE}	3003	V_{DD} = 3 V &V_{DD} = 3.6 V, F_{MAX}		40	ns	3

Notes :

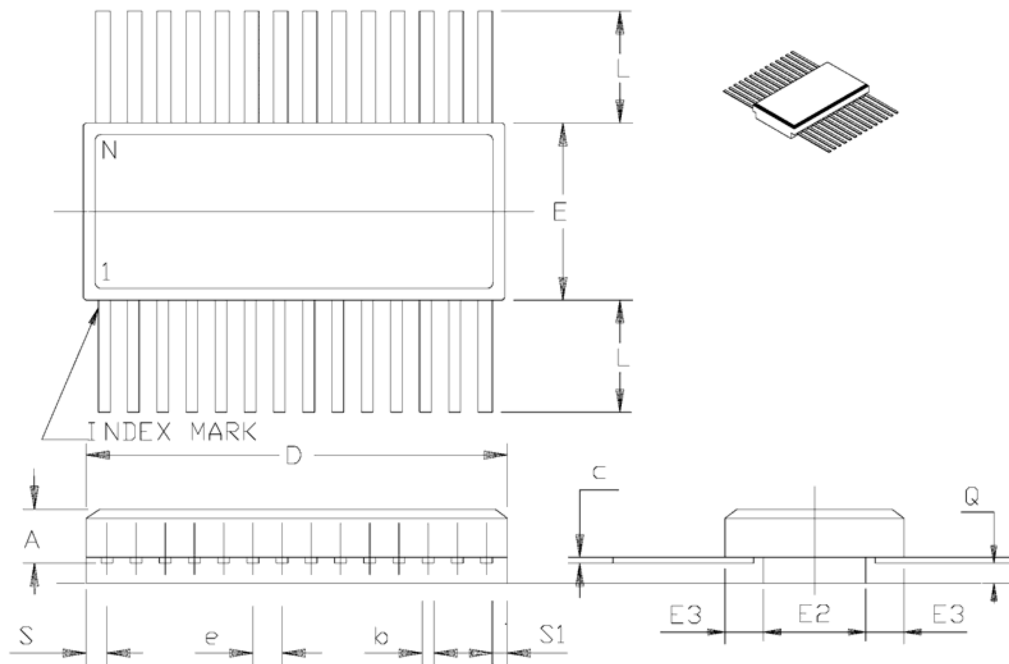
(1) Output load gate equivalent +C_L <30 pF
(2) Float delays are measured with 5 pF AC loads. Transition is measured +/- 200 mV from steady-state active levels
(3) Recorded
(4) Go-no-go tested
(5) This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in Table I
(6) All the cases are tested, but only one is recorded (worst case) if required (note 3)

TABLE 2. Parameter drift values

Test	Sym bol	Test method Mil-Std-883	Conditions	Drift limits	Unit
High level output voltage	V_{OH}	As per table 2	As per table 2	**0.1**	V
Low level output voltage	V_{OL}	As per table 2	As per table 2	**0.1**	V
Low level Input current	I_{IL}	As per table 2	As per table 2	**0.5**	µA
High level Input current	I_{IH}	As per table 2	As per table 2	**0.5**	µA
Supply current Standby mode	I_{CCS}	As per table 2	As per table 2	**15**	µA

Note : the above parameter shall be recorded before and after burn-in and life test to determine the delta.

FIGURE 1. Case outline



	mm		inch	
	Min	**Max**	**Min**	**Max**
A	2.29	3.30	0.090	0.130
b	0.38	0.48	0.015	0.019
c	0.08	0.15	0.003	0.006
D	---	18.80	---	0.740
E	9.65	10.67	0.380	0.420
E2	4.57	---	0.180	---
E3	0.76	---	0.030	---
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.66	---	0.026	---
S	---	1.30	---	0.051
S1	0.00	---	0.000	---
N	28			

FIGURE 2. Terminal connections.

Case outline	X
Pin Number	Name
1	$\overline{RESET}$ /OE
2	NC
3	WP2
4	$\overline{CE}$
5	GND
6	NC
7	NC
8	NC
9	NC
10	NC
11	$\overline{CEO}$
12	NC
13	NC
14	READY
15	NC
16	NC
17	$\overline{SER_EN}$
18	NC
19	VCC
20	NC
21	NC
22	NC
23	NC
24	DATA
25	CLK
26	WP1
27	NC
28	NC*

Note : * indicates this pin must not be used

Name	**Description**
$\overline{RESET}$ /OE	Output enable (active high) and reset (active low) when $\overline{SER_EN}$ is high. The logic polarity of this input is programmable
WP1,WP2	Used to protect portions of memory during programming
$\overline{CE}$	Chip enable input
$\overline{CEO}$	Chip enable output
READY	Open collector reset state indicator
$\overline{SER_EN}$	Serial enable
DATA	Tri-state data for configuration
CLK	Clock input
VCC	Power
GND	Ground

FIGURE 3. Block diagram

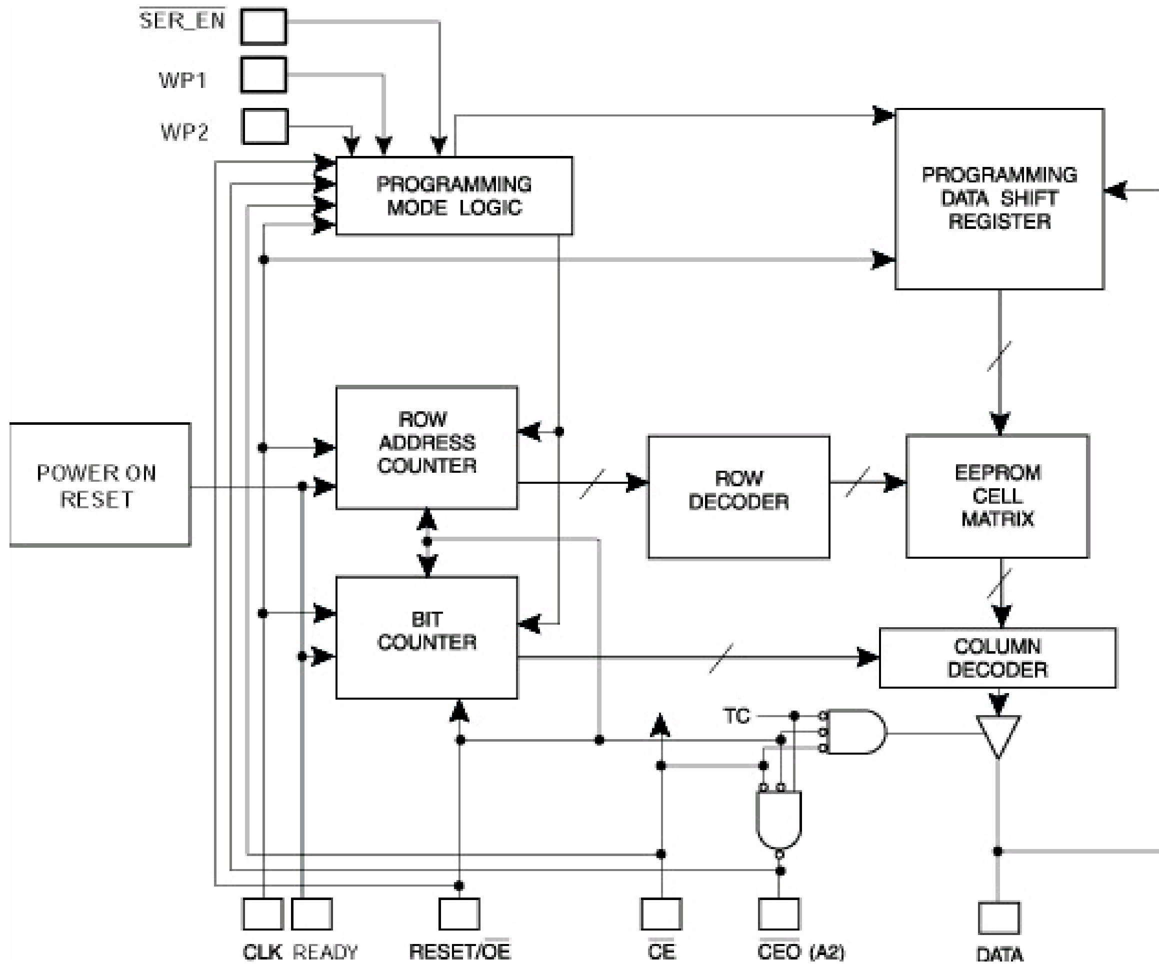
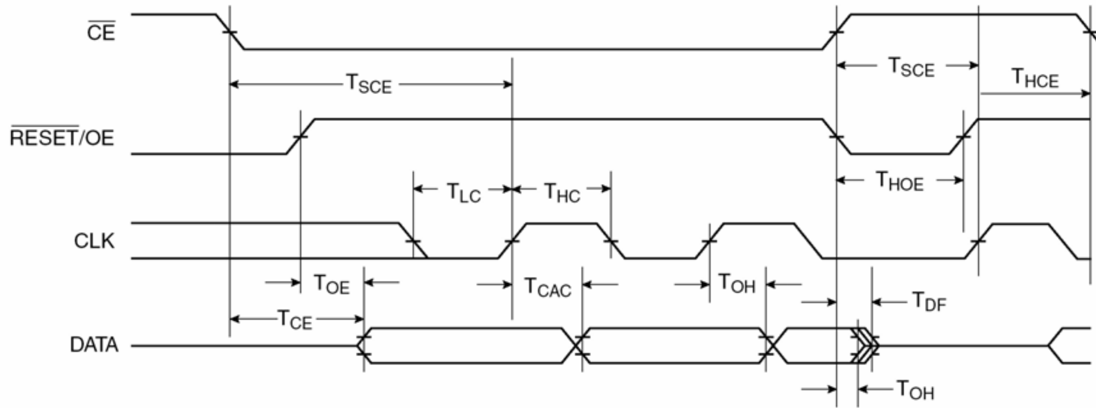


FIGURE 4. Timing waveforms.

4(a). AC characteristics



4(b). AC characteristics when cascading

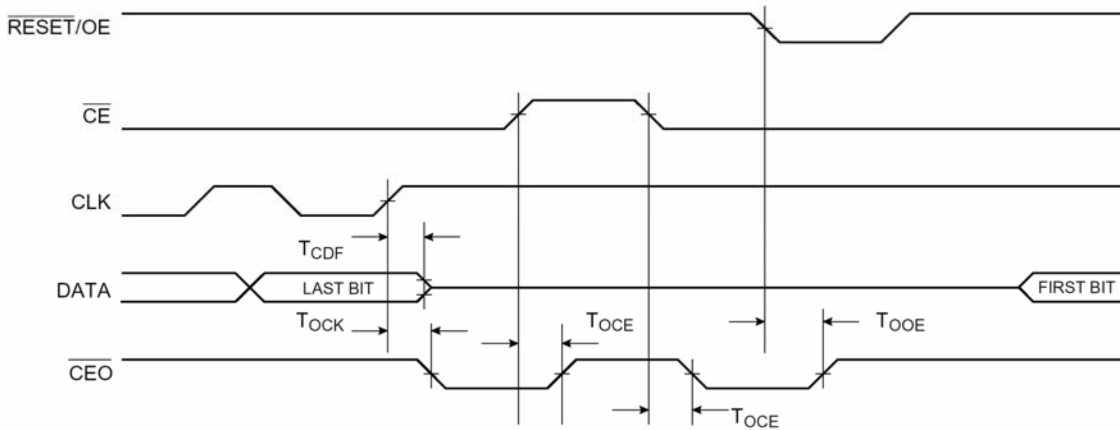
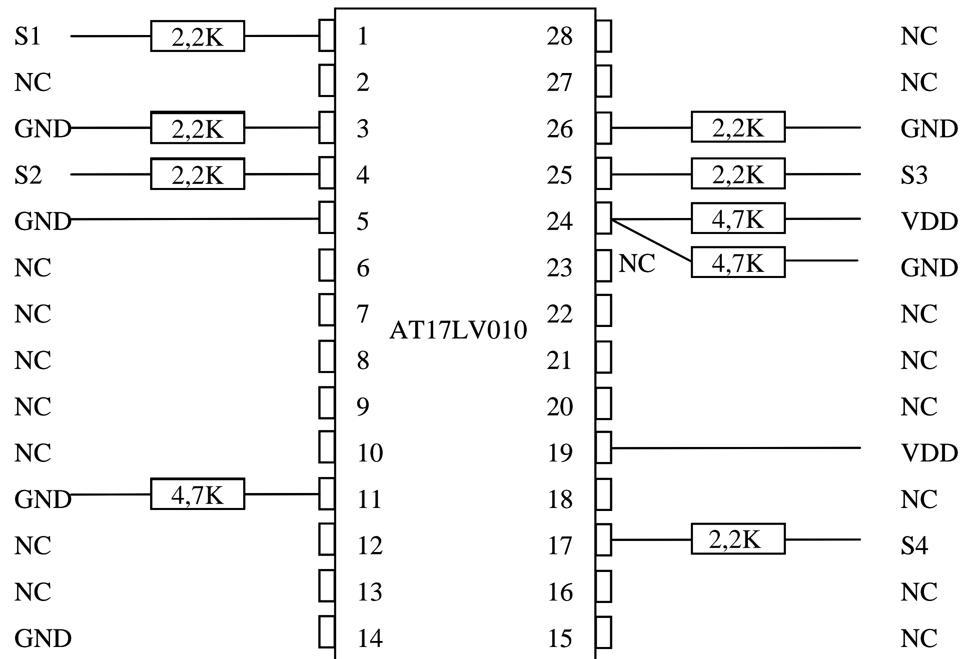
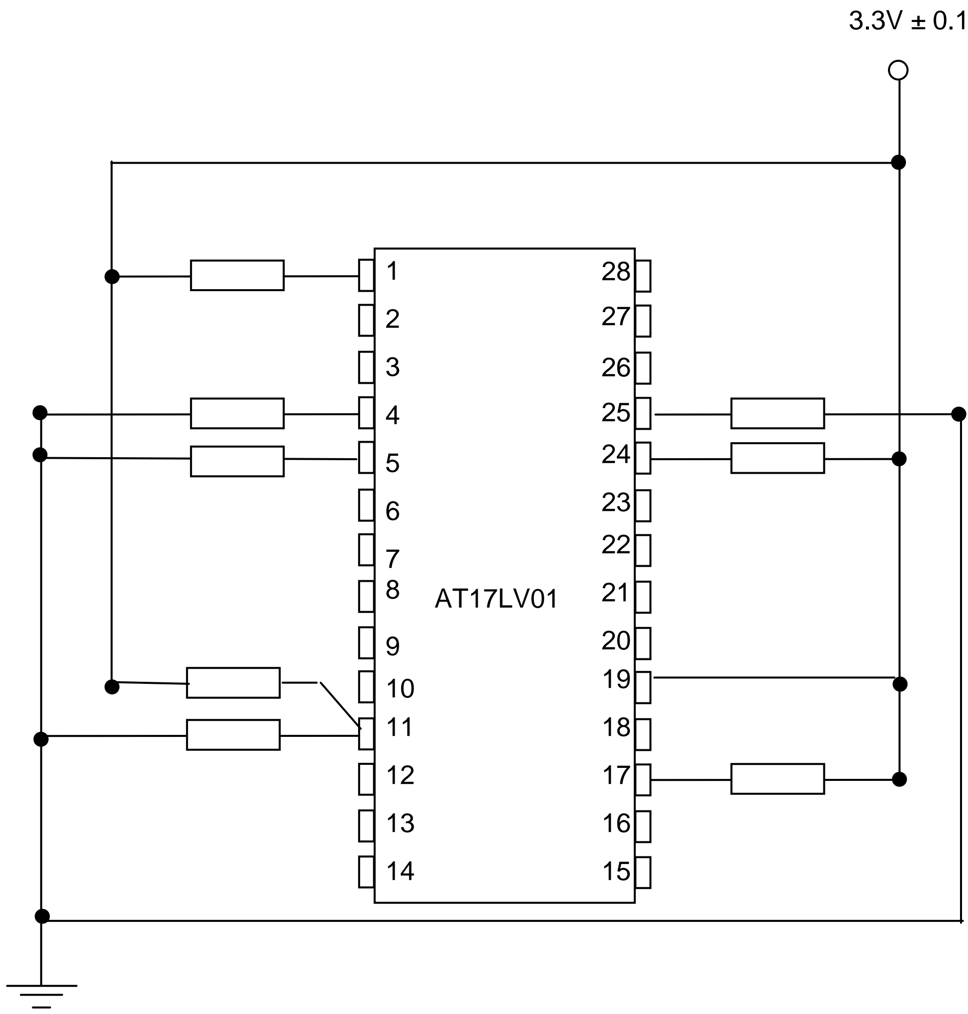


FIGURE 5. Electrical circuit for power burn-in and operating life test.



Notes :
S1 to S4 are signals which enable to read continuously the Eeprom 1 Meg memory plan according to the Figure 4a.

FIGURE 6. Electrical circuit for total dose radiation test.



Input protection resistors = 5,6 kohm +/- 10%