REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add appendix A for die devices 03, 04, 05. - tmh	00-07-03	Monica L. Poelking
B	Add case outline 8. Update boileplate. - phn	02-02-12	Thomas M. Hess
C	Add footnote in 1.2.2. Add RHA features in 1.6 and RHA requirements throughout- phn	03-10-27	Thomas M. Hess
D	Correct dimensions for case outline Y. Update boilerplate in according with MIL-PRF-38535 requirement. phn	07-03-06	Thomas M. Hess
E	Correct supply voltage range from -0.5 V to 7.0 V in 1.3. - phn	08-03-17	Thomas M. Hess

REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D		
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52		
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	E	C	E	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY

Thomas M. Hess

DEFENSE SUPPLY CENTER COLUMBUS
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Thomas M. Hess

APPROVED BY

Monica L. Poelking

DRAWING APPROVAL DATE

00-04-04

MICROCIRCUIT, DIGITAL, CMOS, MG2RTP, GATE ARRAY, MONOLITHIC SILICON

REVISION LEVEL

E

SIZE	CAGE CODE	
A	**67268**	**5962-00B03**

SHEET 1 OF 52

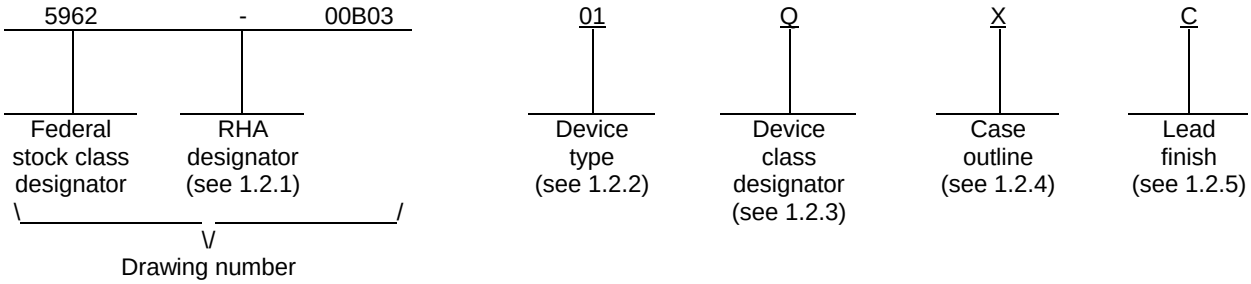
DSCC FORM 2233
APR 97

5962-E300-08

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	MG2RTPL_M01	202 gates available 1/
02	MG2RTPL_MB02	2,799 gates available 1/
03	MG2044P	44,000 gates available
04	MG2142P	142,000 gates available
05	MG2270P	270,000 gates available

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ This device is no longer available.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	40	Ceramic dip side braze
Y	See Figure 1	84	Flatpack unformed leads
Z	See Figure 1	68	Flatpack unformed leads
U	See Figure 1	80	Flatpack gull wing leads
T	See Figure 1	84	Flatpack unformed leads
M	See Figure 1	100	Flatpack gull wing leads 2/
N	See Figure 1	132	Flatpack gull wing leads
4	See Figure 1	160	Flatpack gull wing leads
5	See Figure 1	196	Flatpack gull wing leads 2/
6	See Figure 1	256	Flatpack unformed leads
7	See Figure 1	352	Quad flatpack with non-conductive tie bar
8	See Figure 1	44	Quad chip carrier with J lead

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings 3/ 4/

Supply voltage range (V_{DD}) ..... -0.5 V to 7.0 V
Input voltage range (V_{IN}) ..... -0.5 V to V_{DD} + 0.5 V 5/
Input current (I_{IN})
  Signal pin ..... -10 mA to 10 mA
  Power pin ..... -50 mA to 50 mA
Output short circuit current 6/
  $V_{OUT} = V_{DD}$ ..... 48 mA
  $V_{OUT} = V_{SS}$ ..... -36 mA
Lead temperature (soldering, 10 sec) ..... 300°C 7/
Storage temperature ..... -65°C to 150°C
Maximum junction temperature (T_J) ..... 175°C

1.4 Recommended operating conditions.

Supply voltage range ..... 2.7 V to 5.5 V 8/
Ambient operating temperature (T_A) ..... -55°C to 125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
  logic tests (MIL-STD-883, test method 5012) ..... As specified in the AID

1.6 Radiation features.

Maximum total dose available (dose rate = 0.1 rad(Si)/s) ..... 100 Krads 9/

———

2/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the Altered Item Drawing. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ All voltages referenced to Ground unless otherwise specified.
5/ V_{DD} + 0.5 V shall not exceed 7.0 V.
6/ The maximum output current of any single output in short condition for a maximum duration of 1 second.
7/ Duration 10 s max at a distance not less than 1.6 mm.
8/ This gate array device is capable of being configured with V_{DD} = 3.0 V ±10% or V_{DD} = 5.0 V ±10%.
9/ Unless otherwise specified in the AID.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent VHDL behavioral description).

3.3.4 Functional description terms and symbols.

3.3.5 Logic diagram (or equivalent structural VHDL description or mutually agreed to net list).

3.3.6 Pin function description.

3.3.7 Design tape # or Design document name (i.e., net list).

3.3.8 Design functional tape # or name.

3.3.9 Test functional tape # or name.

3.3.10 Timing diagram(s).

3.3.11 Fault coverage measurement of manufacturing logic tests.

3.3.12 Burn-in circuit.

3.3.13 Radiation exposure circuit.

3.3.14 ESD class and voltage.

3.3.15 Device electrical performance characteristics (additions to Table I). Device electrical performance characteristics shall include dc parametric, functional, ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.16 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.17 RHA post-irradiated electrical. For RHA devices supplied to this drawing, the RHA post irradiated electrical shall be specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage to GND 1/	V_{IC}	I_{OH} = -300 µA	1, 2, 3	All	- 1.2	-0.2	V
Low level input current 2/	I_{IL}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	All	- 5	-	µA
Low level input current, Pull-up 2/	I_{ILPU}	V_{IN} = GND, V_{DD} = 5.5V	1, 2, 3	All	- 100	-	µA
Low level input current, Pull-down 2/	I_{LLPD}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	All	- 5	-	µA
High level input current 2/	I_{IH}	$V_{IN} = V_{DD}$ = 5.5 V	1, 2, 3	All	-	5	µA
High level input current, Pull-up 2/	I_{IHPU}	$V_{IN} = V_{DD}$ = 5.5 V	1, 2, 3	All	-	5	µA
High level input current, Pull-down 2/	I_{IHPD}	$V_{IN} = V_{DD}$ = 5.5 V	1, 2, 3	All	-	300	µA
Output leakage low current 2/	I_{OZL}	Outputs disabled, V_{OUT} = GND	1, 2, 3	All	- 5	-	µA
Output leakage high current Pull-down output 2/	I_{OZHPD}	Outputs disabled, $V_{OUT} = V_{DD}$	1, 2, 3	All	-	300	µA
Output leakage low current Pull-up output 2/	I_{OZLPU}	Outputs disabled, V_{OUT} = GND	1, 2, 3	All	- 100	-	µA
Output leakage high current 2/	I_{OZH}	Outputs disabled, $V_{OUT} = V_{DD}$	1, 2, 3	All	-	5	µA
Low Level Input Voltage 1/	V_{IL}	Functional verification	1, 2, 3	All	-	0.8	V
Low level output voltage BOUT12 2/	V_{OL1}	V_{DD} = 5.5 V, I_{OL} = +12 mA	1, 2, 3	All	-	0.4	V
Low level output voltage BOUT6 2/	V_{OL2}	V_{DD} = 5.5 V, I_{OL} = +6 mA	1, 2, 3	All	-	0.4	V
Low level output Voltage BOUT3 2/	V_{OL3}	V_{DD} = 5.5 V, I_{OL} = +3 mA	1, 2, 3	All	-	0.4	V
High Level Output Voltage BOUT12 2/	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -12 mA	1, 2, 3	All	3.9	-	V
High level output voltage BOUT6 2/	V_{OH2}	V_{DD} = 4.5 V, I_{OH} = -6 mA	1, 2, 3	All	3.9	-	V
High level output voltage BOUT3 2/	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -3 mA	1, 2, 3	All	3.9	-	V
High level input voltage 1/	V_{IH}	Functional verification	1, 2, 3	All	2.2	-	V
Input capacitance 3/	C_I	V_{DD} = 0 V	4	All		15	pF
Output capacitance 3/	C_{IO}	V_{DD} = 0 V	4	All		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics. – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $2.7\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage to GND 1/	V_{IC}	I_{OH} = -300 µA	1, 2, 3	All	1.2	-0.2	V
Low level input current 2/	I_{IL}	V_{IN} = GND, V_{DD} = 3.6 V	1, 2, 3	All	- 1	-	µA
Low level input current, Pull-up 2/	I_{ILPU}	V_{IN} = GND, V_{DD} = 3.6V	1, 2, 3	All	- 50	-	µA
Low level input current, Pull-down 2/	I_{LLPD}	V_{IN} = GND, V_{DD} = 3.6 V	1, 2, 3	All	- 1	-	µA
High level input current 2/	I_{IH}	$V_{IN} = V_{DD}$ = 3.6 V	1, 2, 3	All	-	1	µA
High level input current, Pull-up 2/	I_{IHPU}	$V_{IN} = V_{DD}$ = 3.6 V	1, 2, 3	All		1	µA
High level input current, Pull-down 2/	I_{IHPD}	$V_{IN} = V_{DD}$ = 3.6 V	1, 2, 3	All	-	140	µA
Output leakage low current 2/	I_{OZL}	Outputs disabled, V_{OUT} = GND	1, 2, 3	All	- 1	-	µA
Output leakage high current Pull-down output 2/	I_{OZHPD}	Outputs disabled, $V_{OUT} = V_{DD}$	1, 2, 3	All	-	140	µA
Output leakage low current Pull-up output 2/	I_{OZLPU}	Outputs disabled, V_{OUT} = GND	1, 2, 3	All	- 50	-	µA
Output leakage high current 2/	I_{OZH}	Outputs disabled, $V_{OUT} = V_{DD}$	1, 2, 3	All	-	1	µA
Low level input voltage LVTTL input 1/	V_{IL}	Functional verification	1, 2, 3	All	-	0.8	V
Low level output voltage BOUT12 2/	V_{OL1}	V_{DD} = 3.6 V I_{OL} = +6 mA	1, 2, 3	All	-	0.4	V
Low level output voltage BOUT6 2/	V_{OL2}	V_{DD} = 3.6 V, I_{OL} = +3 mA	1, 2, 3	All	-	0.4	V
Low level output voltage BOUT3 2/	V_{OL3}	V_{DD} = 3.6 V, I_{OL} = +1.5 mA	1, 2, 3	All	-	0.4	V
High level output voltage BOUT12 2/	V_{OH1}	V_{DD} = 2.7 V, I_{OH} = -4 mA	1, 2, 3	All	$0.7V_{DD}$	-	V
High level output voltage BOUT6 3/	V_{OH2}	V_{DD} = 2.7 V, I_{OH} = -2 mA	1, 2, 3	All	$0.7V_{DD}$	-	V
High level output voltage BOUT3 3/	V_{OH3}	V_{DD} = 2.7 V, I_{OH} = -1 mA	1, 2, 3	All	$0.7V_{DD}$	-	V
High level input voltage LVTTL input 1/	V_{IH}	Functional verification	1, 2, 3	All	2.0	-	V
Input capacitance 3/	C_I	V_{DD} = 0 V	4	All		15	pF
Output capacitance 3/	C_{IO}	V_{DD} = 0 V	4	All		15	pF

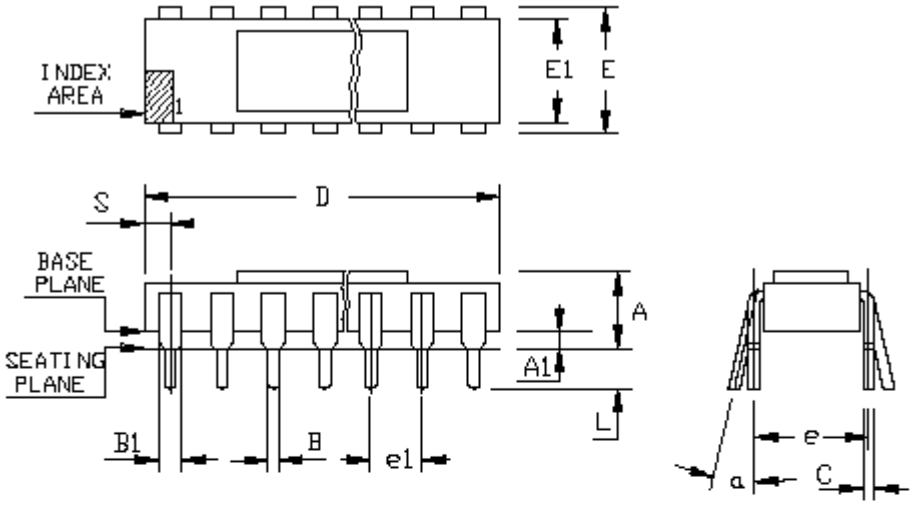
1/ Forcing conditions of the functional test, assure that these limits are met, but they will not be individually recorded.

2/ Read & Record measurements in accordance with MIL-PRF-38535.

3/ Tested at initial design and after major process changes, otherwise guaranteed.

Case X

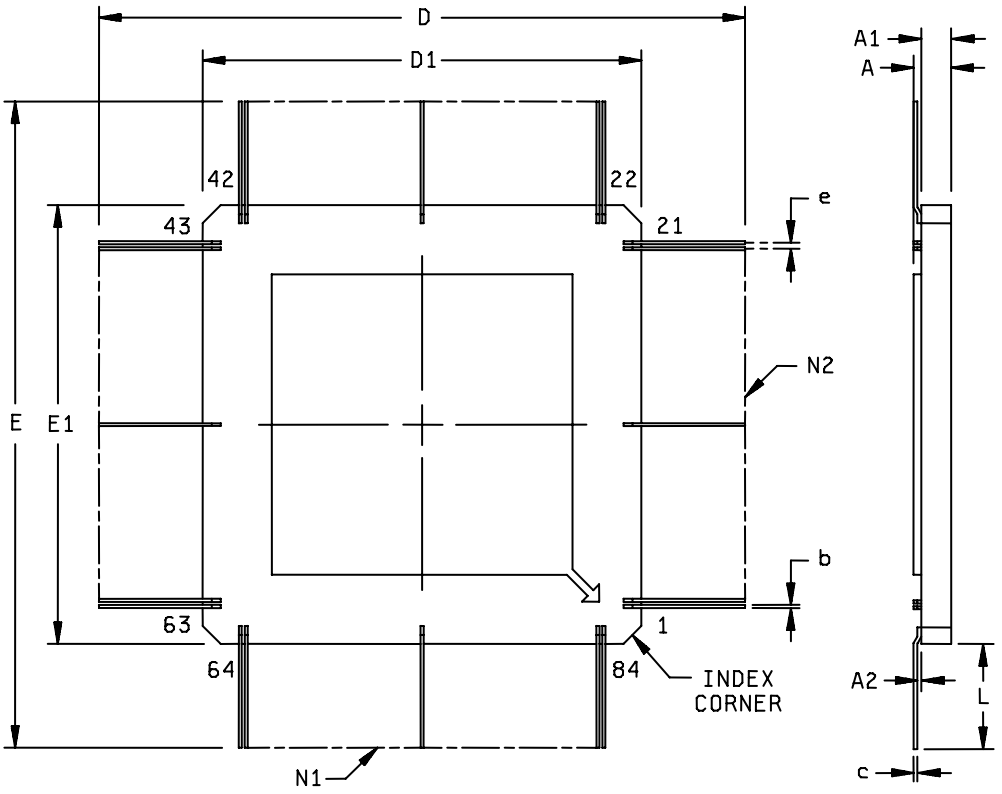
40 LEAD SIDE BRAZE .600



	MM		INCH	
A	2.16	4.83	.085	.190
A1	0.51	1.77	.020	.070
B	0.38	0.58	.015	.023
B1	0.97	1.52	.038	.060
C	0.20	0.30	.008	.012
D	50.30	51.56	1.980	2.030
E	15.12	15.87	.595	.625
E1	14.74	15.49	.580	.610
L	3.18	4.44	.125	.175
S	0.77	1.65	.030	.065
e	15.24	TYP	.600	TYP
e1	2.54	TYP	.100	TYP
a	0°		15°	
PKG STD	D1			

Figure 1. Case outlines

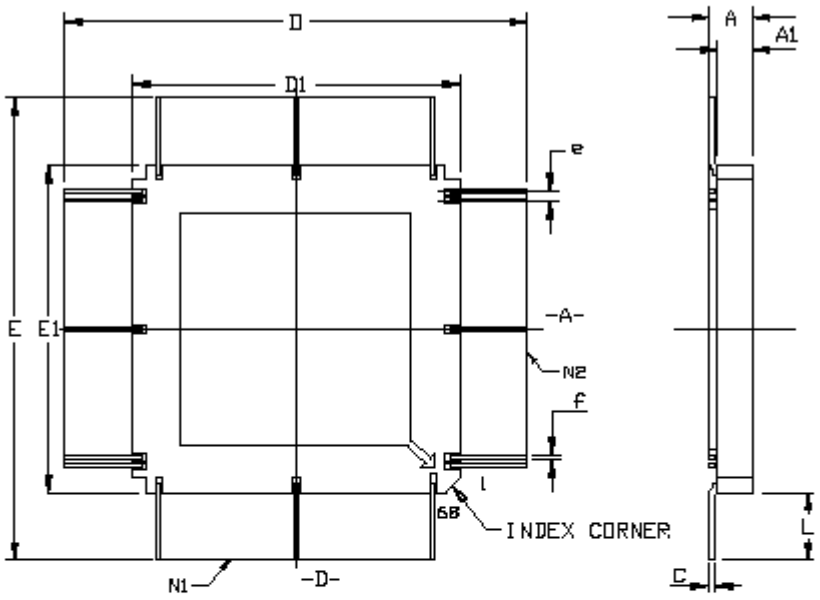
Case Y



Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.05	2.89	.081	.114	D1/E1	28.96	29.46	1.140	1.160
A1	1.82	2.67	.072	.105	e	1.270 BSC		.050 BSC	
A2		0.36		.014	f	0.46 REF		.018 REF	
C	0.22	0.31	.009	.012	L	7.60	8.20	.299	.323
D/E	44.16	45.86	1.738	1.806	N1/N2	21		21	

Figure 1. Case outline – Continued.

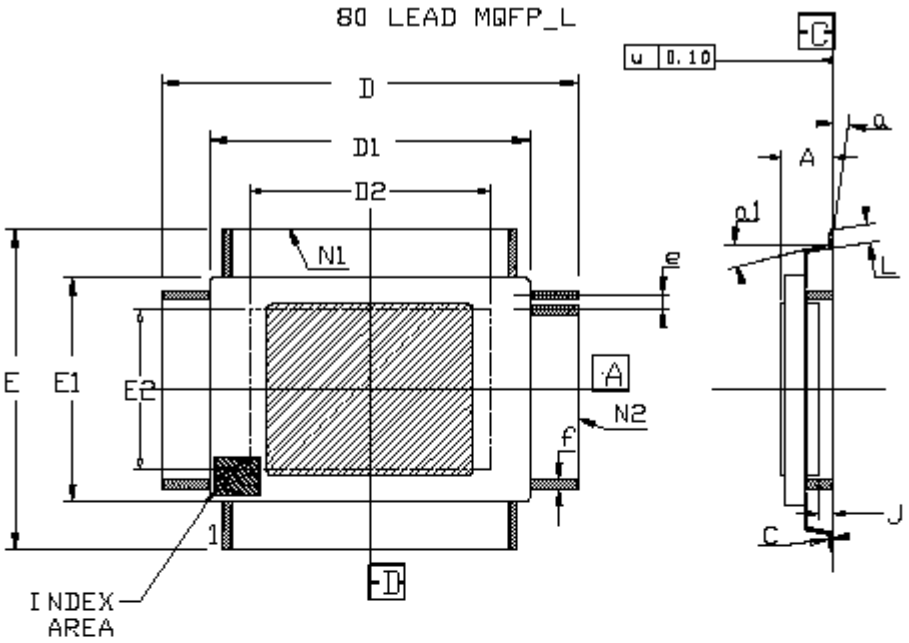
Case Z
68 LEAD MQFP_F



	mm		mils	
	Min	Max	Min	Max
A	2.21	2.54	.072	.100
C	0.10	0.20	.004	.008
D	41.66	47.50	1.640	1.870
D1	23.75	24.51	0.935	0.965
E	41.66	47.50	1.640	1.870
E1	23.75	24.51	0.935	0.965
e	1.270 BSC		.050 BSC	
f	0.30 BSC		.012 BSC	
A1	1.82	2.24	.072	.088
L	8.890	11.43	.350	.450
N1	17		17	
N2	17		17	

Figure 1. Case outline – Continued.

Case U



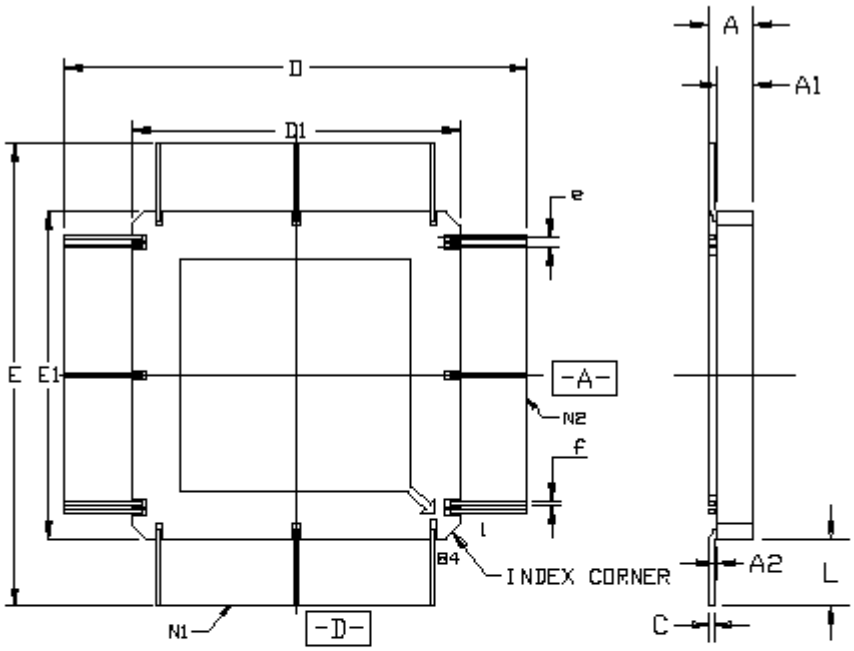
	MM		INCH	
	Min	Max	Min	Max
A	–	3.81	–	.150
C	0.15 TYP		.006 TYP	
D	23.76	24.48	.935	.964
D1	19.80	20.20	.780	.795
E	17.80	18.44	.701	.725
E1	13.85	14.15	.545	.557
e	0.80 BSC		.0315 BSC	
f	0.27	0.37	.010	.015
J	0.10	0.36	.004	.014
L	0.61	1.01	.024	.040
D2	15.87	16.13	.624	.635
E2	9.87	10.13	.388	.399
	α= 4°±4°		α1=7°±7°	
	N1=24		N2=16	

1/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the AID. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.

Figure 1. Case outline – Continued.

Case T

84 LEAD FLAT PACK

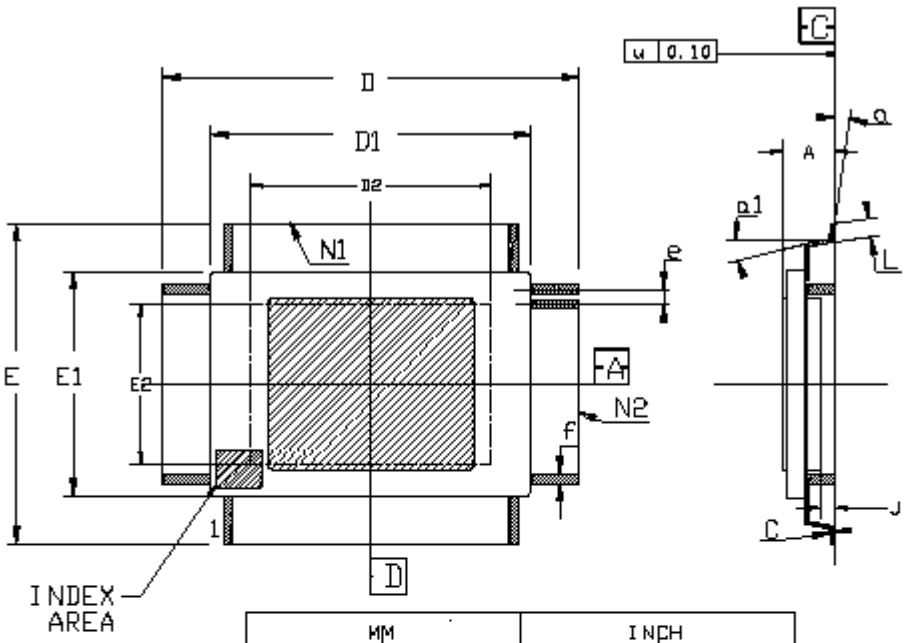


	mm		mils	
	Min	Max	Min	Max
A	1.80	2.44	.071	.096
C	0.10	0.20	.004	.008
D	33.66	34.93	1.325	1.375
D1	16.38	16.64	0.645	0.655
E	33.65	34.93	1.325	1.375
E1	16.38	16.64	0.645	0.655
e	0.635 BSC		.025 BSC	
f	0.20	0.30	.008	.012
A1	1.17	1.80	.046	.071
A2	0.05	0.36	.002	.014
L	8.636	9.144	.340	.360
N1	21		21	
N2	21		21	

Figure 1. Case outline – Continued.

Case M

100 LEAD MQFPL

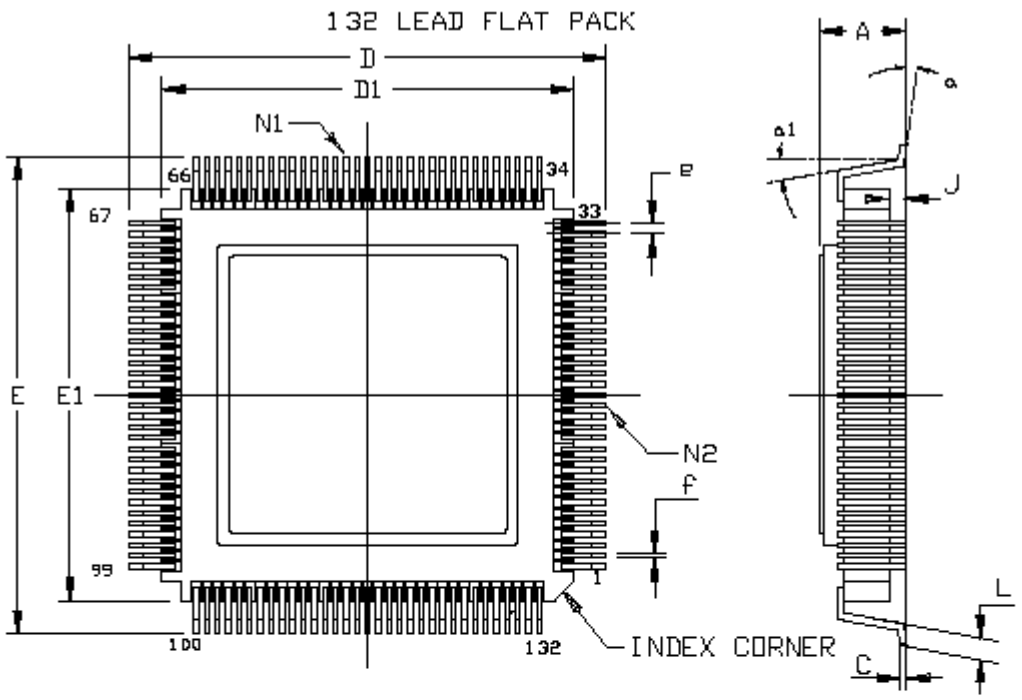


	MM		INCH	
	Min	Max	Min	Max
A	–	3.81	–	.150
C	0.15 TYP		.006 TYP	
D	23.76	24.48	.935	.964
D1	19.80	20.20	.780	.795
E	17.80	18.44	.701	.725
E1	13.85	14.15	.545	.557
e	0.65 BSC		.0256 BSC	
f	0.17	0.33	.0067	.013
J	0.10	0.36	.004	.014
L	0.61	1.01	.024	.040
D2	15.87	16.13	.624	.635
E2	9.87	10.13	.388	.399
	a= 4°±4°		a1=7°±7°	
	N1=30		N2=20	

1/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the AID. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.

Figure 1. Case outline – Continued.

Case N

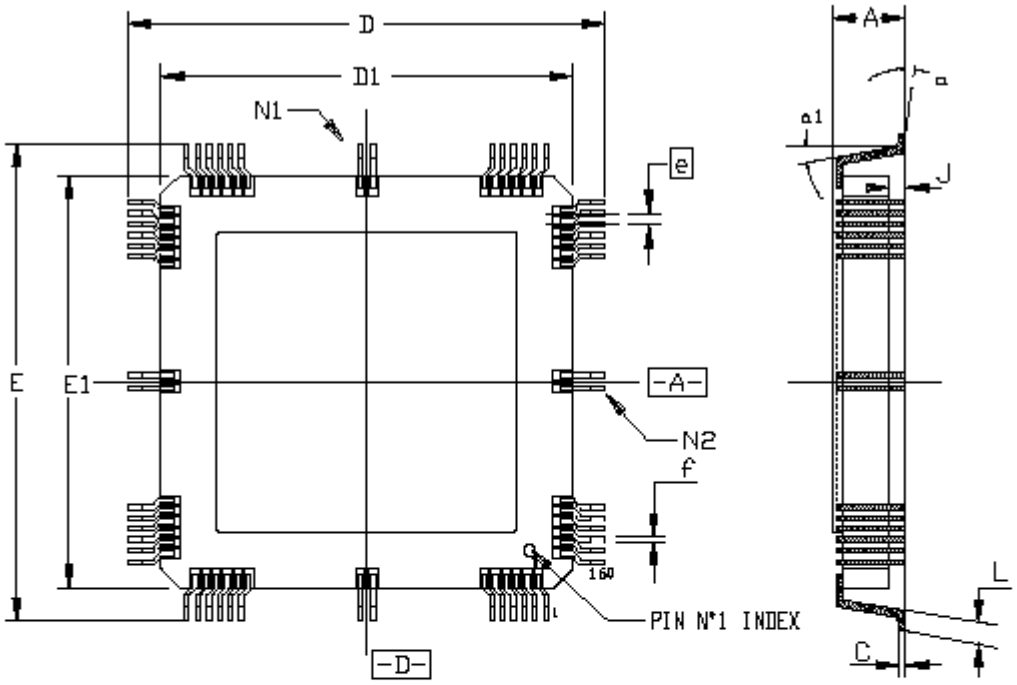


	MM		INCH	
	Min	Max	Min	Max
A	2.46	3.12	.097	.123
C	0.152 TYP		.006 TYP	
D	27.36	28.26	1.077	1.113
D1	24.00	24.38	.945	.960
E	27.36	28.26	1.077	1.113
E1	24.00	24.38	.945	.960
e	0.635 BSC		.025 BSC	
f	0.20 REF		.008 REF	
J	0.15	0.30	.006	.012
L	0.61	1.01	.024	.040
N1	33		33	
N2	33		33	
	α=4° ± 4°		α1=5° ± 5°	

1/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the AID. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.

Figure 1. Case outline – Continued.

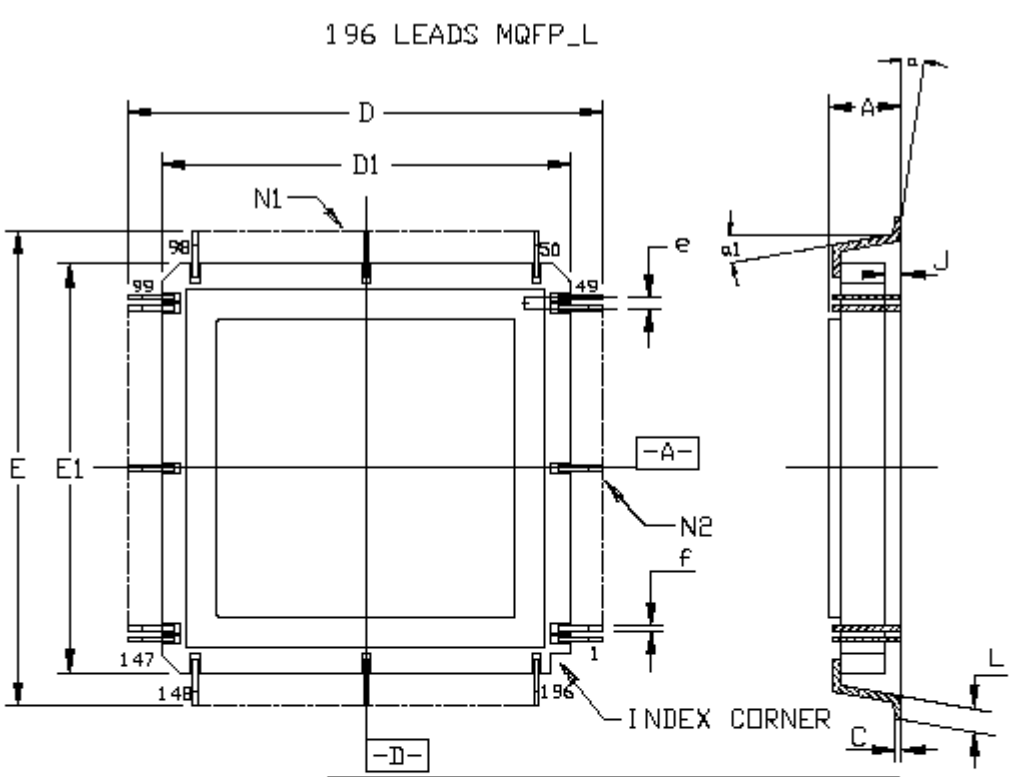
160 LEAD FLAT PACK



	MM		INCH	
	Min	Max	Min	Max
A	2.44	3.60	.096	.142
C	0.15 TYP		.006 TYP	
D	31.93	32.67	1.257	1.286
D1	26.93	27.47	1.060	1.082
E	31.93	32.67	1.257	1.286
E1	26.93	27.47	1.060	1.082
e	0.65 BSC		.0256 BSC	
f	0.30 REF		.012 REF	
J	0.50	1.00	.020	.040
L	1.21	1.41	.047	.056
N1	40		40	
N2	40		40	
	α=2° ± 3°		α1=5° ± 3°	

1/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the AID. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.

Figure 1. Case outline – Continued.



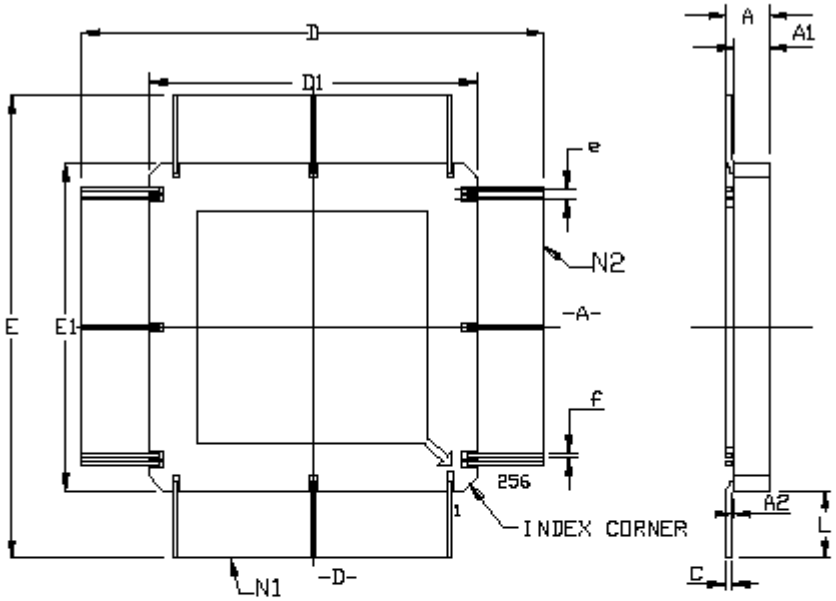
	Min	Max	Min	Max
A	-	2.95	-	.116
C	0.20 TYP		.008 TYP	
D	-	39.75	-	1.565
D1	-	34.54	-	1.360
E	-	39.75	-	1.565
E1	-	34.54	-	1.360
e	0.635 BSC		.025 BSC	
f	0.28 REF		.011 REF	
J	0.15	0.30	.006	.012
L	0.61	1.01	.024	.040
N1	49		49	
N2	49		49	
	a=4° ~ 4°		a1=5° ~ 5°	

1/ The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads in the AID. The leads for this optional package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete.

Figure 1. Case outline – Continued.

Case 6

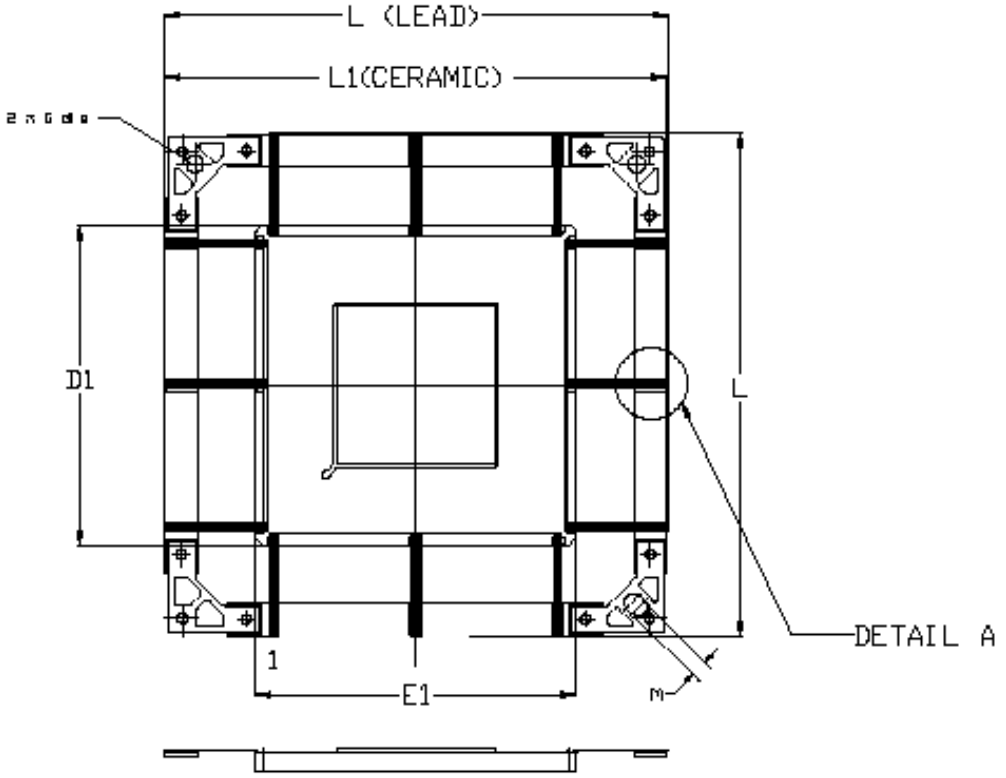
256 LEAD MQFP_F

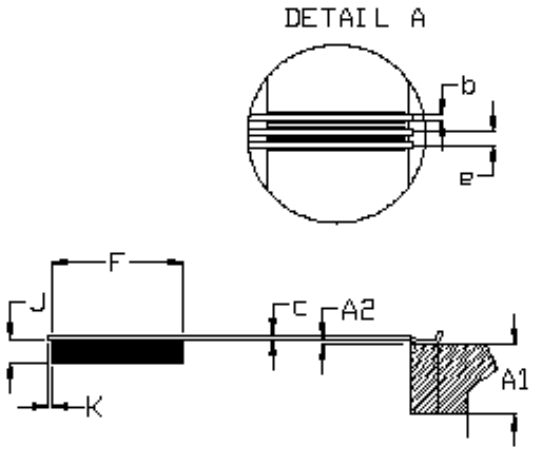


	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

Figure 1. Case outline – Continued.

352 LEADS FLAT PACK CERAMIC TIE BAR



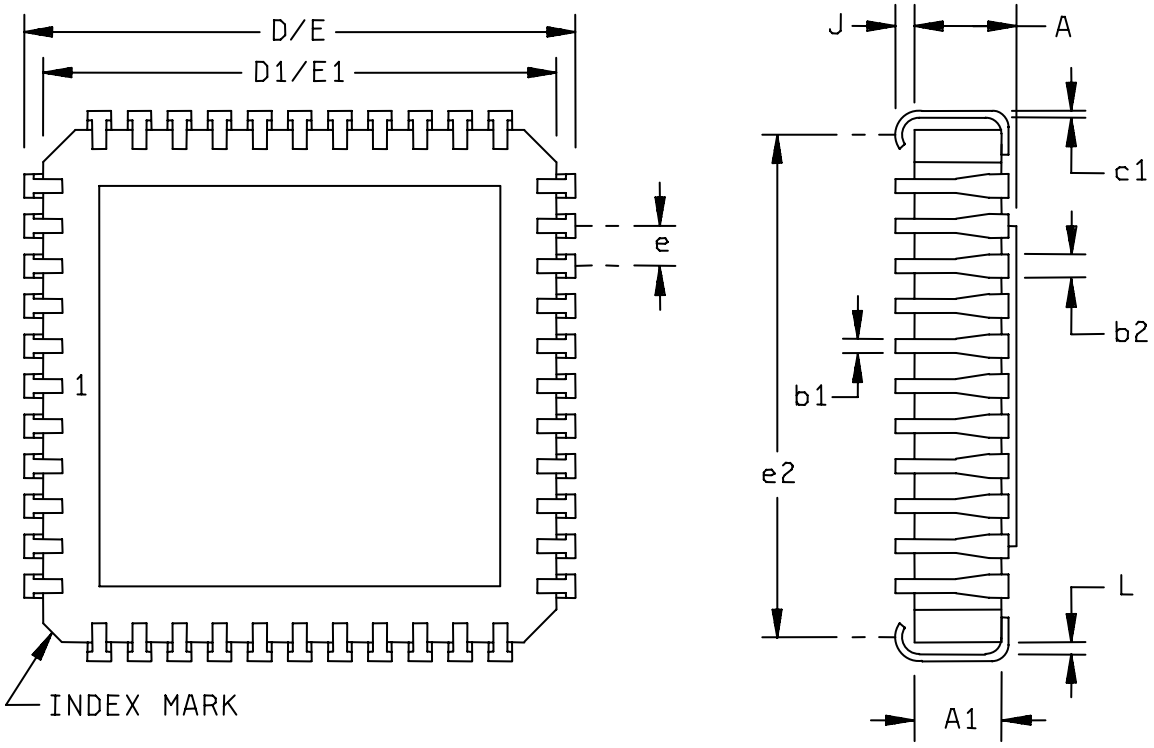


	mm		Inch	
	min	max	min	max
m	2.50	2.65	0.098	0.104
L3	65.85	65.95	2.592	2.596
L2	55.60	57.00	2.189	2.244
L1	74.60	75.40	2.947	3.008
L	74.85	76.40	2.947	3.008
K	----	0.50	-----	0.020
J	0.75	1.05	0.029	0.041
G	2.50	2.60	0.098	0.104
F	4.50	5.50	0.177	0.217
e	0.50	BASIC	0.019685	BASIC
D1-E1	47.52	48.48	1.871	1.908
c	0.11	0.20	0.004	0.008
b1	0.18	0.22	0.007	0.009
b	0.19	0.25	0.007	0.010
A2	0.05	0.36	0.002	0.014
A1	2.35	3.15	0.092	0.124
A	2.75	3.75	0.108	0.148

Figure 1. Case outline – Continued.

Case 8

44 LEAD QUAD CHIP CARRIER WITH J LEAD



	MM		INCH	
A	2.67	4.95	.105	.195
A1	1.65 NOM		.065 NOM	
b1	0.33	0.56	.013	.022
b2	0.55	0.88	.022	.035
c1	0.17	0.25	.007	.010
D/E	17.14	17.78	.675	.700
D1/E1	15.74	16.76	.620	.660
e	1.27 BSC		.050 BSC	
e2	16.00 BSC		.063 BSC	
L	0.12	-	.005	-
ND/NE	11		11	
R	0.50	1.01	.020	.040
J	0.58	-	.023	-

Figure 1. Case outline – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition is described in the AID. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class Q and V, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein) or as described in the manufacturers QM plan.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition as described in the AID. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition “B” unless otherwise specified in the AID.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

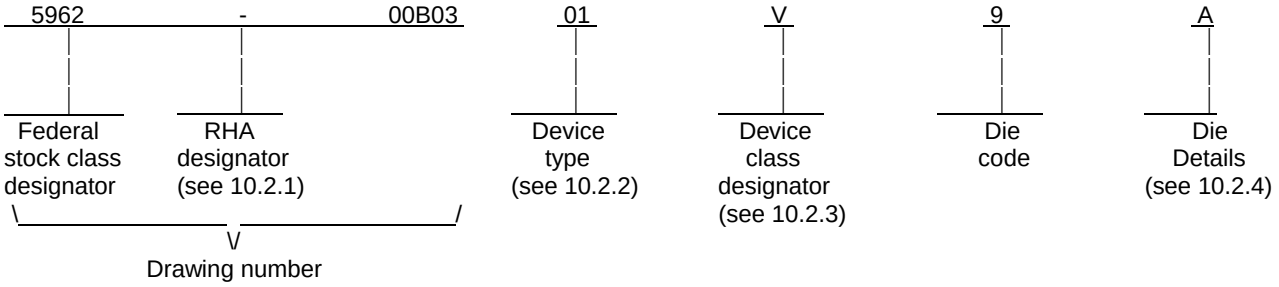
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
03	MG2044P	44,000 gates available
04	MG2142P	142,000 gates available
05	MG2270P	270,000 gates available

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
03	A-1
04	A-2
05	A-3

10.2.4.3. Interface materials.

Die type	Figure number
03	A-1
04	A-2
05	A-3

10.2.4.4. Assembly related information.

Die type	Figure number
03	A-1
04	A-2
05	A-3

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1, A-2 and A-3.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1, A-2 and A-3.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1, A-2 and A-3.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1, A-2 and A-3.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.3.13 of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or 'Q' as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. verification

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified within paragraphs 4.4.4 and 4.4.4.1.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0547.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Due to the complexity of the device, a graphical representation of the pad locations is not available. This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions

Die physical dimensions-.
Die size: 5,400 x 5,450 microns (with scribe line)
Die thickness: 475 microns

Interface materials.
Top metallization: Aluminium + Copper
Backside metallization: Bare Silicon

Glassivation.
Type: Oxinitride
Thickness: 10,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: not connected
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

Pads Location

pad	X	Y	type
1	21.020	25.274	POWER
2	19.920	25.274	
3	18.820	25.274	
4	17.720	25.274	
5	16.620	25.274	
6	15.520	25.274	
7	14.420	25.274	
8	13.320	25.274	
9	12.220	25.274	
10	11.120	25.274	
11	10.020	25.274	
12	8.921	25.274	
13	7.820	25.274	
14	6.720	25.274	
15	5.620	25.274	
16	4.520	25.274	
17	3.420	25.274	
18	2.321	25.274	
19	1.220	25.274	
20	0.120	25.274	
21	-0.979	25.274	
22	-2.079	25.274	
23	-3.179	25.274	
24	-4.279	25.274	
25	-5.379	25.274	
26	-6.479	25.274	
27	-7.580	25.274	
28	-8.680	25.274	
29	-9.780	25.274	
30	-10.880	25.274	
31	-11.979	25.274	
32	-13.079	25.274	
33	-14.180	25.274	
34	-15.279	25.274	
35	-16.380	25.274	
36	-17.479	25.274	
37	-18.579	25.274	

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
38	-20.793	25.274	BLOCK
39	-21.993	25.274	BLOCK
40	-25.040	23.796	BLOCK_NOPO
41	-25.040	22.550	BLOCK
42	-25.040	21.351	BLOCK
43	-25.040	20.154	
44	-25.040	19.054	
45	-25.040	17.954	
46	-25.040	16.854	
47	-25.040	15.755	
48	-25.040	14.654	
49	-25.040	13.555	
50	-25.040	12.454	
51	-25.040	11.354	
52	-25.040	10.255	
53	-25.040	9.155	
54	-25.040	8.055	
55	-25.040	6.955	
56	-25.040	5.854	
57	-25.040	4.755	
58	-25.040	3.655	
59	-25.040	2.554	
60	-25.040	1.454	
61	-25.040	0.354	
62	-25.040	-0.745	
63	-25.040	-1.845	
64	-25.040	-2.946	
65	-25.040	-4.045	
66	-25.040	-5.145	
67	-25.040	-6.245	
68	-25.040	-7.345	
69	-25.040	-8.445	
70	-25.040	-9.546	
71	-25.040	-10.645	
72	-25.040	-11.745	
73	-25.040	-12.845	
74	-25.040	-13.945	
75	-25.040	-15.045	
76	-25.040	-16.145	
77	-25.040	-17.245	

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
78	-25.040	-18.345	
79	-25.040	-19.445	
80	-25.040	-20.545	POWER
81	-25.040	-21.645	POWER
82	-25.040	-22.745	POWER
83	-24.268	-25.274	POWER
84	-23.168	-25.274	POWER
85	-22.068	-25.274	POWER
86	-20.968	-25.274	POWER
87	-19.868	-25.274	
88	-18.768	-25.274	
89	-17.668	-25.274	
90	-16.568	-25.274	
91	-15.468	-25.274	
92	-14.368	-25.274	
93	-13.268	-25.274	
94	-12.168	-25.274	
95	-11.068	-25.274	
96	-9.968	-25.274	
97	-8.868	-25.274	
98	-7.768	-25.274	
99	-6.668	-25.274	
100	-5.568	-25.274	
101	-4.468	-25.274	
102	-3.368	-25.274	
103	-2.268	-25.274	
104	-1.168	-25.274	
105	-0.068	-25.274	
106	1.032	-25.274	
107	2.132	-25.274	
108	3.232	-25.274	
109	4.332	-25.274	
110	5.432	-25.274	
111	6.532	-25.274	
112	7.632	-25.274	
113	8.732	-25.274	
114	9.832	-25.274	
115	10.932	-25.274	
116	12.032	-25.274	
117	13.132	-25.274	

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
118	14.232	-25.274	
119	15.332	-25.274	
120	16.432	-25.274	
121	17.532	-25.274	
122	18.632	-25.274	
123	20.793	-25.274	BLOCK
124	21.993	-25.274	BLOCK
125	25.040	-23.796	BLOCK_NOPO
126	25.040	-22.550	BLOCK
127	25.040	-21.351	BLOCK
128	25.040	-20.154	
129	25.040	-19.054	
130	25.040	-17.954	
131	25.040	-16.854	
132	25.040	-15.755	
133	25.040	-14.654	
134	25.040	-13.555	
135	25.040	-12.454	
136	25.040	-11.354	
137	25.040	-10.255	
138	25.040	-9.155	
139	25.040	-8.055	
140	25.040	-6.955	
141	25.040	-5.854	
142	25.040	-4.755	
143	25.040	-3.655	
144	25.040	-2.554	
145	25.040	-1.454	
146	25.040	-0.354	
147	25.040	0.745	
148	25.040	1.845	
149	25.040	2.946	
150	25.040	4.045	
151	25.040	5.145	
152	25.040	6.245	
153	25.040	7.345	
154	25.040	8.445	
155	25.040	9.546	
156	25.040	10.645	
157	25.040	11.745	

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
158	25.040	12.845	
159	25.040	13.945	
160	25.040	15.045	
161	25.040	16.145	
162	25.040	17.245	
163	25.040	18.345	
164	25.040	19.445	
165	25.040	22.250	BLOCK
166	25.040	23.350	BLOCK

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

Due to the complexity of the device, a graphical representation of the pad locations is not available. This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions

Die physical dimensions-.
Die size: 8,600 x 8,510 microns (with scribe line)
Die thickness: 475 microns

Interface materials.
Top metallization: Aluminium + Copper
Backside metallization: Bare Silicon

Glassivation.
Type: Oxinitride
Thickness: 10,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: not connected
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

Pads Location

pad	X	Y	type
1	37.020	40.566	POWER
2	35.920	40.566	
3	34.820	40.566	
4	33.721	40.566	
5	32.620	40.566	
6	31.520	40.566	
7	30.420	40.566	
8	29.320	40.566	
9	28.221	40.566	
10	27.120	40.566	
11	26.020	40.566	
12	24.920	40.566	
13	23.820	40.566	
14	22.720	40.566	
15	21.620	40.566	
16	20.520	40.566	
17	19.420	40.566	
18	18.320	40.566	
19	17.220	40.566	
20	16.120	40.566	
21	15.020	40.566	
22	13.921	40.566	
23	12.820	40.566	
24	11.721	40.566	
25	10.620	40.566	
26	9.521	40.566	
27	8.421	40.566	
28	7.321	40.566	
29	6.220	40.566	
30	5.120	40.566	
31	4.020	40.566	
32	2.920	40.566	
33	1.821	40.566	
34	0.721	40.566	
35	-0.379	40.566	
36	-1.480	40.566	
37	-2.580	40.566	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
38	-3.679	40.566	
39	-4.779	40.566	
40	-5.880	40.566	
41	-6.979	40.566	
42	-8.079	40.566	
43	-9.179	40.566	
44	-10.279	40.566	
45	-11.380	40.566	
46	-12.479	40.566	
47	-13.579	40.566	
48	-14.679	40.566	
49	-15.779	40.566	
50	-16.880	40.566	
51	-17.979	40.566	
52	-19.079	40.566	
53	-20.179	40.566	
54	-21.279	40.566	
55	-22.380	40.566	
56	-23.480	40.566	
57	-24.579	40.566	
58	-25.679	40.566	
59	-26.779	40.566	
60	-27.880	40.566	
61	-28.979	40.566	
62	-30.079	40.566	
63	-31.180	40.566	
64	-32.279	40.566	
65	-33.380	40.566	
66	-34.479	40.566	
67	-35.579	40.566	
68	-36.794	40.566	BLOCK
69	-37.993	40.566	BLOCK
70	-41.041	39.087	BLOCK_NOPO
71	-41.041	37.842	BLOCK
72	-41.041	36.642	BLOCK
73	-41.041	35.447	
74	-41.041	34.346	
75	-41.041	33.246	
76	-41.041	32.146	
77	-41.041	31.046	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
78	-41.041	29.947	
79	-41.041	28.846	
80	-41.041	27.746	
81	-41.041	26.646	
82	-41.041	25.547	
83	-41.041	24.446	
84	-41.041	23.346	
85	-41.041	22.247	
86	-41.041	21.146	
87	-41.041	20.046	
88	-41.041	18.947	
89	-41.041	17.846	
90	-41.041	16.747	
91	-41.041	15.646	
92	-41.041	14.546	
93	-41.041	13.446	
94	-41.041	12.347	
95	-41.041	11.246	
96	-41.041	10.146	
97	-41.041	9.046	
98	-41.041	7.946	
99	-41.041	6.846	
100	-41.041	5.747	
101	-41.041	4.646	
102	-41.041	3.546	
103	-41.041	2.446	
104	-41.041	1.346	
105	-41.041	0.246	
106	-41.041	-0.853	
107	-41.041	-1.954	
108	-41.041	-3.054	
109	-41.041	-4.154	
110	-41.041	-5.253	
111	-41.041	-6.353	
112	-41.041	-7.454	
113	-41.041	-8.553	
114	-41.041	-9.653	
115	-41.041	-10.754	
116	-41.041	-11.853	
117	-41.041	-12.954	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
118	-41.041	-14.053	
119	-41.041	-15.153	
120	-41.041	-16.253	
121	-41.041	-17.354	
122	-41.041	-18.453	
123	-41.041	-19.553	
124	-41.041	-20.654	
125	-41.041	-21.753	
126	-41.041	-22.853	
127	-41.041	-23.954	
128	-41.041	-25.053	
129	-41.041	-26.153	
130	-41.041	-27.253	
131	-41.041	-28.354	
132	-41.041	-29.453	
133	-41.041	-30.553	
134	-41.041	-31.653	
135	-41.041	-32.754	
136	-41.041	-33.853	
137	-41.041	-34.953	
138	-41.041	-36.053	POWER
139	-41.041	-37.154	POWER
140	-41.041	-38.253	POWER
141	-40.268	-40.566	POWER
142	-39.168	-40.566	POWER
143	-38.068	-40.566	POWER
144	-36.968	-40.566	POWER
145	-35.868	-40.566	
146	-34.768	-40.566	
147	-33.668	-40.566	
148	-32.568	-40.566	
149	-31.468	-40.566	
150	-30.368	-40.566	
151	-29.268	-40.566	
152	-28.168	-40.566	
153	-27.068	-40.566	
154	-25.968	-40.566	
155	-24.868	-40.566	
156	-23.768	-40.566	
157	-22.668	-40.566	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
158	-21.568	-40.566	
159	-20.468	-40.566	
160	-19.368	-40.566	
161	-18.268	-40.566	
162	-17.168	-40.566	
163	-16.068	-40.566	
164	-14.968	-40.566	
165	-13.868	-40.566	
166	-12.768	-40.566	
167	-11.668	-40.566	
168	-10.568	-40.566	
169	-9.468	-40.566	
170	-8.368	-40.566	
171	-7.268	-40.566	
172	-6.168	-40.566	
173	-5.068	-40.566	
174	-3.968	-40.566	
175	-2.868	-40.566	
176	-1.768	-40.566	
177	-0.668	-40.566	
178	0.432	-40.566	
179	1.532	-40.566	
180	2.632	-40.566	
181	3.732	-40.566	
182	4.832	-40.566	
183	5.932	-40.566	
184	7.032	-40.566	
185	8.132	-40.566	
186	9.232	-40.566	
187	10.332	-40.566	
188	11.432	-40.566	
189	12.532	-40.566	
190	13.632	-40.566	
191	14.732	-40.566	
192	15.832	-40.566	
193	16.932	-40.566	
194	18.032	-40.566	
195	19.132	-40.566	
196	20.232	-40.566	
197	21.332	-40.566	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
198	22.432	-40.566	
199	23.532	-40.566	
200	24.632	-40.566	
201	25.732	-40.566	
202	26.832	-40.566	
203	27.932	-40.566	
204	29.032	-40.566	
205	30.132	-40.566	
206	31.232	-40.566	
207	32.332	-40.566	
208	33.432	-40.566	
209	34.532	-40.566	
210	35.632	-40.566	
211	36.794	-40.566	BLOCK
212	37.993	-40.566	BLOCK
213	41.041	-39.087	BLOCK_NOPO
214	41.041	-37.842	BLOCK
215	41.041	-36.642	BLOCK
216	41.041	-35.447	
217	41.041	-34.346	
218	41.041	-33.246	
219	41.041	-32.146	
220	41.041	-31.046	
221	41.041	-29.947	
222	41.041	-28.846	
223	41.041	-27.746	
224	41.041	-26.646	
225	41.041	-25.547	
226	41.041	-24.446	
227	41.041	-23.346	
228	41.041	-22.247	
229	41.041	-21.146	
230	41.041	-20.046	
231	41.041	-18.947	
232	41.041	-17.846	
233	41.041	-16.747	
234	41.041	-15.646	
235	41.041	-14.546	
236	41.041	-13.446	
237	41.041	-12.347	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
238	41.041	-11.246	
239	41.041	-10.146	
240	41.041	-9.046	
241	41.041	-7.946	
242	41.041	-6.846	
243	41.041	-5.747	
244	41.041	-4.646	
245	41.041	-3.546	
246	41.041	-2.446	
247	41.041	-1.346	
248	41.041	-0.246	
249	41.041	0.853	
250	41.041	1.954	
251	41.041	3.054	
252	41.041	4.154	
253	41.041	5.253	
254	41.041	6.353	
255	41.041	7.454	
256	41.041	8.553	
257	41.041	9.653	
258	41.041	10.754	
259	41.041	11.853	
260	41.041	12.954	
261	41.041	14.053	
262	41.041	15.153	
263	41.041	16.253	
264	41.041	17.354	
265	41.041	18.453	
266	41.041	19.553	
267	41.041	20.654	
268	41.041	21.753	
269	41.041	22.853	
270	41.041	23.954	
271	41.041	25.053	
272	41.041	26.153	
273	41.041	27.253	
274	41.041	28.354	
275	41.041	29.453	
276	41.041	30.553	
277	41.041	31.653	

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
278	41.041	32.754	
279	41.041	33.853	
280	41.041	34.953	
281	41.041	36.053	POWER
282	41.041	37.542	BLOCK
283	41.041	38.642	BLOCK

FIGURE A-2. Die bonding pad locations and electrical functions – Continued

Due to the complexity of the device, a graphical representation of the pad locations is not available. This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions

Die physical dimensions-.
Die size: 11,300 x 11,610 microns (with scribe line)
Die thickness: 475 microns

Interface materials.
Top metallization: Aluminium + Copper
Backside metallization: Bare Silicon

Glassivation.
Type: Oxinitride
Thickness: 10,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: not connected
Special assembly instructions: None

FIGURE A-3. Die bonding pad locations and electrical functions

Pads Location

pad	X	Y	type
1	49.695	54.486	POWER
2	48.595	54.486	
3	47.495	54.486	
4	46.395	54.486	
5	45.295	54.486	
6	44.196	54.486	
7	43.096	54.486	
8	41.995	54.486	
9	40.895	54.486	
10	39.795	54.486	
11	38.695	54.486	
12	37.596	54.486	
13	36.495	54.486	
14	35.395	54.486	
15	34.295	54.486	
16	33.196	54.486	
17	32.095	54.486	
18	30.995	54.486	
19	29.895	54.486	
20	28.796	54.486	
21	27.695	54.486	
22	26.595	54.486	
23	25.495	54.486	
24	24.396	54.486	
25	23.295	54.486	
26	22.195	54.486	
27	21.096	54.486	
28	19.995	54.486	
29	18.895	54.486	
30	17.796	54.486	
31	16.695	54.486	
32	15.595	54.486	
33	14.495	54.486	
34	13.396	54.486	
35	12.295	54.486	
36	11.196	54.486	
37	10.095	54.486	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
38	8.995	54.486	
39	7.896	54.486	
40	6.795	54.486	
41	5.696	54.486	
42	4.595	54.486	
43	3.495	54.486	
44	2.395	54.486	
45	1.296	54.486	
46	0.195	54.486	
47	-0.905	54.486	
48	-2.004	54.486	
49	-3.104	54.486	
50	-4.204	54.486	
51	-5.304	54.486	
52	-6.404	54.486	
53	-7.504	54.486	
54	-8.604	54.486	
55	-9.704	54.486	
56	-10.804	54.486	
57	-11.905	54.486	
58	-13.004	54.486	
59	-14.104	54.486	
60	-15.204	54.486	
61	-16.305	54.486	
62	-17.404	54.486	
63	-18.505	54.486	
64	-19.604	54.486	
65	-20.705	54.486	
66	-21.805	54.486	
67	-22.904	54.486	
68	-24.004	54.486	
69	-25.105	54.486	
70	-26.204	54.486	
71	-27.304	54.486	
72	-28.404	54.486	
73	-29.505	54.486	
74	-30.604	54.486	
75	-31.704	54.486	
76	-32.804	54.486	
77	-33.904	54.486	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
78	-35.005	54.486	
79	-36.104	54.486	
80	-37.205	54.486	
81	-38.304	54.486	
82	-39.404	54.486	
83	-40.504	54.486	
84	-41.605	54.486	
85	-42.704	54.486	
86	-43.804	54.486	
87	-44.904	54.486	
88	-46.004	54.486	
89	-47.105	54.486	
90	-48.205	54.486	
91	-49.468	54.486	BLOCK
92	-50.668	54.486	BLOCK
93	-53.715	53.007	BLOCK_NOPO
94	-53.715	51.761	BLOCK
95	-53.715	50.561	BLOCK
96	-53.715	49.365	
97	-53.715	48.266	
98	-53.715	47.165	
99	-53.715	46.065	
100	-53.715	44.965	
101	-53.715	43.865	
102	-53.715	42.765	
103	-53.715	41.666	
104	-53.715	40.566	
105	-53.715	39.465	
106	-53.715	38.365	
107	-53.715	37.266	
108	-53.715	36.165	
109	-53.715	35.066	
110	-53.715	33.965	
111	-53.715	32.865	
112	-53.715	31.765	
113	-53.715	30.665	
114	-53.715	29.566	
115	-53.715	28.465	
116	-53.715	27.365	
117	-53.715	26.265	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
118	-53.715	25.166	
119	-53.715	24.065	
120	-53.715	22.965	
121	-53.715	21.866	
122	-53.715	20.766	
123	-53.715	19.666	
124	-53.715	18.566	
125	-53.715	17.465	
126	-53.715	16.366	
127	-53.715	15.265	
128	-53.715	14.165	
129	-53.715	13.065	
130	-53.715	11.966	
131	-53.715	10.865	
132	-53.715	9.765	
133	-53.715	8.665	
134	-53.715	7.565	
135	-53.715	6.465	
136	-53.715	5.365	
137	-53.715	4.265	
138	-53.715	3.165	
139	-53.715	2.065	
140	-53.715	0.966	
141	-53.715	-0.135	
142	-53.715	-1.234	
143	-53.715	-2.334	
144	-53.715	-3.434	
145	-53.715	-4.534	
146	-53.715	-5.635	
147	-53.715	-6.734	
148	-53.715	-7.835	
149	-53.715	-8.934	
150	-53.715	-10.034	
151	-53.715	-11.135	
152	-53.715	-12.234	
153	-53.715	-13.335	
154	-53.715	-14.434	
155	-53.715	-15.534	
156	-53.715	-16.634	
157	-53.715	-17.735	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
158	-53.715	-18.834	
159	-53.715	-19.934	
160	-53.715	-21.035	
161	-53.715	-22.134	
162	-53.715	-23.234	
163	-53.715	-24.334	
164	-53.715	-25.434	
165	-53.715	-26.534	
166	-53.715	-27.634	
167	-53.715	-28.735	
168	-53.715	-29.834	
169	-53.715	-30.934	
170	-53.715	-32.034	
171	-53.715	-33.135	
172	-53.715	-34.234	
173	-53.715	-35.334	
174	-53.715	-36.434	
175	-53.715	-37.535	
176	-53.715	-38.634	
177	-53.715	-39.734	
178	-53.715	-40.834	
179	-53.715	-41.934	
180	-53.715	-43.034	
181	-53.715	-44.135	
182	-53.715	-45.234	
183	-53.715	-46.334	
184	-53.715	-47.434	
185	-53.715	-48.534	
186	-53.715	-49.635	
187	-53.715	-50.734	POWER
188	-53.715	-51.834	POWER
189	-52.943	-54.486	POWER
190	-51.843	-54.486	POWER
191	-50.743	-54.486	POWER
192	-49.643	-54.486	POWER
193	-48.543	-54.486	
194	-47.443	-54.486	
195	-46.343	-54.486	
196	-45.243	-54.486	
197	-44.143	-54.486	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
198	-43.043	-54.486	
199	-41.943	-54.486	
200	-40.843	-54.486	
201	-39.743	-54.486	
202	-38.643	-54.486	
203	-37.543	-54.486	
204	-36.443	-54.486	
205	-35.343	-54.486	
206	-34.243	-54.486	
207	-33.143	-54.486	
208	-32.043	-54.486	
209	-30.943	-54.486	
210	-29.843	-54.486	
211	-28.743	-54.486	
212	-27.643	-54.486	
213	-26.543	-54.486	
214	-25.443	-54.486	
215	-24.343	-54.486	
216	-23.243	-54.486	
217	-22.143	-54.486	
218	-21.043	-54.486	
219	-19.943	-54.486	
220	-18.843	-54.486	
221	-17.743	-54.486	
222	-16.643	-54.486	
223	-15.543	-54.486	
224	-14.443	-54.486	
225	-13.343	-54.486	
226	-12.243	-54.486	
227	-11.143	-54.486	
228	-10.043	-54.486	
229	-8.943	-54.486	
230	-7.843	-54.486	
231	-6.743	-54.486	
232	-5.643	-54.486	
233	-4.543	-54.486	
234	-3.443	-54.486	
235	-2.343	-54.486	
236	-1.243	-54.486	
237	-0.143	-54.486	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
238	0.957	-54.486	
239	2.057	-54.486	
240	3.157	-54.486	
241	4.257	-54.486	
242	5.357	-54.486	
243	6.457	-54.486	
244	7.557	-54.486	
245	8.657	-54.486	
246	9.757	-54.486	
247	10.857	-54.486	
248	11.957	-54.486	
249	13.057	-54.486	
250	14.157	-54.486	
251	15.257	-54.486	
252	16.357	-54.486	
253	17.457	-54.486	
254	18.557	-54.486	
255	19.657	-54.486	
256	20.757	-54.486	
257	21.857	-54.486	
258	22.957	-54.486	
259	24.057	-54.486	
260	25.157	-54.486	
261	26.257	-54.486	
262	27.357	-54.486	
263	28.457	-54.486	
264	29.557	-54.486	
265	30.657	-54.486	
266	31.757	-54.486	
267	32.857	-54.486	
268	33.957	-54.486	
269	35.057	-54.486	
270	36.157	-54.486	
271	37.257	-54.486	
272	38.357	-54.486	
273	39.457	-54.486	
274	40.557	-54.486	
275	41.657	-54.486	
276	42.757	-54.486	
277	43.857	-54.486	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
278	44.957	-54.486	
279	46.057	-54.486	
280	47.157	-54.486	
281	48.257	-54.486	
282	49.468	-54.486	BLOCK
283	50.668	-54.486	BLOCK
284	53.715	-53.007	BLOCK_NOPO
285	53.715	-51.761	BLOCK
286	53.715	-50.561	BLOCK
287	53.715	-49.365	
288	53.715	-48.266	
289	53.715	-47.165	
290	53.715	-46.065	
291	53.715	-44.965	
292	53.715	-43.865	
293	53.715	-42.765	
294	53.715	-41.666	
295	53.715	-40.566	
296	53.715	-39.465	
297	53.715	-38.365	
298	53.715	-37.266	
299	53.715	-36.165	
300	53.715	-35.066	
301	53.715	-33.965	
302	53.715	-32.865	
303	53.715	-31.765	
304	53.715	-30.665	
305	53.715	-29.566	
306	53.715	-28.465	
307	53.715	-27.365	
308	53.715	-26.265	
309	53.715	-25.166	
310	53.715	-24.065	
311	53.715	-22.965	
312	53.715	-21.866	
313	53.715	-20.766	
314	53.715	-19.666	
315	53.715	-18.566	
316	53.715	-17.465	
317	53.715	-16.366	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
318	53.715	-15.265	
319	53.715	-14.165	
320	53.715	-13.065	
321	53.715	-11.966	
322	53.715	-10.865	
323	53.715	-9.765	
324	53.715	-8.665	
325	53.715	-7.565	
326	53.715	-6.465	
327	53.715	-5.365	
328	53.715	-4.265	
329	53.715	-3.165	
330	53.715	-2.065	
331	53.715	-0.966	
332	53.715	0.135	
333	53.715	1.234	
334	53.715	2.334	
335	53.715	3.434	
336	53.715	4.534	
337	53.715	5.635	
338	53.715	6.734	
339	53.715	7.835	
340	53.715	8.934	
341	53.715	10.034	
342	53.715	11.135	
343	53.715	12.234	
344	53.715	13.335	
345	53.715	14.434	
346	53.715	15.534	
347	53.715	16.634	
348	53.715	17.735	
349	53.715	18.834	
350	53.715	19.934	
351	53.715	21.035	
352	53.715	22.134	
353	53.715	23.234	
354	53.715	24.334	
355	53.715	25.434	
356	53.715	26.534	
357	53.715	27.634	

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

Pads Location

pad	X	Y	type
358	53.715	28.735	
359	53.715	29.834	
360	53.715	30.934	
361	53.715	32.034	
362	53.715	33.135	
363	53.715	34.234	
364	53.715	35.334	
365	53.715	36.434	
366	53.715	37.535	
367	53.715	38.634	
368	53.715	39.734	
369	53.715	40.834	
370	53.715	41.934	
371	53.715	43.034	
372	53.715	44.135	
373	53.715	45.234	
374	53.715	46.334	
375	53.715	47.434	
376	53.715	48.534	
377	53.715	49.635	
378	53.715	51.461	BLOCK
379	53.715	52.561	BLOCK

FIGURE A-3. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-03-17

Approved sources of supply for SMD 5962-00B03 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/
5962-00B0303Q4C 3/	F7400	MMFW-G2044PHxxxMQ
5962-00B0303V4C 3/	F7400	SMFW-G2044PHxxxSV
5962R00B0303V4C 3/	F7400	SMFW-G2044PHxxxSR
5962-00B0303Q9A 3/	F7400	MM0-G2044PHxxxMQ
5962-00B0303V9A 3/	F7400	SM0-G2044PHxxxSV
5962-00B0303QNC 3/	F7400	MMF7-G2044PHxxxMQ
5962-00B0303VNC 3/	F7400	SMF7-G2044PHxxxSV
5962R00B0303VNC 3/	F7400	SMF7-G2044PHxxxSR
5962-00B0304Q9A 3/	F7400	MM0-G2142PHxxxMQ
5962-00B0304V9A 3/	F7400	SM0-G2142PHxxxSV
5962-00B0304Q5C 3/	F7400	MMF9-G2142PHxxxMQ 4/ MMK9-G2142PHxxxMQ 5/
5962-00B0304V5C 3/	F7400	SMF9-G2142PHxxxSV 4/ SMK9-G2142PHxxxSV 5/
5962R00B0304V5C 3/	F7400	SMF9-G2142PHxxxSR 4/ SMK9-G2142PHxxxSR 5/
5962-00B0304Q4C 3/	F7400	MMFW-G2142PHxxxMQ
5962-00B0304V4C 3/	F7400	SMFW-G2142PHxxxSV
5962R00B0304V4C 3/	F7400	SMFW-G2142PHxxxSR
5962-00B0304QNC 3/	F7400	MMF7-G2142PHxxxMQ
5962-00B0304VNC 3/	F7400	SMF7-G2142PHxxxSV
5962R00B0304VNC 3/	F7400	SMF7-G2142PHxxxSR
5962-00B0304Q6C 3/	F7400	MMKZ-G2142PHxxxMQ
5962-00B0304V6C 3/	F7400	SMKZ-G2142PHxxxSV
5962R00B0304V6C 3/	F7400	SMKZ-G2142PHxxxSR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/
5962-00B0305Q9A 3/	F7400	MM0-G2270PHxxxMQ
5962-00B0305V9A 3/	F7400	SM0-G2270PHxxxSV
5962-00B0305Q5C 3/	F7400	MMF9-G2270PHxxxMQ 4/ MMK9-G2270PHxxMQ 5/
5962-00B0305V5C 3/	F7400	SMF9-G2270PHxxxSV 4/ SMK9-G2270PHxxxSV 5/
5962R00B0305V5C 3/	F7400	SMF9-G2270PHxxxSR 4/ SMK9-G2270PHxxxSR 5/
5962-00B0305Q4C 3/	F7400	MMFW-G2270PHxxxMQ
5962-00B0305V4C 3/	F7400	SMFW-G2270PHxxxSV
5962R00B0305V4C 3/	F7400	SMFW-G2270PHxxxSR
5962-00B0305QNC 3/	F7400	MMF7-G2270PHxxxMQ
5962-00B0305VNC 3/	F7400	SMF7-G2270PHxxxSV
5962R00B0305VNC 3/	F7400	SMF7-G2270PHxxxSR
5962-00B0305Q6C 3/	F7400	MMKZ-G2270PHxxxMQ
5962-00B0305V6C 3/	F7400	SMKZ-G2270PHxxxSV
5962R00B0305V6C 3/	F7400	SMKZ-G2270PHxxxSR
5962-00B0305Q7C 3/	F7400	MMYC-G2270PHxxxMQ
5962-00B0305V7C 3/	F7400	SMYC-G2270PHxxxSV
5962R00B0305V7C 3/	F7400	SMYC-G2270PHxxxSR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing. The “xxx” is reserved to indicate the customer specific code
3/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID.
4/ For unformed leads.
5/ For formed leads.

Vendor CAGE number	Vendor name and address
F7400	Atmel La Chantrerie 44306 Nantes Cedex3 France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.