MEC1621/MEC1621i

Low Power 32-bit Microcontroller with Embedded Flash

Product Features

- 3.3V Operation
- ACPI Compliant
- LPC Interface
  - LPC I/O Cycles Decoded
- VTR (standby) and VBAT (Power Planes)
  - Low Standby Current in Sleep Mode
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- ARC-625D Embedded Controller (EC)
  - 16 KB Single Cycle 32-bit Wide Dual-ported SRAM, Accessible as Closely Coupled Data Memory and Instruction Memory
  - 32 x 32 x 64 Fast Multiply
  - Divide Assist and Saturation Arithmetic
  - Maskable Interrupt Aggregator/Accelerator Interface
  - Maskable Hardware Wake-Up Events
  - Sleep mode
  - JTAG Debug Port, Includes JTAG Master
  - MCU Serial Debug Port
  - 8-Channel DMA Interface Supports SMBus Controllers and EC/Host GP-SPI Controllers
  - Delay Register
  - Boot ROM
- Embedded Flash
  - 192 KB user space 32-bit Access, 30 ns Access Time, 10 K Cycles Endurance
  - 1 KB EEPROM Emulation, 40 ns Access Time, 250 K Cycles Endurance
  - Programmable by LPC, EC and JTAG Interfaces
  - Flash Security Enhancements
    - 4K Boot Block Protection
    - Direct JTAG and Direct LPC-protected (2) Pages at or Near Top of Memory for Password Protection
- Legacy Support
  - Fast GATEA20 & Fast CPU_RESET
- System to EC Message Interface
  - 8042 Style Host Interface
  - Embedded Memory Interface
    - Host Serial or Parallel IRQ Source
    - Provides Two Windows to On-Chip SRAM for Host Access

- Two Register Mailbox Command Interface
- Host Access of Virtual Registers Without EC Intervention
- Mailbox Registers Interface
  - Thirty-two 8-Bit Scratch Registers
  - Two Register Mailbox Command Interface
  - Two Register SMI Source Interface
- ACPI Embedded Controller Interface
  - Four Instances
  - 1 or 4 Byte Full Duplex Bidirectional Data Transfer Capable
- ACPI Power Management Interface
  - SCI Event-Generating Functions
- BIOS Debug Port
  - ISA Port 80 Plug-in Card Emulation
  - 2 Instances
  - Time Stamping Option
- Battery Backed Resources
  - Power-Fail Status Register
  - 32 KHz Clock Generator
  - Week Alarm Timer Interface with Programmable Wake-up from 1ms to 45 Days
  - VBAT-Powered Control Interface
    - 6 Latched Inputs
    - GPIO Capable
  - VBAT-Backed 64 Byte Memory
- Three EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 400 KHz Capable
  - Hardware Bus Access "Fairness" Interface
  - SMBus Time-outs Interface
  - 12 Port Flexible Multiplexing
  - Port Isolation
- PECI Interface 3.0
- Keyboard Matrix Scan Interface
  - 18 x 8 Interrupt/Wake Capable Multiplexed Keyboard Scan Matrix
  - Row Predrive Option

MEC1621/MEC1621i

- Three independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
- 146 General Purpose I/O Pins
  - 8 GPIO Pass-Through Port (GPTP)
- 3-pin LED Interface
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
  - Operational in EC Sleep States
- Programmable 16-bit Counter/Timer Interface
  - Four Wake-capable 16-bit Auto-reloading Counter/Timer Instances
  - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement.
  - 4 External Inputs, 4 External Outputs
- Hibernation Timer Interface
  - Two 32.768 KHz Driven Timers
  - Programmable Wake-up from 0.5ms to 128 Minutes
- System Watch Dog Timer (WDT)
- Input Capture and Compare Timer
  - 32-bit Free-running timer
  - Six 32-bit Capture Registers
  - Two 32-bit Compare Registers
  - Capture, Compare and Overflow Interrupts
- BC-Link^{TM} Interconnection Bus
  - Two High Speed and one Low Speed Bus Masters Controllers
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
  - One 3-pin EC-driven Full Duplex Serial Communication Interface
  - One 4-pin EC/Host-driven Full Duplex Serial Communication Interface to SPI Flash Interface
  - Flexible Clock Rates
  - SPI Burst Capable
- FAN Support
  - 16 Programmable Pulse-Width Modulator Outputs
    - Multiple Clock Rates
    - 16-Bit 'On' & 16-Bit 'Off' Counters
  - 6 Fan Tachometers
  - 6 x 2 Capture/Compare Timer Interface
- ADC Interface
  - 10-bit Conversion in 10μs
  - 16 Channels
  - Integral Non-Linearity of ±0.5 LSB; Differential Non-Linearity of ±0.5 LSB

- HDMI-CEC Interface Controller
- Thermal Monitoring Interface
  - 4 Temperature Channels
    - 3 External Channels
    - 1 Internal Channel
    - Diode or Thermistor Support
  - Fail-Safe Temperature Feature
    - Dedicated hands-off monitoring on Temperature Channel 1
    - HW Strapping for Threshold Temperature and for Diode/Thermistor choice
    - System Shutdown output, Integrated with EC VCI_OUT logic
- Two Pin Debug Port with Standard 16C550A Register Interface
  - Accessible from Host and EC
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 2 Mbps
- Resistor/Capacitor Identification Detection (RC_ID)
  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIO's
  - Provides 8 Quantized States on One Pin
- Integrated Standby Power Reset Generator
- Gang Programmer Interface
  - JTAG Enabled
  - Supports Mass Programming and Mass Verify
  - JTAG Mass Erase
- Clock Generator
  - VBAT powered 32.768 KHz Oscillator ±2% Accuracy
    - VBAT powered 32.768 KHz external input
    - External Clock Auto Detect Option
  - Operational on Suspend Power
  - Programmable Clock Power Management Control & Distribution
  - 20.27 MHz (nom) Oscillator
- Packages:
  - 176 Pin LFBGA RoHS Compliant package
  - 225 Pin LFBGA RoHS Compliant package

Description

The MEC1621/MEC1621i is the mixed signal base component of a multi-device advanced I/O controller architecture. The MEC1621/MEC1621i incorporates a high-performance 32-bit ARC 625D embedded microcontroller with a 192 Kilobyte Embedded Flash Subsystem, 16 Kilobytes of SRAM and a 1 Kilobyte EEPROM Emulation. The MEC1621/MEC1621i communicates with the system host using the Intel® Low Pin Count bus.

The MEC1621/MEC1621i is the EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link™ communication protocol to access up to three companion components. The BC-Link™ protocol is peer-to-peer providing communication between the MEC1621/MEC1621i embedded controller and registers located in a companion.

The MEC1621/MEC1621i is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on" and system power management functions. The MEC1621/MEC1621i also contains an integrated VTR Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events as defined by the MEC1621/MEC1621i Wake Interface.

The MEC1621/MEC1621i defines a software development system interface that includes an MCU Serial Debug Port, a two pin serial debug port with a 16C550A register interface that is accessible to the EC or to the LPC host and can operate up to 2 MB/s, a flexible Flash programming interface, a BIOS Debug Port, Gang Programmer Interface, and a JTAG interface. The EC can also drive the JTAG interface as a master.

A top-level block diagram of the MEC1621/MEC1621i is shown below in .

MEC1621/MEC1621i

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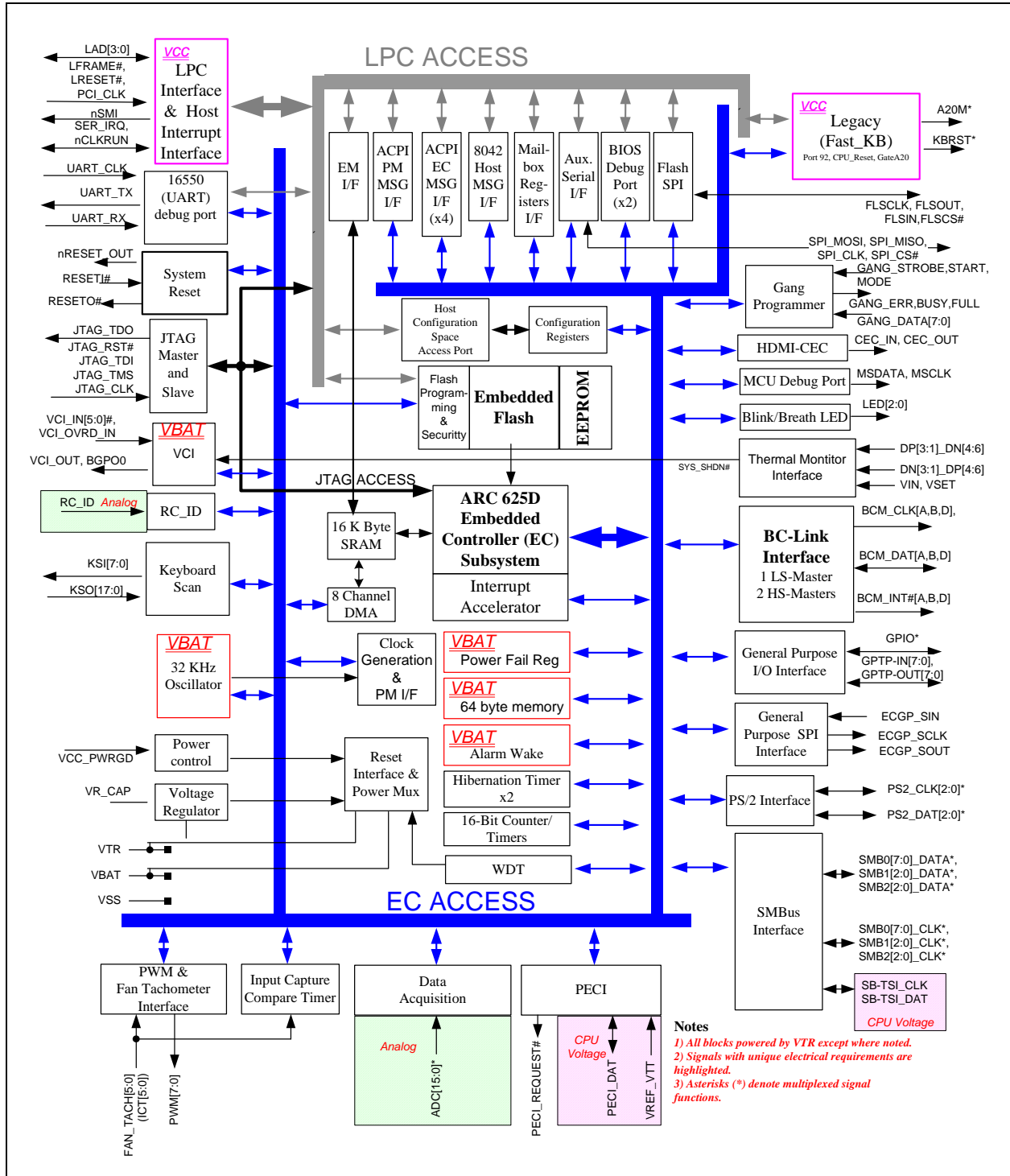- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

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Block Diagram

FIGURE 1:   MEC1621/MEC1621i Block Diagram

Package Outlines

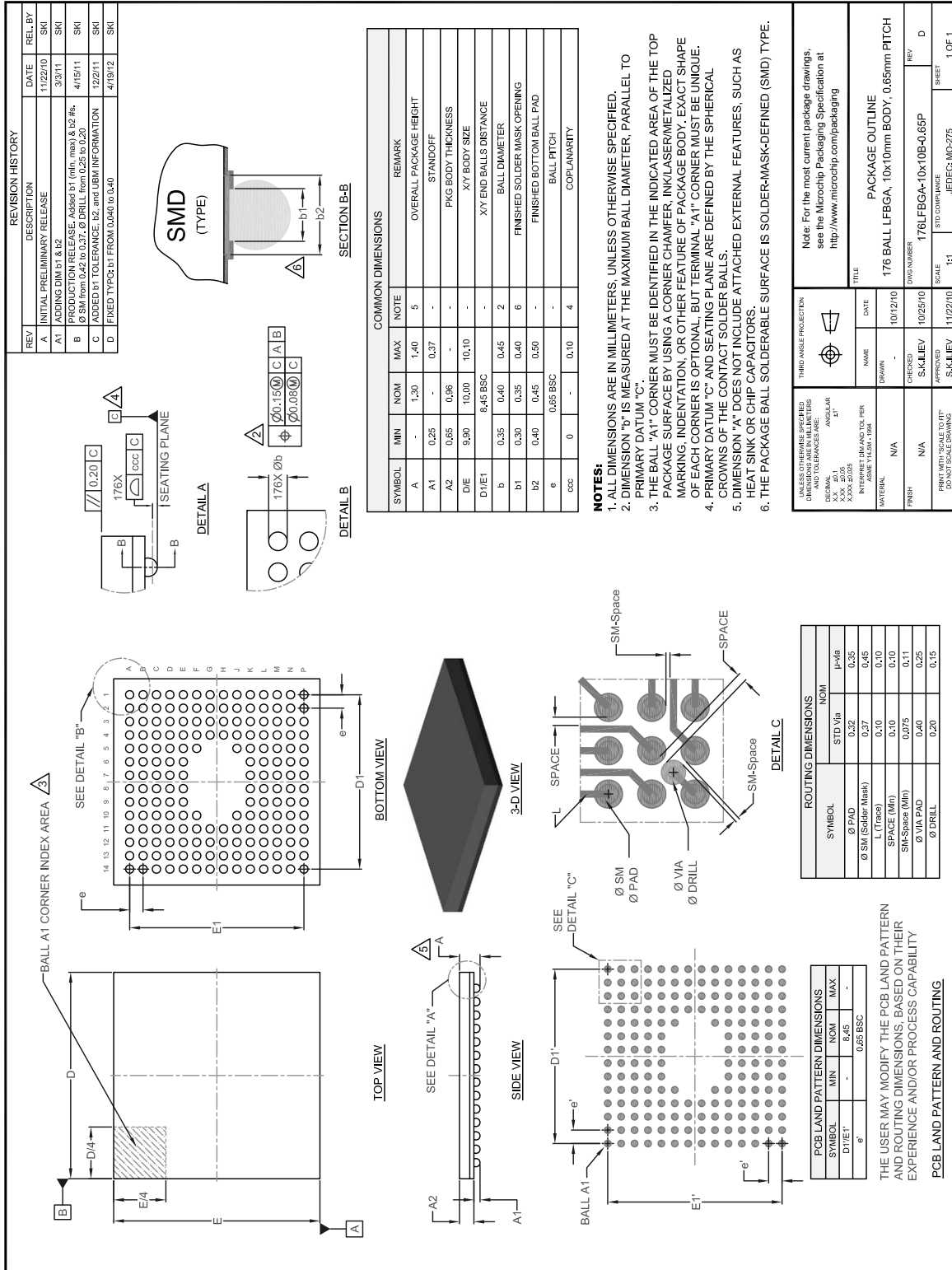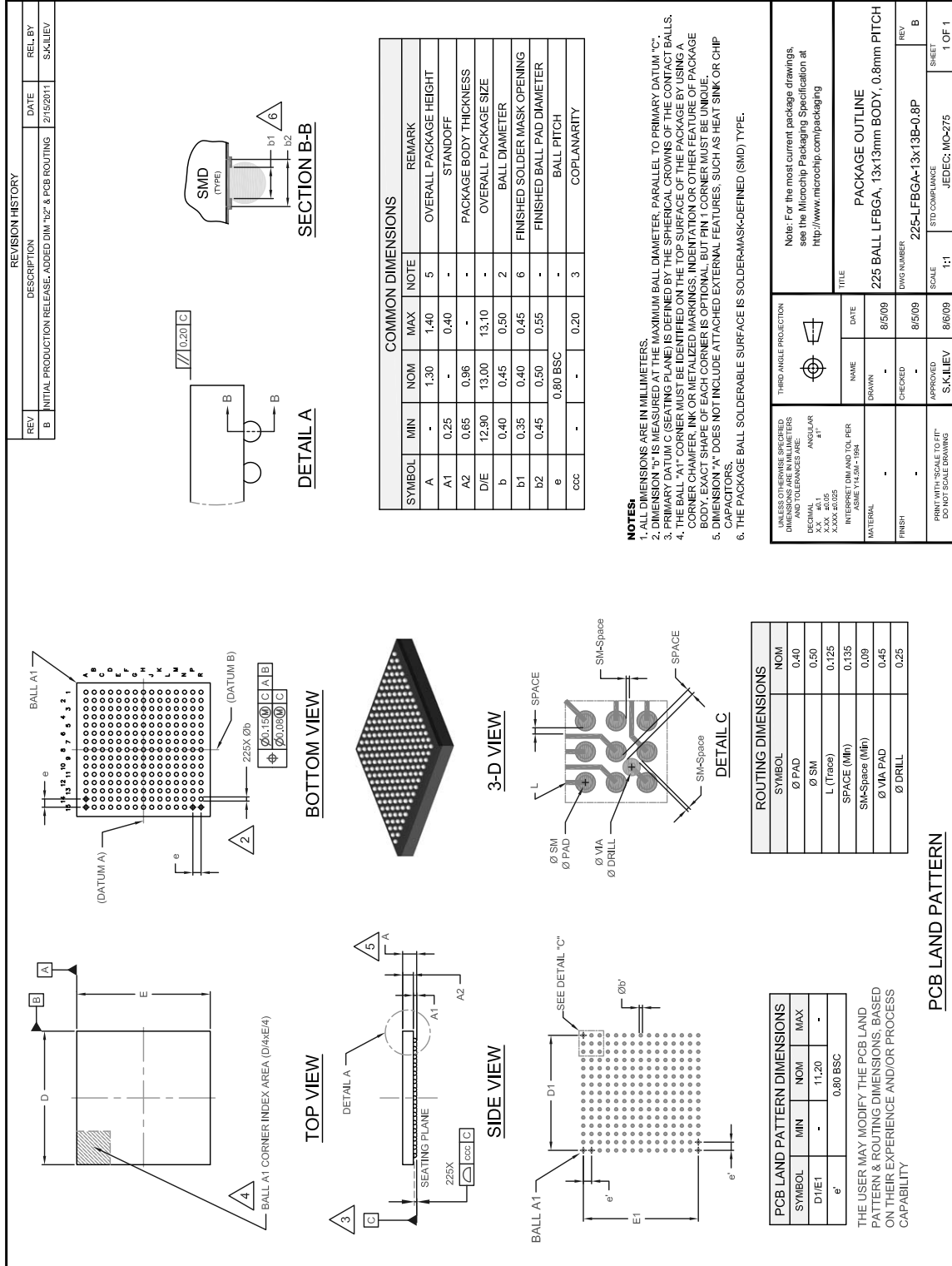**FIGURE 2:** 176-PIN LFBGA 10MM X 10MM BODY, 0.65MM PITCH

REVISION HISTORY

REV	DESCRIPTION	DATE	REL. BY
A	INITIAL PRELIMINARY RELEASE	11/22/10	SKI
A1	ADDING DIM b1 & b2	3/3/11	SKI
B	PRODUCTION RELEASE. Added b1 (min, max) & b2 #s. Ø SM from 0.42 to 0.37, Ø DRILL from 0.25 to 0.20	4/15/11	SKI
C	ADDED b1 TOLERANCE, b2, and UBM INFORMATION	12/2/11	SKI
D	FIXED TYPO: b1 FROM 0.040 to 0.40	4/19/12	SKI

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	1.30	1.40	5	OVERALL PACKAGE HEIGHT
A1	0.25	-	0.37	-	STANDOFF
A2	0.65	0.96	-	-	PKG BODY THICKNESS
D/E	9.90	10.00	10.10	-	X/Y BODY SIZE
D1/E1		8.45 BSC		-	X/Y END BALLS DISTANCE
b	0.35	0.40	0.45	2	BALL DIAMETER
b1	0.30	0.35	0.40	6	FINISHED SOLDER MASK OPENING
b2	0.40	0.45	0.50	-	FINISHED BOTTOM BALL PAD
e		0.65 BSC		-	BALL PITCH
ccc	0		0.10	4	COPLANARITY

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. THE BALL "A1" CORNER MUST BE IDENTIFIED IN THE INDICATED AREA OF THE TOP PACKAGE SURFACE BY USING A CORNER CHAMFER, INK/LASER/METALIZED MARKING, INDENTATION, OR OTHER FEATURE OF PACKAGE BODY. EXACT SHAPE OF EACH CORNER IS OPTIONAL, BUT TERMINAL "A1" CORNER MUST BE UNIQUE.
4. PRIMARY DATUM "C" AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT SOLDER BALLS.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.
6. THE PACKAGE BALL SOLDERABLE SURFACE IS SOLDER-MASK-DEFINED (SMD) TYPE.

SECTION B-B

SMD (TYPE)

DETAIL A

SEATING PLANE

176X

DETAIL B

176X Øb

BOTTOM VIEW

3-D VIEW

SEE DETAIL "B"

BALL A1 CORNER INDEX AREA

TOP VIEW

SEE DETAIL "A"

SIDE VIEW

DETAIL C

Ø SM
Ø PAD

Ø VIA
Ø DRILL

SM-Space

SPACE

ROUTING DIMENSIONS

SYMBOL	NOM	
	STD Via	µ-Via
Ø PAD	0.32	0.35
Ø SM (Solder Mask)	0.37	0.45
L (Trace)	0.10	0.10
SPACE (Min)	0.10	0.10
SM-Space (Min)	0.075	0.11
Ø VIA PAD	0.40	0.25
Ø DRILL	0.20	0.15

PCB LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
D1'/E1'	-	8.45	-
e'		0.65 BSC	

THE USER MAY MODIFY THE PCB LAND PATTERN AND ROUTING DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

PCB LAND PATTERN AND ROUTING

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS
AND TOLERANCES ARE:

DECIMAL   ANGULAR
X.X   ±0.1   ±1°
X.XX   ±0.05
X.XXX ±0.025

INTERPRET DIM AND TOL PER
ASME Y14.5M - 1994

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	-	10/12/10
CHECKED	S.K.ILIEV	10/25/10
APPROVED	S.K.ILIEV	11/22/10

| MATERIAL | N/A |
| FINISH | N/A |

PRINT WITH "X-SCALE TO FIT"
DO NOT SCALE DRAWING

PACKAGE OUTLINE

TITLE: 176 BALL LFBGA, 10x10mm BODY, 0.65mm PITCH

DWG NUMBER: 176LFBGA-10x10B-0.65P   REV D

STD COMPLIANCE: JEDEC: MO-275

SCALE: 1:1   SHEET: 1 OF 1

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FIGURE 3: **225-PIN LFBGA 13MM X 13MM BODY, 0.8MM PITCH**

REVISION HISTORY

REV	DESCRIPTION	DATE	REL. BY
B	INITIAL PRODUCTION RELEASE. ADDED DIM "b2" & PCB ROUTING	2/15/2011	S.K.ILIEV

SECTION B-B

SMD (TYPE)

DETAIL A

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	1.30	1.40	5	OVERALL PACKAGE HEIGHT
A1	0.25	-	0.40	-	STANDOFF
A2	0.65	0.96	-	-	PACKAGE BODY THICKNESS
D/E	12.90	13.00	13.10	-	OVERALL PACKAGE SIZE
b	0.40	0.45	0.50	2	BALL DIAMETER
b1	0.35	0.40	0.45	6	FINISHED SOLDER MASK OPENING
b2	0.45	0.50	0.55	-	FINISHED BALL PAD DIAMETER
e		0.80 BSC		-	BALL PITCH
ccc	-	-	0.20	3	COPLANARITY

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. THE BALL "A1" CORNER MUST BE IDENTIFIED ON THE TOP SURFACE OF THE PACKAGE BY USING A CORNER CHAMFER, INK OR METALIZED MARKINGS, INDENTATION OR OTHER FEATURE OF PACKAGE BODY, EXACT SHAPE OF EACH CORNER IS OPTIONAL, BUT PIN 1 CORNER MUST BE UNIQUE.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.
6. THE PACKAGE BALL SOLDERABLE SURFACE IS SOLDER-MASK-DEFINED (SMD) TYPE.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.025
ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	-	8/5/09
CHECKED	-	8/5/09
APPROVED	S.K.ILIEV	8/6/09

MATERIAL -
FINISH -

PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

TITLE
PACKAGE OUTLINE
225 BALL LFBGA, 13x13mm BODY, 0.8mm PITCH

DWG NUMBER
225-LFBGA-13x13B-0.8P
REV B

SCALE 1:1
STD COMPLIANCE JEDEC: MO-275
SHEET 1 OF 1

BOTTOM VIEW

BALL A1
(DATUM B)
225X Øb
225X Ø0.15 C A B
Ø0.08 C
(DATUM A)

3-D VIEW

DETAIL C

Ø SM
Ø PAD
Ø VIA
Ø DRILL
SPACE
SM-Space
SPACE
SM-Space

ROUTING DIMENSIONS

SYMBOL	NOM
Ø PAD	0.40
Ø SM	0.50
L (Trace)	0.125
SPACE (Min)	0.135
SM-Space (Min)	0.09
Ø VIA PAD	0.45
Ø DRILL	0.25

TOP VIEW

BALL A1 CORNER INDEX AREA (D/4xE/4)

DETAIL A

SIDE VIEW

SEATING PLANE
225X ccc C

SEE DETAIL "C"

PCB LAND PATTERN

BALL A1

PCB LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
D1/E1	-	11.20	-
e'		0.80 BSC	

THE USER MAY MODIFY THE PCB LAND PATTERN & ROUTING DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

MEC1621/MEC1621i

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: **REVISION HISTORY**

Revision	Section/Figure/Entry	Correction
DS00001774A (06-05-14)	Document Release	

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| PART NO. | [X] | - | XXX | - | [X]⁽¹⁾ |

PART NO.   [X]   -   XXX   -   [X]$^{(1)}$

Device   Temperature Range   Package   Tape and Reel Option

Device:	MEC1621, MEC1621i
Temperature Range:	Blank = 0°C to +85°C (Extended Commercial) i = -40°C to +85°C (Industrial)
Package:	RZP = 176-pin LFBGA VE = 225-pin LFBGA
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel$^{(1)}$

Examples:

a)   MEC1621-RZP
176-pin LFBGA (10mm x 10mm, 0.65mm pitch)
RoHS Compliant package

b)   MEC1621i-RZP
176-pin LFBGA (10mm x 10mm, 0.65mm pitch)
RoHS Compliant package
with Industrial Temperature rating

c)   MEC1621-VE
225-pin LFBGA (13mm x 13mm, 0.8mm pitch)
RoHS Compliant package

d)   MEC1621i-VE
225-pin LFBGA (13mm x 13mm, 0.8mm pitch)
RoHS Compliant package
with Industrial Temperature rating

Note 1:   Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 4,000.

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