Features

- Up to 1.6M Used Gates and 596 Pads with 3.3V, 3V and 2.5V Libraries
- High Speed - 170 ps Gate Delay - 2 Input NAND, FO = 2 (nominal)
- System Level Integration Technology Cores on Request
- Memories: SRAM and TPRAM, Gate Level or Embedded, with EDAC
- I/O Interfaces:
  - 5V Tolerant/Compliant (S) or 3V (R) Matrix Options
  - CMOS, LVTTL, LVDS, PCI, USB, etc.
  - Output Currents Programmable from 2 to 24 mA, by Step of 2 mA
  - Cold Sparing Buffers (2 µA Max. Leakage Current at 3.6V Worst Case Mil Temp.)
- 250 MHz PLL (on request), 220 MHz LVDS and 800 MHz Max. Toggle Frequency at 3.3V
- Deep Submicron CAD Flow
- ESD better than 2000V
- No Single Event Latch-Up below an LET Threshold of 80 MeV/mg/cm^2
- SEU Hardened Flip-flops
- Tested Up to a Total Dose of 300 Krad (Si) according to Mil STD 883 Method 1019
- Quality Grades
  - QML Q and V with SMD 5962-01B01 and 5962-08B01
  - ESCC QML with ESCC 9202 / 076

Rad Hard 1.6M Used Gates 0.35 µm CMOS Sea of Gates/ Embedded Array

MH1RT

Description

The MH1RT Gate Array and Embedded Array families from Atmel are fabricated on a radiation hardened 0.35 micron CMOS process, with up to 4 levels of metal for interconnect. This family features arrays with up to 1.6 million routable gates and 596 pads. The high density and high pin count capabilities of the MH1RT family, coupled with the ability to embed cores or memories on the same silicon, make the MH1RT series of arrays one of the best choices for System Level Integration.

The MH1RT series is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Verilog®, DFT®, Synopsys® and Vital are the reference front end tools. The Cadence® 'Logic Design Planner' floor planning associated with timing driven layout provides an efficient back end cycle.

The MH1RT series comes as a dual use of the MH1 series, adding:

- through process changes, the latch-up susceptibility better than 80 MeV/mg/cm^2 and the 300 Krad (Si) radiation level as required by most space programs.

- through cells relayout, an SEU built-in protection allowing to SEU harden only where it is necessary with respect to function requirements

With a background of 15 years experience, the MH1RT series comes as the Atmel 7th generation of ASIC series designed for radiation hardened applications.

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Table 1. List of Available MH1RT Matrices

Device Number	Typical Routable Gates	Max Pad Count	Max I/O Count	Gate Speed(1)	Max. Sites Count
MH1099E	519,000	332	324	180 ps	920,385
MH1156E	764,000	412	404	180 ps	1,447,975
MH1242E	1,198,000	512	504	180 ps	2,275,377
MH1332E	1,634,000	596	588	180 ps	3,098,804

Notes: 1. Nominal 2 Input NAND Gate FO = 2 at 3.3V.

Design

Design Systems Supported

Atmel supports several major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and estimated pre-route delay simulations.

The following design systems are supported:

Table 2. Supported design systems

System	Available Tools
Cadence	NCsim® - Verilog Simulator Encounter™ - Floorplanner RTL compiler® - Synthesis (Ambit)
Mentor/Model Tech	Questasim/Modelsim Verilog and VHDL (VITAL) Simulator DFT - Scan insertion and ATPG, BIST
Synopsys®	Design Compiler™ - Synthesis Primetime® - Static Path Formality® - Equivalence Checking DFTmax - Scan insertion and ATPG

Design Flow and Tools

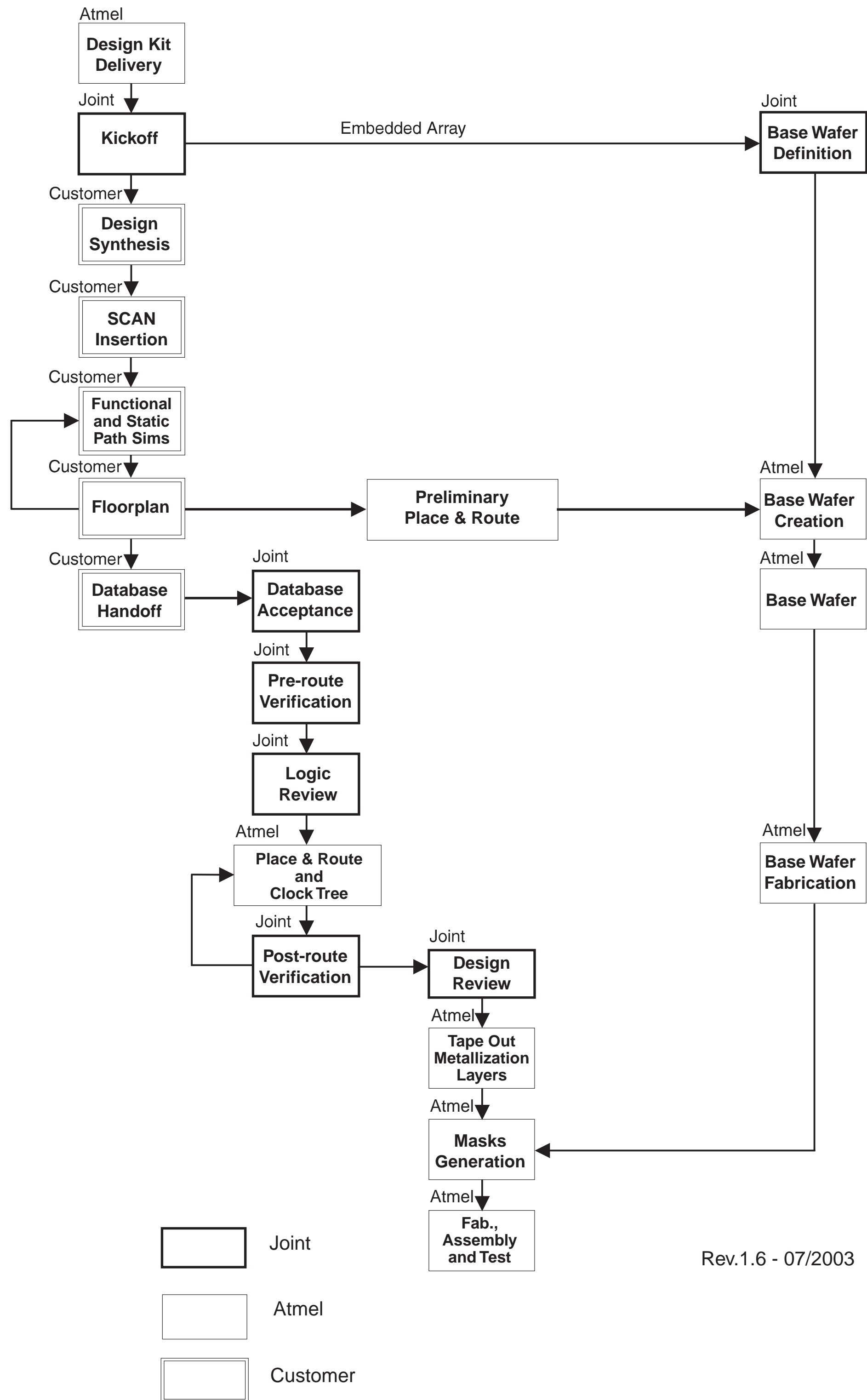
Atmel's design flow for Gate Array/Embedded Array is structured to allow the designer to consolidate the greatest number of system components possible onto the same silicon chip, using available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage, and process, and includes the effects of metal loading, inter-level capacitance, and edge rise and fall times. The Design Flow includes clock tree synthesis to minimize skew and latency. RC extraction is performed on final design database and incorporated into the timing analysis.

The Typical Gate Array/Embedded Array Design Flow, shown on page 4, provides a pictorial description of the typical interaction between Atmel's Gate Array/Embedded Array design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning, and SCAN insertion activities. Tools such as Synopsys Synthesis, Cadence and Mentor Logic Simulators are used, and many others are available. Should a design include embedded memory or an embedded core, Atmel needs to understand the partition of the Array, and define the location of the memory blocks and/or cores (preliminary place and route) so that an underlayer layout model can be created (Base Wafer).

Following the Logic Review, the design is routed, and post-route RC data is extracted. Following post-route verification and the Design Review, the design is taped out for fabrication.

The purpose of these reviews is to check the conformity of the design to Atmel rules, and acknowledge it in formal documents.

Figure 1. Typical Gate Array/Embedded Array Design Flow



Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5V compliant buffers, one buffer site must be reserved for the V_{DD5} pin, which is used to distribute power to the buffers.

Figure 2. Gate Array

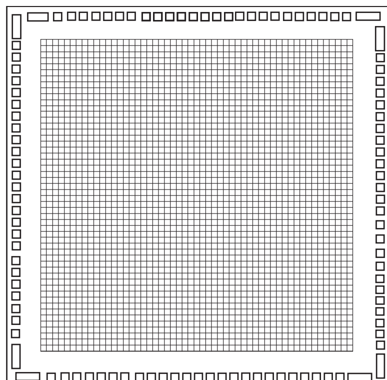
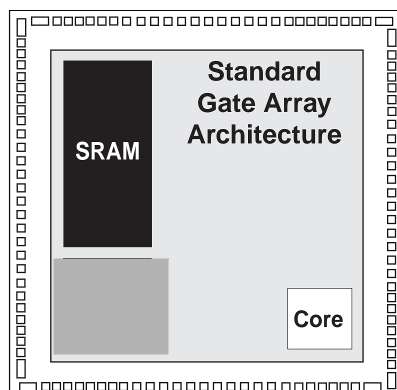


Figure 3. Embedded Array



I/O Site: Pad and Sub-Sections

The I/O sites can be configured as input, output, 3-state output and bidirectional buffers, each with pullup or pulldown capability, if required, by utilizing their corresponding sub-section. Bidirectionnal buffers are the result of an input and output buffers placed in adjacent sub-sections in the same I/O site. Special buffers may require multiple I/O sites. Oscillators require 2 I/O sites, each power and ground pin utilizes one I/O site.

PCI Buffers

PCI compatible input and output buffers are available for each bias voltage, 3V and 5V.

LVDS Buffers

Each LVDS buffer uses 2 I/O sites.

LVDS drivers are specific for each bias voltage and require one external current bias resistor per chip; LVDS receiver is the same for all bias voltages and requires 1 external line matching 100 Ω resistor per receiver.

Cold Sparing

It is the use of twice the same chip, A1 and A2, A1 ON and A2 OFF, with all signal pins/pads connected by pairs, A1I1 with A2I1, A101 with A201,...

During this mode operation:

- the chip OFF must survive and operate when turned ON without functional, AC, DC or reliability impact,
- the current pulled by the OFF chip must be limited to a low value: Atmel specification for their dedicated cold sparing buffers is 2 µA worst case by signal pins/pads.

For any other operation mode, refer to maximum ratings.

Memory Blocks

Memory blocks can be either synthesized on gates (when smaller than 8 bits) or compiled and embedded in the array itself. Various combinations of Through Flow or Bus Watch EDACs, 4, 8, 16 and 32 bit wide, can be used to alleviate the effect of SEU induced errors.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors (LSI Logic®, Motorola®, SMOS®, Oki®, NEC®, Fujitsu®, AMI® and others) into the gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-to-pin compatible, drop-in replacement.

Design Entry

Design entry is performed by the customer using an Atmel ASIC library. A complete netlist and vector set must then be provided to Atmel. Upon acceptance of this data set, Atmel continues with the standard design flow.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx®, Actel®, Altera®, AMD® and Atmel) into the gate arrays. There are four primary reasons to convert from an FPGA/PLD to a gate array. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

Cell Library

Atmel's MH1RT Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The MH1RT Series PLL operates at frequencies of up to 250 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization.

These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Cells	Number of Cells
Logic Cells	95
I/O Buffers 3V or 2.5V or 3.3V 5V Tolerant 5V Compliant	 110 36 70
Specific Cells LVDS, PCI	 11
SEU Hardened Cells	9
Cold Sparing	63

Electrical Characteristics

Absolute Maximum Ratings

Operating Ambient Temperature .... -55°C to +125°C

Storage Temperature.................................. -65°C to +150°C

Maximum Input Voltage VDD .... +0.5V and VCC + 0.5V

Maximum 3.3V Operating Voltage .... 4V (VDD)

Maximum 5V Operating Voltage .... 6V (VCC)

ESD level .... > 2000V

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 3. 2.5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All		-55	25	125	C
V_{DD}	Supply Voltage	All		2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	$V_{IN} = V_{SS}$	-1 70 -5		1 230 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	$V_{IN} = V_{DD\,(Max.)}$	-1 -5 70		1 5 540	µA
I_{OZ}	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (Max.) No pull resistor	-1	–	1	µA
V_{IL}	Low level Input voltage	CMOS				0.3Vdd	V
		PCI				0.325Vdd	
		Schmitt level		0.78		1.25	
V_{IH}	High level Input voltage	CMOS		0.7 Vdd			V
		PCI		0.475Vdd			
		Schmitt level		1.06		1.61	
Delta V	CMOS Hysterisis			0.25	0.34		V
I_{ICS}	Cold sparing leakage input current	PICZ	Vin = 0 to VDDmax	-2		2	µA
I_{OCS}	Cold sparing leakage output current	POxxZ	Vout = 0 to VDDmax	-2		2	µA
V_{CSTH} (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA		0.5		V

Table 3. 2.5V DC Characteristics (Continued)

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
V_{OL}	Low-level Output Voltage [4]	PO11	I_{OL} = 0.8 mA, Vdd = Vdd (Min.)			0.4	V
V_{OH}	High level output voltage [5]	PO11	Ioh = -0.6 mA, Vdd = Vdd (Min.)	2			V
$I_{OS (6)}$	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd (Max.), Vout = Vdd Vouy = Vss			 15 8	mA
I_{CCSB}	Leakage current per cell		Vdd = Vdd (Max.)		0.27	4	nA
I_{CCOP}	Dynamic current per gate		Vdd = Vdd (Max.)			0.32	µW/MHz

1. For standard pull-ups: PRU (#), # = {1-31} index for Ron: Ron = # x RO where RO = 19 kΩ typ, 30 kΩ Max., 12 kΩ Min.
2. For standard pull-downs: PRD (#), # = {1-31} index for Ron: Ron = # x RO where RO = 11 kΩ typ, 30 kΩ Max., 5 kΩ Min.
3. Guaranteed not tested
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 1.6 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -1.6 mA for standard buffers (including cold sparing) measured at Voh = 2.0V
6. Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

Table 4. 3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All		-55	25	125	C
V_{DD}	Supply Voltage	All		2.7	3.0	3.3	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 [1] Pull down resistor PRD1	CMOS	$V_{IN} = V_{SS}$	-1 108 -5		1 330 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 [2]	CMOS	$V_{IN} = V_{DD(Max.)}$	-1 -5 108		1 5 825	µA
I_{OZ}	High impedance state output current	All	VIN = VDD OR VSS, VDD = VDD (Max.) No pull resistor	-1		1	µA
V_{IL}	Low level Input voltage	CMOS				0.8	V
		PCI				$0.325V_{DD}$	
		Schmitt level		0.90		1.42	
V_{IH}	High level Input voltage	CMOS		2			V
		PCI		$0.475V_{DD}$			
		Schmitt level		1.25		1.93	
Delta V	CMOS Hysterisis			0.31	0.42		V

Table 4. 3V DC Characteristics (Continued)

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
I_{ICS}	Cold sparing leakage input current	PICZ	VIN = 0 to VDDmax	-2	–	-2	µA
I_{OCS}	Cold sparing leakage output current	POxxZ	Vout = 0 to VDDmax	-2	–	-2	µA
V_{CSTH} (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA	–	0.5	–	V
V_{OL}	Low-level Output Voltage (4)	PO11	I_{OL} = 1 mA, Vdd = Vdd(Min.)	–	–	0.4	V
V_{OH}	High level output voltage (5)	PO11	Ioh = -0.8 mA, Vdd = Vdd(Min.)	2.4	–	–	V
$I_{OS\ (6)}$	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss	–	–	 21 12	mA
I_{CCSB}	Leakage current per cell	–	Vdd = Vdd(Max.)	–	0.6	5	nA
I_{CCOP}	Dynamic current per gate	–	Vdd = Vdd(Max.)	–	–	0.54	µW/MHz

1. For standard pull-ups: PRU (#), # = {1-31} index for Ron: Ron = # x RO where RO = 15 kΩ typ, 25 kΩ Max., 10 kΩ Min.
2. For standard pull-downs: PRD (#), # = {1-31} index for Ron: Ron = # x RO where RO = 9 kΩ typ, 25 kΩ Max., 4 kΩ Min.
3. Guaranteed not tested.
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -1.8 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):1-C:
   hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -1.8 mA for standard buffers (including cold sparing) measured at Voh = 2.4V
6. Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

Table 5. 3.3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All		-55	25	125	C
V_{DD}	Supply Voltage	All		3	3.3	3.6	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	$V_{IN} = V_{SS}$	-1 120 -5		1 400 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	$V_{IN} = V_{DD(Max.)}$	-1 -5 150		1 5 900	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd(Max.) No pull resistor	-1		1	µA
V_{IL}	Low level Input voltage	CMOS				0.8	V
		PCI				0.325Vdd	
		Schmitt level		0.99		1.51	

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Table 5. 3.3V DC Characteristics (Continued)

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
		CMOS		2			V
		PCI		0.475Vdd			
V_{IH}	High level Input voltage	Schmitt level		1.40		2.08	
Delta V	CMOS Hysterisis			0.37	0.48		V
I_{CS}	Cold sparing leakage input current	PICZ	Vdd = Vss = 0V Vin = 0 to VDD Max	-2		-2	µA
I_{OCS}	Cold sparing leakage output current	POxxZ	Vdd = Vss = 0V Vin = 0 to VDD Max	-2		-2	µA
V_{CSTH} (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA		0.5		V
V_{OL}	Low-level Output Voltage (4)	PO11	I_{OL} = 2 mA, Vdd = Vdd(Min.)			0.4	V
V_{OH}	High level output voltage (5)	PO11	Ioh = -1.8 mA, Vdd = Vdd(Min.)	2.4			V
I_{OS} (6)	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss			 23 13	mA
I_{CCSB}	Leakage current per cell		Vdd = Vdd(Max.)		0.7	5	nA
I_{CCOP}	Dynamic current per gate		Vdd = Vdd(Max.)			0.69	µW/MHz

1. For standard pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ Max., 9 kΩ Min.
2. For standard pull-downs:PRD(#), # = {1-31} index for Ron: Ron = # x RO where RO = 8kΩ typ, 20 kΩ Max., 4 kΩ Min.
3. Guaranteed not tested.
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = -2.0 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = -2.0 mA for standard buffers (including cold sparing) measured at Voh = 2.4V
6. Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

Table 6. 5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All		-55	25	125	C
V_{dd}	Supply Voltage	5V Tolerant		3.0	3.3	3.6	V
V_{cc}	Supply Voltage	5V Compliant		4.5	5	5.5	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	$V_{IN} = V_{SS}$	-1 180 -5		1 690 5	µA

Table 6. 5V DC Characteristics (Continued)

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 [2]	CMOS	$V_{IN} = V_{DD(Max.)}$	-1 -5 30		1 5 400	µA
Ioz	High impedance state output current	All	Vin = Vdd orVss,Vdd=Vdd(max No pull resistor	-1		1	µA
Vil	Low level Input voltage	PICV, PICV5				0.8	V
		PCI				0.325Vdd	
		Schmitt level		0.99		1.51	
V_{IH}	High level Input voltage	PICV, PICV5		2			V
		PCI		0.475Vdd			
		Schmitt level		1.40		2.08	
Delta V	CMOS Hysterisis			0.37	0.48		V
I_{ICS}	Cold sparing leakage input current	PICZ	Vin = 0 to VDDmax	-2		-2	µA
I_{OCS}	Cold sparing leakage output current	POxxZ	Vout = 0 to VDDmax	-2		-2	µA
V_{CSTH} [3]	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA		0.6		V
V_{OL} [4]	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Iol = 0.5 mA Iol = 0.6 mA Iol = 1.2 mA Iol = 1.1 mA Iol = 1.3 mA Iol = 1.5 mA			0.4	V
V_{OH} [5]	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Ioh = 0.5 mA Ioh = 0.6 mA Ioh = 1.2 mA Ioh = 1.1 mA Ioh = 1.3 mA Ioh = 1.5 mA	2 2.4 2.4 2.4 2.4 2.4			V
I_{OS} (6)	Output short circuit current Iosn Iosp	 PO11V PO11V	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss			 28 17	mA

1. For 5V tolerant/compliant pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ Max., 8 kΩ Min.
2. For 5V tolerant/compliant pull-downs: PRD(#), # = {1-31} index for Ron: Ron = # x RO where:
   RO = 19 kΩ typ, 45 kΩ Max., 9 kΩ Min. in 3.3V range,
   RO = 23 kΩ typ, 55 kΩ Max., 11 kΩ Min. in 3V range,
   RO = 36 kΩ typ, 80 kΩ Max., 17 kΩ Min. in 2.5V range,
3. Guaranteed not tested.

4. Tolerant Buffers (including cold spearing):
   IO = -1.0, 1.3, 1.4 mA measured at VOL = 0.4, 0.4, 0.4V in 2.5, 3.0, 3.3V range respectively.
   Compliant Buffers (VCC = 4.5V)
   IO = -1.1, 1.4, 1.6 mA measured at VOL = 0.4, 0.4, 0.4 V in 2.5, 3.0, 3.3V range respectively.
5. Tolerant Buffers (including cold spearing):
   IO = -1.0, -1.3, -1.4 mA measured at VOH = 2.0, 2.4, 2.4V in 2.5, 3.0, 3.3V range respectively.
   Compliant Buffers (VCC = 4.5V)
   IO = -1.1, -1.4, -1.6 mA measured at VOH = 2.0, 2.4, 2.4 V in 2.5, 3.0, 3.3V range respectively.
6. Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

LVDS Driver DC and AC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 7. 2.5V LVDS Driver DC/AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	Core	2.3	2.7	V	–
|VOD|	Output differential voltage	Rload = 100Ω	247	454	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	622	1375	mV	see Figure 4
|Delta VOD| (1)	Change in |VOD|	Rload = 100Ω	0	50	mV	see Figure 4
|Delta VOS| (1)	Change in VOS: Steady-state	Rload = 100Ω	0	50	mV	–
	Change in VOS: Dynamic state		0	100	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.4	4.8	mA	–
Rbias	Bias resistor	–	9.8	10.2	KΩ	1 per chip
Ibias	Bias static current	–	5.8	11.7	mA	
F Max	Maximum operating frequency	VDD = 2.5V ± 0.2V	–	180	MHz	Consumption 14.8 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	669	1178	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	670	1167	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1270	2660	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	110	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

(1) Parameter guaranteed by design, not tested

Table 8. 3V LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	·C	–
V_{DD}	Supply Voltage	Core	2.7	3.3	V	–
|VOD|	Output differential voltage	Rload = 100Ω	247	454	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	622	1375	mV	see Figure 4
|Delta VOD| (1)	Change in |VOD|	Rload = 100Ω	0	50	mV	–
|Delta VOS| (1)	Change in VOS: Steady-state	Rload = 100Ω	0	50	mV	–
	Change in VOS: Dynamic state		0	150	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.6	5	mA	–
Rbias	Bias resistor	–	12.8	13.2	KΩ	1 per chip
Ibias	Bias static current	–	6.5	13.8	mA	–
F Max.	Maximum operating frequency	VDD = 3V ± 0.3V	–	200	MHz	Consumption 18.6 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	512	968	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	512	970	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1150	2300	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	70	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

(1) Parameter guaranteed by design, not tested

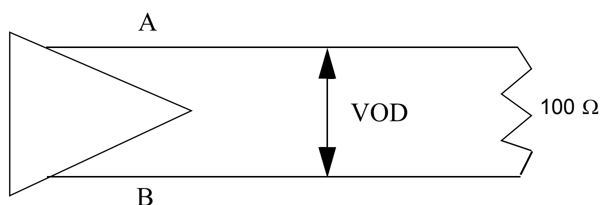
Table 9. 3.3V LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	3	3.6	V	–
|VOD|	Output differential voltage	Rload = 100Ω	247	454	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	622	1375	mV	see Figure 4
|Delta VOD| (1)	Change in |VOD|	Rload = 100Ω	0	50	mV	–

Table 9. 3.3V LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
|Delta VOS| (1)	Change in VOS: Steady-state	Rload = 100Ω	0	50	mV	–
	Change in VOS: Dynamic state		0	200	mV	–
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delta VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	200	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.2	mA	–
ISAB	Output current	Drivers shorted together	2.6	4.8	mA	–
Rbias	Bias resistor	–	16.3	16.7	kΩ	1 per chip
Ibias	Bias static current	–	7	14.6	mA	–
F Max.	Maximum operating frequency	VDD = 3.3V ± 0.3V	–	220	MHz	Consumption 20.9 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	445	838	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	445	841	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1120	2120	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	80	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Figure 4. Test Termination Measurements



$$VOS = \frac{(VA + VB)}{2}$$

Figure 5. Rise and Fall Measurements

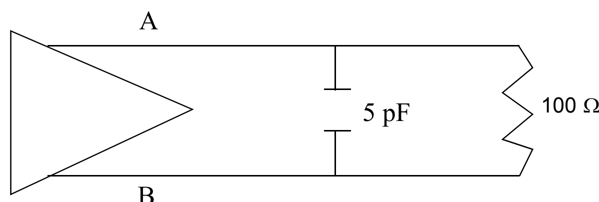


Table 10. LVDS Receiver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	·C	–
V_{DD}	Supply Voltage	–	2.3	3.6	V	–
Vi	Input voltage range	–	0	2400	mV	–
Vidth	Input differential voltage	–	-100	+100	mV	–
Tp	Propagation delay	Cout = 50 pF, VDD = 2.5V ± 0.2V Cout = 50 pF, VDD = 3.0V ± 0.3V Cout = 50 pF, VDD = 3.3V ± 0.3V	0.9 0.7 0.7	3.5 2.7 2.4	ns	–
Tskew	Duty cycle distortion	Cout = 50 pF	-	500	ps	–

Table 11. I/O Buffers DC Characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3V	5.6	pF
$C_{I/O}$	Capacitance, Bi-Directional	3V	6.6	pF

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of a Gate Array/Embedded Array, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of a Gate Array/Embedded Array, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The MH1RT Series are offered in ceramic packages: multi-layer quad flat packs (MQFP), multi - layer column grid array (MCGA) and multi-layer land grid array (MLGA). Packages lid may be connected to ground or not.

Table 12. Packaging Options

Package Type [1,2]	Pin Count
MQFP	132,196, 256 and 352
MCGA and MLGA	349, 472 (1.27 mm pitch)

Notes: 1. Contact Atmel local design centers to check the availability of the matrix/package combination.
2. Four decks packages.

Document Revision History

4110K - 11/07

1. Added missing ESD information. See pages 1 & 8.

4110L - 11/10

1. Add LGA package option
2. Correction of LVDS transmitter tables (VOL/VOH)

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